

Ultrahigh-Performance Differential-Output Programmable-Gain Instrumentation Amplifier for Data Acquisition

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Data-acquisition systems and programmable-logic controllers (PLCs) require versatile high-performance analog front ends that interface with a variety of sensors to measure signals accurately and reliably. Depending on the particular type of sensor and the magnitude of the voltage or current being measured, the signal may need to be amplified or attenuated to match the full-scale input range of the analog-to-digital converter (ADC) used for further digital processing and feedback control.

Typical voltage measurement spans in data-acquisition systems range from ± 0.1 V to ± 10 V. By choosing the correct voltage range, the user implicitly changes the system gain to maximize the amplitude of the sampled voltage at the input of the analog-to-digital converter (ADC), which, in turn, maximizes the signal-to-noise ratio (SNR) and measurement accuracy. In typical data-acquisition systems, signals that require attenuation and signals that require amplification are processed by different signal paths. This usually results in a more complex system design, requires extra components, and uses more board space. Solutions that offer attenuation and amplification in the same signal path generally use programmable-gain amplifiers and variable-gain amplifiers, but these amplifiers do not usually offer the high dc precision and temperature stability required by many industrial and instrumentation applications.

One way to build a powerful analog front end that provides both attenuation and amplification in a single signal path—and differential outputs to drive high-performance analog-to-digital converters—is to cascade a programmable-gain instrumentation amplifier (PGIA), such as the AD8250 (gain of 1, 2, 5, or 10), AD8251 (gain of 1, 2, 4, or 8), or AD8253 (gain of 1, 10, 100, or 1000), with a fully differential funnel (attenuating) amplifier, such as the AD8475, in a circuit similar to that shown in Figure 1. This solution offers simplicity, flexibility, and high speed—along with excellent precision and temperature stability.

The aforementioned programmable-gain instrumentation amplifiers, featuring $5.3\text{-G}\Omega$ differential input impedance and -110-dB total-harmonic distortion (THD), are ideal for interfacing with a wide variety of sensors. At a gain of 10, guaranteed specifications for the AD8250 include: 3-MHz bandwidth, $18\text{-nV}/\sqrt{\text{Hz}}$ voltage noise, 685-ns settling time to 0.001%, $1.7\text{-}\mu\text{V}/^\circ\text{C}$ offset drift, $10\text{-ppm}/^\circ\text{C}$ gain drift, and 90-dB common-mode rejection from dc to 50 kHz. This combination of precision dc performance coupled with high speed makes the amplifiers well-suited for data-acquisition applications with multiplexed inputs.

The AD8475 high-speed, fully differential funnel amplifier with integrated precision resistors provides precision attenuation of 0.4 or 0.8, common-mode level-shifting, single-ended-to-differential conversion, and input overvoltage protection. This easy-to-use, fully integrated precision gain block is designed to process signal levels up to ± 10 V using a single +5 V supply. As a result, it can match industrial-level signals with the differential input voltage range of low-voltage high-performance 16-bit and 18-bit successive-approximation (SAR) ADCs with sampling rates of up to 4 MSPS.

The AD825x and AD8475, working together as shown in Figure 1, provide a flexible high-performance analog front end. Table 1 shows the gain combinations that can be achieved, depending on the input and output voltage range requirements.

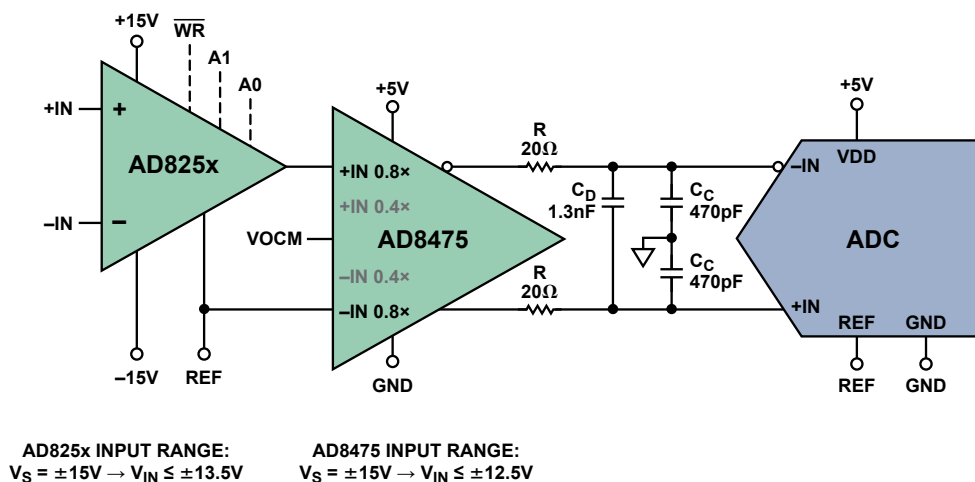


Figure 1. Data-acquisition analog front end that uses the AD825x PGIA and AD8475 differential-output funnel amplifier.

Table 1. Input Voltage Ranges and Gains Possible with the AD8475 in Combination with the AD8250, AD8251, and AD8253

DAQ Instrument Measurement Range (V)	Peak-to-Peak Voltage (V)	ADC Max Voltage per Input (V)	Overall System Gain	AD825x Gain	AD8475 Gain	Peak-to-Peak Voltage at ADC Input	AD825x Input Voltage Limit Needed (to Protect ADC)	
±10	20	4.096	0.4	1	0.4	8	10.24	AD8250 Gain
±5	10	4.096	0.8	2	0.4	8	5.12	
±2	4	4.096	2	5	0.4	8	2.048	
±1	2	4.096	4	10	0.4	8	1.024	
±5	10	4.096	0.8	1	0.8	8	5.12	
±2.5	5	4.096	1.6	2	0.8	8	2.56	
±1	2	4.096	4	5	0.8	8	1.024	
±0.5	1	4.096	8	10	0.8	8	0.512	
±10	20	4.096	0.4	1	0.4	8	10.24	AD8251 Gain
±5	10	4.096	0.8	2	0.4	8	5.12	
±2.5	5	4.096	1.6	4	0.4	8	2.56	
±1	2	4.096	3.2	8	0.4	6.4	1.28	
±5	10	4.096	0.8	1	0.8	8	5.12	
±2.5	5	4.096	1.6	2	0.8	8	2.56	
±1	2	4.096	3.2	4	0.8	6.4	1.28	
±0.5	1	4.096	6.4	8	0.8	6.4	0.64	
±10	20	4.096	0.4	1	0.4	8	10.24	AD8253 Gain
±1	2	4.096	4	10	0.4	8	1.024	
±0.1	0.2	4.096	40	100	0.4	8	0.1024	
±0.01	0.02	4.096	400	1000	0.4	8	0.01024	
±5	10	4.096	0.8	1	0.8	8	5.12	
±0.5	1	4.096	8	10	0.8	8	0.512	
±0.05	0.1	4.096	80	100	0.8	8	0.0512	
±0.005	0.01	4.096	800	1000	0.8	8	0.00512	

Capabilities: Input Voltage Range and Bandwidth

The maximum input voltage range for the AD825x family of PGIAs is about ±13.5 V when operating on ±15-V power supplies (the AD8250 and AD8251 provide additional overvoltage protection of up to 13 V beyond the power-supply rails). In this application, the effective limit on the PGIA input voltage range is set by the full-scale voltage range of the ADC inputs and the signal path gain from the sensor to the ADC. For example, the [AD7986](#) 18-bit, 2-MSPS PulSAR ADC operates on a single +2.5-V supply, with a typical 4.096-V reference voltage. Its differential inputs accept up to ±4.096 V (0 V to 4.096 V and 4.096 V to 0 V on the inputs). If the overall gain of the analog front end is set to 0.4, with the AD825x configured for a gain of 1 and the AD8475 configured for a gain of 0.4, the system can process an input signal with a maximum magnitude of ±10.24 V.

To determine the combination of gain settings required in any system, consider the full-scale input voltage of the ADC (VFS) and the minimum/maximum current or voltage levels expected from the sensors.

$$GAIN_{SYSTEM} = GAIN_{AD825x} \times GAIN_{AD8475}$$

$$V_{INmax} = \frac{V_{FS(ADC)}}{GAIN_{SYSTEM}}$$

The speed and bandwidth of this analog front end is exceptional given its level of precision and functionality. The speed and bandwidth capabilities of this circuit are determined by the

following combination of factors:

- AD825x settling time: For a 10-V output voltage step, the AD8250 settles to 0.001% (16 bits) in 615 ns.
- AD825x slew rate: The AD825x slews at a rate between 20 V/μs and 30 V/μs depending on the gain setting. The AD8475 slews at a rate of 50 V/μs, so the system is limited by the AD825x slew rate.
- Antialiasing filter (AAF) cutoff frequency: This user-determined filter band-limits the signal presented at the ADC inputs to prevent aliasing and improve the SNR of the signal chain (see amplifier and ADC data sheets for details).
- ADC sample rate: The AD8475 can drive up to 4-MSPS converters with 18-bit resolution.

Many data-acquisition and process-control systems measure pressure, temperature, and other low-frequency input signals, so the dc precision and temperature stability of the front-end amplifiers are critical to the system performance. Many of these applications include multiple sensors that are multiplexed to the amplifier inputs in a polling fashion. Typically, the polling frequency is much greater than the bandwidth of the signal of interest. When the multiplexer switches from one sensor to the next, the voltage change seen by the amplifier inputs is unknown, so the design must accommodate the worst-case scenario: a full-scale voltage step. The amplifier must be able to settle from this full-scale step within the time allotted to switching. This settling time also needs to be lower than the settling time required by the ADC to sample and acquire the signal.

An antialiasing filter (AAF) is recommended between the AD8475 and the ADC's inputs. The AAF band-limits the signal and the noise presented to the ADC inputs to prevent undesirable aliasing effects and to improve the system SNR. Additionally, the AAF absorbs some of the ADC input transient currents, so the filter also provides some isolation between the amplifier and the ADC's switched-capacitor inputs. Typically, the AAF is implemented using a simple RC network as shown in Figure 1. The following equations describe the filter bandwidth:

$$FilterBW_{DIFF} = \frac{1}{2\pi \times 2RC_D}$$
$$FilterBW_{CM} = \frac{1}{2\pi \times RC_C}$$

In many cases, the filter's R and C values are optimized empirically to provide the necessary bandwidth, settling time, and drive capability for the ADC. Refer to the ADC data sheet for specific recommendations.

Conclusion

Together, the AD8475 and AD825x family of PGAs implement a simple analog front end that provides high performance, functionality, and flexibility. A variety of programmable gain combinations are possible for both amplification and attenuation, allowing different measurement voltage ranges to be optimized. The AD825x's performance and programmability are well-suited for multiplexed measurement systems, and the AD8475 provides

an excellent interface to precision analog-to-digital converters. The two amplifiers work well together to retain the integrity of the sensor signal, as a high-performance analog front end for industrial measurement systems.

See [Circuit Note CN-0180, Precision, Low Power, Single-Supply, Fully Integrated Differential ADC Driver for Industrial-Level Signals](#) for additional information on the AD8475 as a driver for a precision successive-approximation ADC.

Authors

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