Transformer-Coupled Front-End for Wideband A/D Converters

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INTRODUCTION

With the push into higher-frequency IF sampling, the analog inputs and overall front-end design of the A/D converter have become crucial elements of receiver design. Many applications are migrating to super-Nyquist sampling in order to eliminate a mix-down stage in the system design. Amplifiers pose a problem at these high frequencies, because high performance isn't as easy to achieve as in the Nyquist applications for which they are typically used. In addition, the amplifier's inherent noise will degrade the ADC's signal-to-noise ratio (SNR), no matter what input frequency is used. A transformer provides the designer with a relatively easy solution that resolves the noise issue, while providing a good coupling mechanism for high-frequency inputs.

The Transformer

Let us look at the basic makeup of a transformer and summarize what it provides to the user. First, the transformer is inherently ac-coupled, since it is galvanically isolated and will not pass dc levels. It provides the designer with basically noise-free gain, which depends on the designer's choice of turns ratio. The transformer also provides a quick and easy way of translating from a single-ended to a differential circuit. Finally, a center-tapped transformer provides the freedom to set the common-mode level arbitrarily. This combination of virtues reduces component count in front-end designs, where it is critical to keep complexity at a minimum.

However, care should be taken when using center-tapped transformers. If the converter circuit presents large imbalances between the differential analog inputs, a large amount of current could flow through the transformer's center tap, possibly saturating the core. For example, instability could result if V_{REF} is used to drive the center tap of the transformer, and a full-scale analog signal overdrives the ADC's input, turning on the protection diodes.

Although simple in appearance, transformers should not be taken lightly. There is much to know about and learn from them. Let's look at a simple model of the transformer and see what is "under the hood." A couple of simple equations relate the currents and voltages occurring at the terminals of an ideal transformer, as shown in Figure 1. When voltage is stepped up by a transformer, its impedance load will be reflected back to the input. The turns ratio, $a = N1/N2$, defines the ratio of primary voltage to secondary voltage; the currents are inversely related ($a = I2/I1$), and the ratio of the impedance seen in the primary reflected from the secondary goes as the square of the turns ratio ($Z1/Z2 = a^2$). The transformer's signal gain is expressed simply as 20 log (V2/V1) = 20 log √(Z2/Z1), so a transformer with a voltage gain of 3 dB would have a 1:2 impedance ratio. That makes for an easy first step of the design.

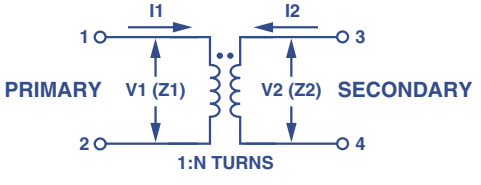

Figure 1a. Transformer input and output variables.

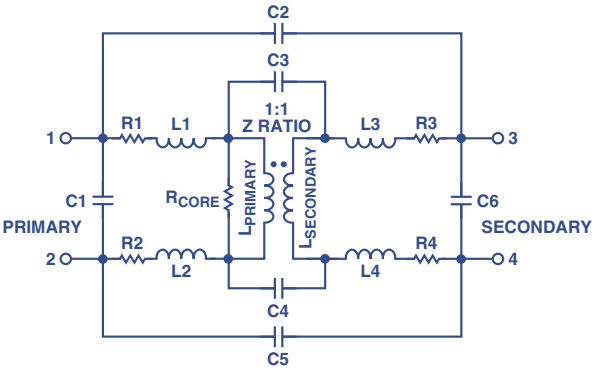

Figure 1b. Typical transformer model.

Figure 1b shows many of the inherent and parasitic departures from the ideal that come into play with a transformer. Each of these has a role in establishing the transformer's frequency response. They can help or hinder performance, depending on the front-end implementation. Figure 1b provides a good way to model a transformer to get first-order expectations. Some manufacturers provide modeling information, either on their website or through a support group. Anyone planning to do the model analysis using the hardware will need a network analyzer and a handful of samples to make all of the measurements properly.

Real transformers have losses and limited bandwidth. As the configuration of parasitics implies, one can think of a transformer as a wideband bandpass filter, which can be defined in terms of its –3-dB points. Most manufacturers will specify transformer frequency response in terms of the 1-, 2-, and 3-dB bandwidth. The amplitude response is accompanied by a phase characteristic. Usually a good transformer will have a 1%-to-2% phase imbalance over its frequency passband.

Let us now consider some design examples involving a transformer-coupled front-end for an ADC. Since the transformer is used primarily for isolation and center-tapping, these examples will be simplified for discussion by using a unity turns ratio.

Examples

In the first example, shown in Figure 2, an AD6645[1] 14-bit, 80-Msps ADC, with a differential input impedance of 1 kohm, is used. The 33-ohm series resistors provide isolation from transient currents in the input circuit of the ADC. The 501-ohm terminating resistor is chosen to achieve a 50-ohm input on the primary to match the 50-ohm analog input source. Thus

$$R_{in} = 58\Omega \,\|\, \left(66\Omega + \left(501\Omega \,\|\, 1000\Omega\right)\right) = 50.65\Omega \qquad (1)$$

The resistive combination in the transformer secondary is effectively in parallel with the 58-ohm resistor. The choice of terminating resistor depends on the desired input impedance. For simplicity, it will be assumed that a match to a 50-ohm source is required for all of the examples in this section.

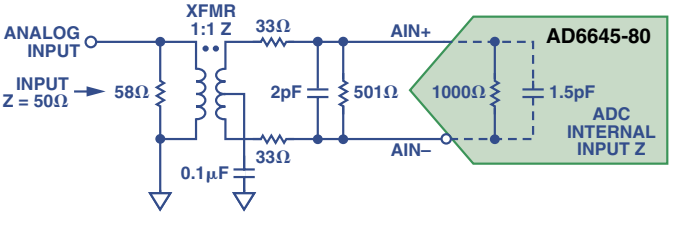

Figure 2. A 1:1 transformer coupling a 50-ohm input source with an ADC having a known input impedance.

This is an easy example because we assume that the input frequency is in baseband or first Nyquist zone. However, the situation is quite different if the front-end design is called on to handle a 100-MHz analog input. What happens in the transformer? With such a high IF frequency applied, any difference in parasitic capacitive coupling (C2–C5 in Figure 1b) unbalances the secondary outputs of the transformer. The resulting asymmetry gives rise to even-order distortions at the converter's analog input, which leads to 2nd-order harmonic distortions in the digital signal.

To illustrate this point, Figure 3 shows the voltages on the secondary when a 2-V p-p sinusoidal input is applied to the primary (100 MHz in Figure 3a and 200 MHz in Figure 3b). The secondary outputs are each expected to produce a 1-V p-p sine wave. But at 100 MHz, their amplitudes deviate by 10.5 mV p-p, with 0.5° phase imbalance. And at 200 MHz, the amplitude difference is 38 mV p-p, or 1.9%.

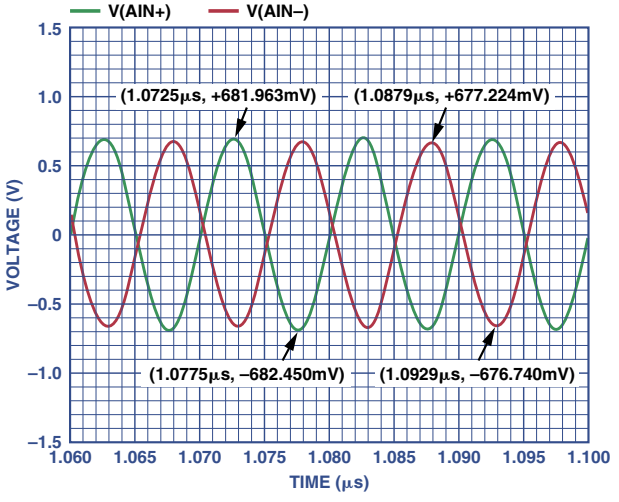

Figure 3a. 100-MHz input. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.364 V p-p, AIN– (red) = 1.354 V p-p, Difference = 10.45 mV p-p.

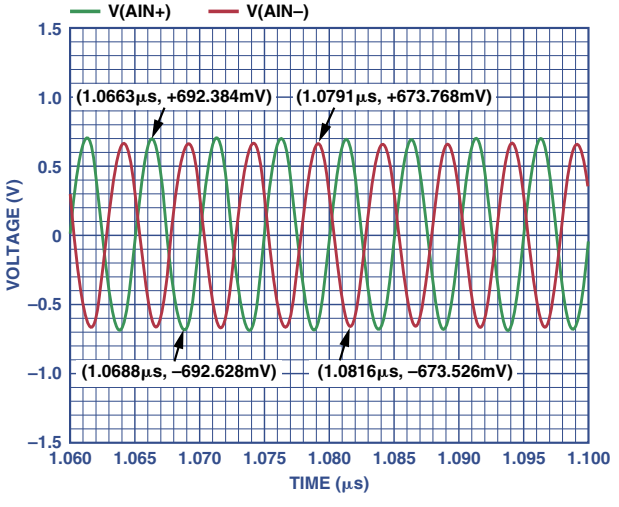

Figure 3b. 200-MHz input. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.385 V p-p, AIN– (red) = 1.347 V p-p, Difference = 37.72 mV p-p.

One way to improve the situation is to apply a second transformer in cascade with the first to provide additional isolation and reduce the unbalanced capacitive feedthrough (Figure 4).

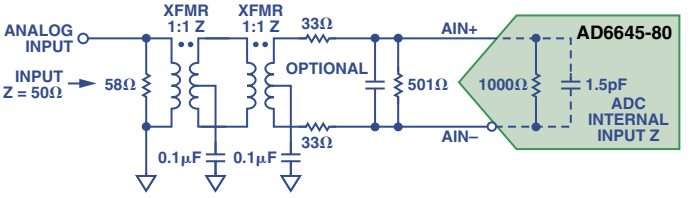

Figure 4. Cascaded transformers.

Using this scheme, the differential voltages applied to the converter are less likely to deviate from one another, particularly at high frequencies where this matters most. Figure 5 illustrates this point: the first transformer's secondary differences in parasitic coupling capacitances, C1 and C2, are reduced. The second transformer in cascade enables a redistribution of the core current lost and provides more equal signals to the primary of the second transformer. The two cascaded transformers in this configuration provide a better balanced solution for high frequencies.

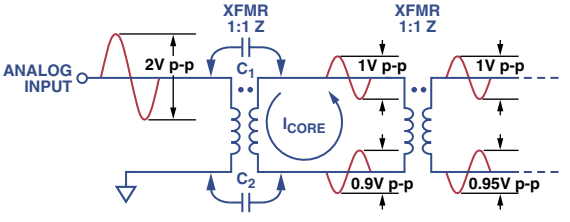

Figure 5. Two transformers in cascade improve signal balance.

The performance benefit can be seen in Figure 6 from the simulation. In Figure 6a, with an analog input of 100 MHz, the deviation drops to 0.25 mV p-p, or 0.013%. And at 200 MHz (Figure 6b), there is only a 0.88 mV p-p difference between the transformer's secondary outputs, or 0.044%. This is a big improvement, attained by adding one extra component.

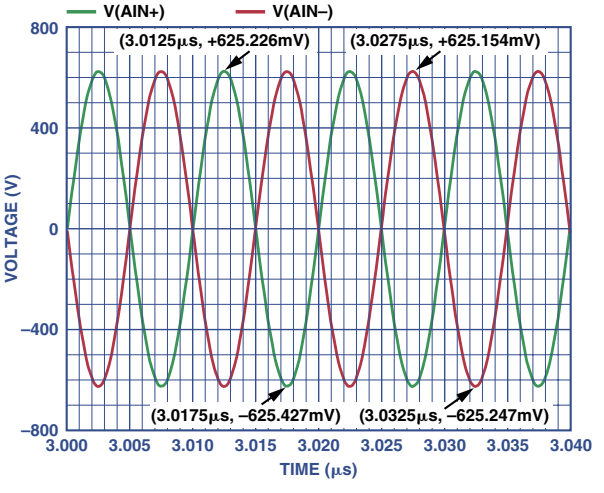

Figure 6a. 100 MHz. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.25 V p-p, AIN– (red) = 1.25 V p-p, Difference = 0.25 mV p-p.

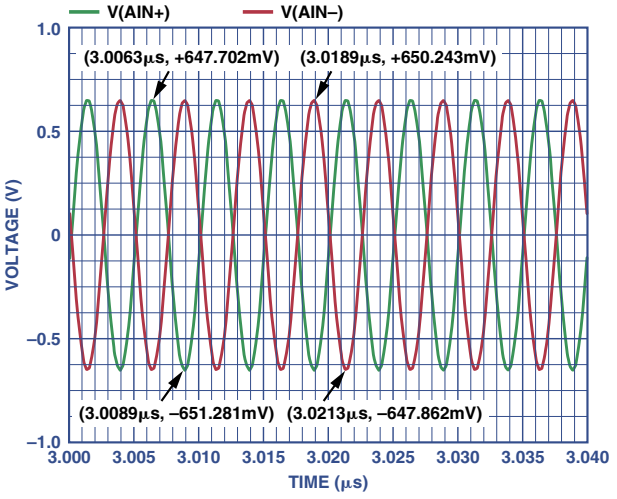

Figure 6b. 200 MHz. Simulation of the transformer's secondary outputs: AIN+ (green) = 1.298 V p-p, AIN– (red) = 1.298 V p-p, Difference = 0.88 mV p-p.

Another way to approach this is to use a two-balun type transformer configuration. A balun (balance-unbalance) acts like a transmission line and usually has greater bandwidth than the standard flux type transformers discussed earlier. They can provide good isolation between the primary and secondary with relatively low loss. However, they require more power to drive because the input impedance is halved from the primary to the secondary. Figure 7a shows a common implementation that is used in order to achieve a wide passband. In Figure 7b, the balun type transformer is precompensated for the imbalance.

Response Peaking

Figure 8a shows a typical transformer frequency response, essentially that of a wideband filter with bandwidth in excess of 100 MHz. An inductor in series with the transformer's primary can be used to alter the bandwidth response of the transformer, by peaking the gain in the passband and providing a steeper roll-off outside the passband (Figure 8b). The inductor has the effect of adding a zero and a pole in the transfer function.

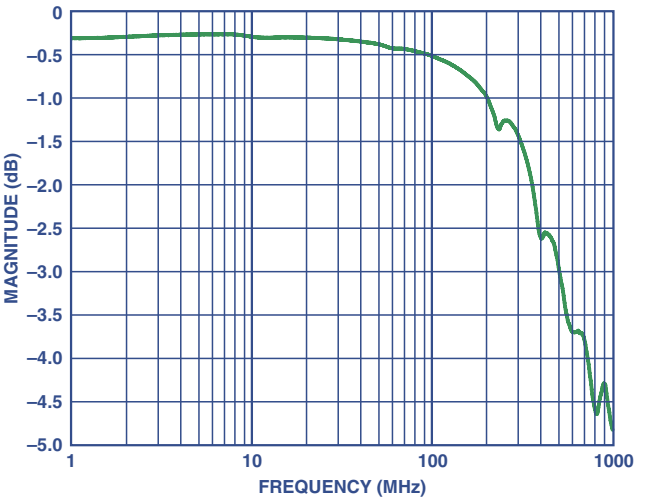

Figure 8a. Frequency response of a typical transformer.

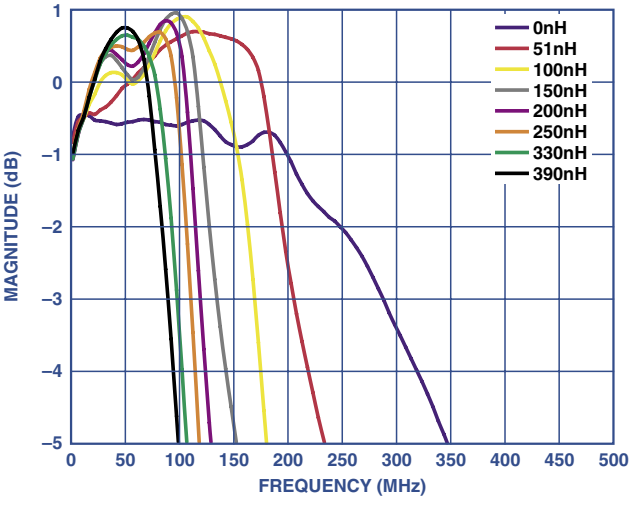

Figure 8b. Frequency response of a typical transformer with an inductor in series.

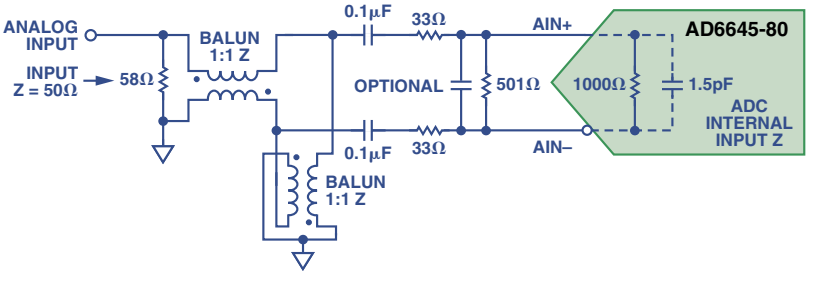

Figure 7a. Transformer-coupled input using a two-balun type transformer configuration.

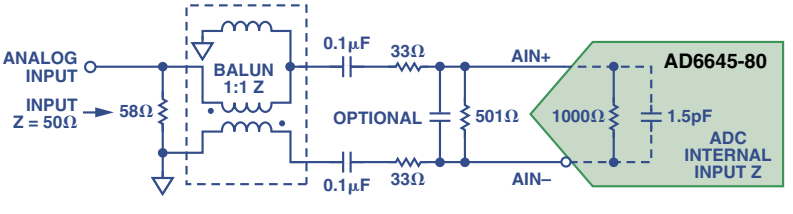

Figure 7b. Transformer-coupled input using a compensated-balun type transformer.

Figure 9 shows the circuit of Figure 2 with a series inductor. The value of inductance depends on the desired amount of peaking and bandwidth. However, the designer should note that this peaking could be undesirable where flatness of response and well-behaved phase response are important criteria.

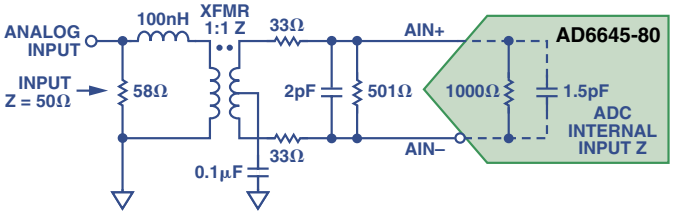

Figure 9. Inductor compensated 50-ohm input impedance with a 1:1 transformer and known ADC input impedance.

Switched-Capacitor ADCs

Up to this point we have only talked about interfacing ADCs with a known input impedance, using as an example the AD6645-80. But what about an ADC that has a switched-capacitor interface? Switched-capacitor ADCs have no internal buffer, so the user is making a connection directly with the internal sampling circuit—which has an impedance that varies widely with applied input frequency. In Figure 10, the A/D converter is the AD9236-80[2] with a 10-MHz analog input. In *track* (sample) mode, the input looks like a 4,135-ohm differential impedance in parallel with a 1.9 pF capacitor. But the *hold* mode will look different. Application Note AN-742[3] provides good information on getting these analog input impedance values. Many of ADI's switched-capacitor ADC values can be downloaded in spreadsheet form at the ADC's product page on the Analog Devices website, giving both *track-and-hold* values from 0.3 MHz to 1 GHz.

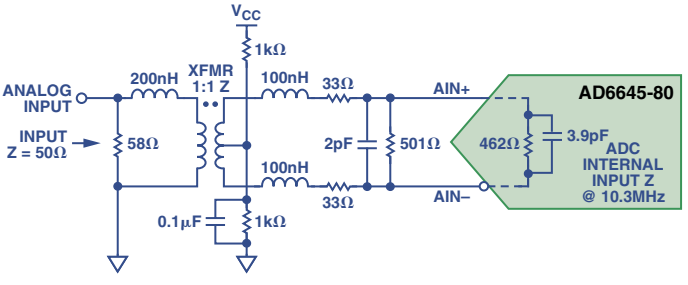

Figure 10. Switched-capacitor front-end implementation.

The 200-nH series inductance is meant to cancel out the reactance of the input capacitor that was reflected back from the ADC's input, making the input look as resistive as possible in order to achieve a good 50-ohm termination in the frequency band of interest. Note that other inductance values might be used to set the bandwidth and gain flatness desired, as seen in Figure 8b.

For all the examples discussed here, a 1:1 turns ratio (impedance ratio) was used. So the transformer provides a nominal voltage gain of 0 dB. This is the easiest type of transformer to configure, because the transformer's parasitics are relatively easy to understand and compensate for. However, some applications may require inherent voltage gain, when the input signals are low. Using a turns ratio of 1:2 or 1:4 (impedance ratio of 4 or 16), the transformer provides respective voltage gains of 6 dB or 12 dB.

The benefit here is that, unlike an amplifier, a transformer generates essentially no noise. However, the parasitics in a 1:2 or 1:4 transformer are much more difficult to compensate for, particularly over a wide range of frequencies. With a 1:2 turns ratio, for example, the capacitive terms quadruple while the inductive and resistive terms go down to one-fourth their original value. For a 1:4 turns ratio, the same terms go up or down by a factor of 16. The challenge is even more difficult when interfacing with a switched-capacitor-input ADC, because the capacitive terms are both large and variable with frequency. Considering the difficulties, the best way to undertake a design such as this is to optimize for the center frequency of interest within the given band.

CONCLUSION

An experienced designer will note that our discussion has focused largely on ideal circuit relationships and, while hinting at the turns-ratio and parasitic issues—and some of the architectural design approaches to dealing with them—we have only skimmed the surface. So what is to be done when tackling a new design? The designer needs to know as much as possible about the transformer selected for the design in relation to the ADC. The best way to do this in any front-end design is to investigate the parasitics that come into play over the frequencies of interest. Proper design and analysis involves the use of a network analyzer. It will show how the front-end design acts over a given frequency range with respect to impedance, VSWR, insertion loss, and differential phase mismatch—thus providing much key information on how the ADC will work in a transformer-coupled application.

FURTHER READING

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