

How to Save Power in Battery Applications Using the Power-Down Mode in an ADC

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Size and power consumption are two critical features in portable battery-powered applications. Otherwise acceptable components can be designed out of portable systems based on deficiencies in these two features alone. Everybody desires smaller, more compact mobile phones, MP3 players, PDAs, and digital cameras—with increased time between battery charges or replacement. For semiconductor manufacturers, this translates into a requirement for lower power ICs with high performance and the same—or even extra—features in ever smaller packages.

In portable battery-powered applications, battery life is a critical concern to the system designer. Battery discharge curves differ, depending on the type of battery and the current drain. For example, Figure 1 shows the typical discharge curves for a Lithium/MnO₂ (primary) cell with three typical current loads. They show that the higher the current it must supply, the shorter the battery's life. Since even small amounts of current shorten the battery's life, minimizing the current drawn quiescently by the system components when not operating—or whenever possible during operation—can extend battery life.

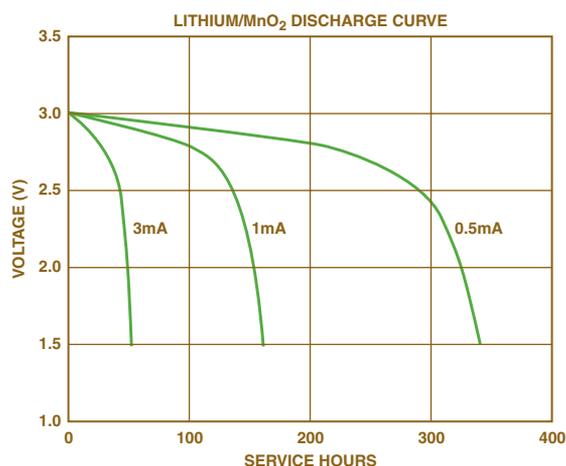


Figure 1. Typical discharge curves.

Nowadays, almost every analog/digital converter (ADC) sold into the battery-powered device market provides a power-down mode as a standard feature. The technique used to place the ADC into the power-down state—and its effectiveness—differ from part to part.

Some ADCs have a dedicated shut-down pin to shift the device into power-down mode. The weakness of this approach is that an extra pin, which results in increased pin count for the ADC, can increase the package size. Other ADCs, like the AD7887, require a *write* to an on-board control register to produce a power-down state. This is generally the case with multichannel ADCs, where an internal register is used for channel selection as well as mode selection. This on-board register also means an extra DATA IN serial interface pin.

In order to cut down on pin count, some recent ADCs use the standard interface lines to implement power-down modes; an example is the 12-bit, 1-MSPS AD7476A, available in the tiny 6-pin SC-70 package.

The AD7476A's 3-wire read-only serial interface not only controls the conversion process and accesses the conversion result from the ADC—it is also used to establish the device's different operating modes. The mode of operation is selected by controlling the state of \overline{CS} (*conversion start*) during a conversion. This has the advantage that the signals required to change modes are standard serial interface signals.

The serial interface consists of the \overline{CS} , SCLK, and SDATA lines. A normal conversion requires sixteen serial clock pulses for completion. The \overline{CS} signal is used to initiate the conversion and to frame the sixteen serial clocks. After the conversion has been initiated, the time at which \overline{CS} is pulled *high* will determine if the AD7476A will enter power-down mode—or, if already in a power-down mode, whether or not the AD7476A will return to normal operation. Changing the mode of operation can easily be done with a standard 8- or 16-pulse SCLK burst from a microcontroller—or with a framing signal of any length from a DSP.

Figure 2 shows the timing diagram during a normal conversion, and Figure 3 shows how the power-down mode can be entered by controlling the \overline{CS} signal. This mode of operation is designed to provide flexible power management options and to minimize power dissipation for different application requirements.

To reduce power consumption and maintain battery life, the AD7476A should be placed into its low power state between conversions or after a burst of several conversions.

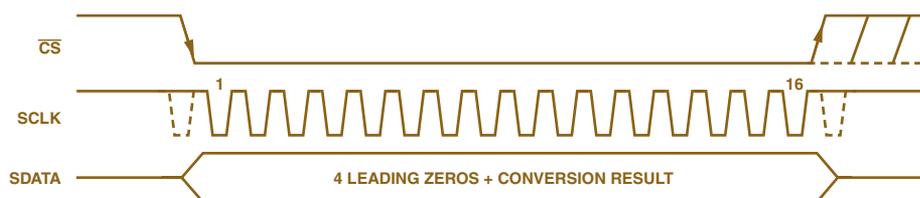


Figure 2. Serial interface signals in a normal conversion.

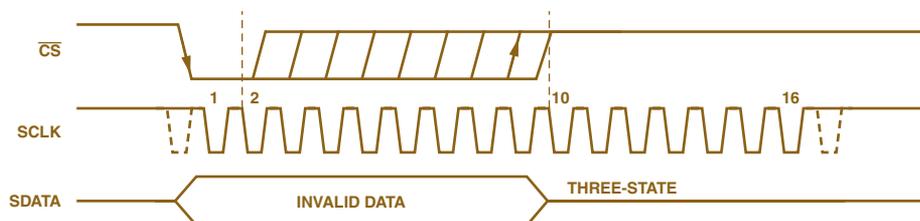


Figure 3. Using the serial interface signals to enter power-down mode.

More about the AD7476A

The AD7476A is a 12-bit successive approximation (SAR-type) ADC, operating on a 2.35-V to 5.25-V supply and capable of throughput rates of up to 1 MSPS. The AD7476A combines CMOS technology and advanced design techniques to achieve low power-dissipation at high throughput rates.

The AD7476A's average power consumption during the cycle time is determined by the percentage of time it spends in a full power state (operational), as compared to the interval spent in a low power state (power down). The greater the time spent in power-down, the lower the average power consumption.

To achieve the lowest power dissipation with the AD7476A, the conversion should be run as quickly as possible. Since the conversion time is determined by the SCLK frequency, the faster the SCLK frequency, the shorter the conversion time. Thus, the device can remain in the power-down mode for a longer interval and will dissipate maximum power for a shorter time.

Figure 4 shows the average power consumption by the AD7476A for different SCLK frequencies with a fixed throughput rate of 100 kSPS. The ADC is put in the power-down mode after the conversion is complete, and is powered up by means of a dummy conversion. As the plot shows, the faster the clock frequency, the lower the average power consumption.

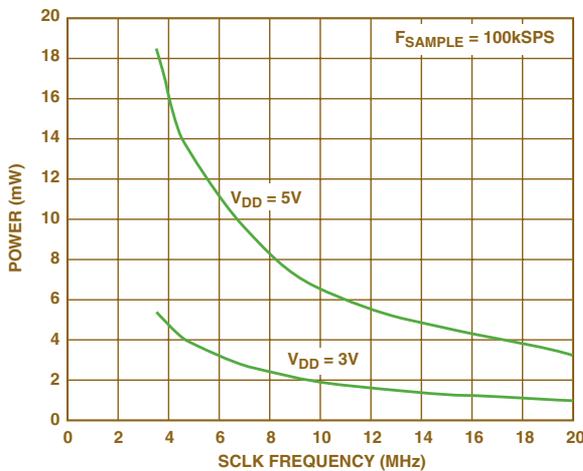


Figure 4. AD7476A power consumption for different serial clock frequencies.

Figure 5 shows that for a fixed SCLK frequency of 20 MHz, when operating the ADC at low throughput rates, the average power consumed by the ADC is very low. However, as the throughput rate increases, the average power consumption increases, because the ADC remains in a power-down state for a shorter period of time compared to the time in the operating state. The other plot shows the average power consumed by the ADC when there is no power-down mode implemented between conversions. Together they show that—while at lower throughput rates significant power savings can be achieved by placing the ADC into a power-down state between conversions—increasingly diminished power savings accrue as the conversion rate increases. For example, at 300 kSPS, the difference between the two cases is less than 0.5 mW.

A further step in the different power-down modes implemented through standard serial interface signals is the *automatic* power-down mode. Following the trend of very low power ADCs for portable battery-powered applications, Analog Devices has recently

made available the AD7466, a *micropower*, 12-bit SAR-type ADC housed in a 6-lead SOT-23 package. It can be operated from 1.6 V to 3.6 V and is capable of throughput rates of up to 200 kSPS.

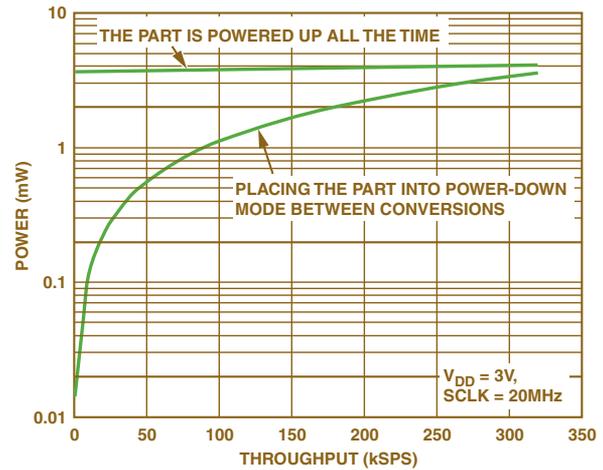


Figure 5. AD7476A power consumption comparison.

The AD7466 powers up prior to conversion and returns to power-down mode when the conversion is complete; this eliminates the need for dummy conversions. In the same way as for the AD7476A, the AD7466's conversion time is determined by SCLK, allowing the conversion time to be reduced by increasing the serial clock speed, thus providing the same kind of power saving.

Figure 6 shows the AD7466's power consumption for different throughput rates, serial clock frequencies, and supplies. The current consumption in power-down mode is typically 8 nA. The AD7466 consumes 0.9 mW max when operating at 3 V, and 0.3 mW max for 1.8 V operation at 100 kSPS.

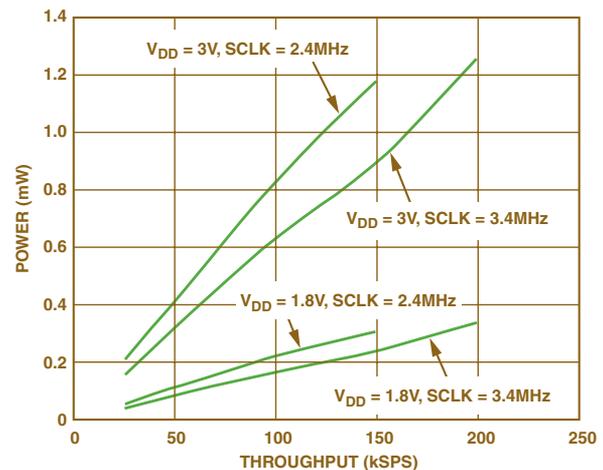


Figure 6. AD7466 power consumption vs. throughput rate for different SCLK and supply voltages.

We have shown that faster SCLK frequencies and longer power-down modes greatly reduce the average power consumed by the ADC. These power savings, combined with the space-saving 6-lead 2 mm × 2.1 mm SC70 surface-mount package, make the AD7476A an ideal candidate for portable battery-powered applications and a very compact alternative to other solutions. And for extremely low-power-budget applications powered at ≤3.6 V, the AD7466 is the ideal solution. □