



# ***Reliability Report***

**Report Title:** ADN4680E New Product  
Qualification in LFCSP (Cu bond  
wires)

**Report Number:** 16622

**Revision:** A

**Date:** 18 August 2021

## Summary

This report documents the successful completion of the interim reliability qualification requirements for the release of the ADN4680E product in a 48-LFCSP package using copper bond wires, assembled at ASE (AEK). The ADN4680E comprises four multipoint, low voltage differential signaling (M-LVDS) transceivers (driver and receiver pairs) that can operate at up to 250 Mbps (125 MHz).

**Table 1: ADN4680E Product Characteristics**

### Die/Fab

Die Id	TMMK91 A
Die Size (mm)	3.20 x 3.38
Wafer Fabrication Site	E_TSMC1008
Wafer Fabrication Process	0.35µm DMOS
Approximate Transistor Count	7,000
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu(0.5%)

### Package/Assembly

Package	48-LFCSP
Body Size (mm)	7.00 x 7.00 x 0.75
Assembly Location	ASE (AEK)
Molding Compound	Sumitomo G700LYT
Die Attach	Hitachi EN 4900GC conductive
Wire Type	MKE APC PdCuAu
Wire Diameter (mil)	0.8
Lead Frame Material	Copper
Lead Finish	Matte Sn
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

## Description / Results of Tests Performed

Tables 2 through 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

**Table 2: LFCSP at ASE (AEK) Package Qualification Test Results**

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADN4680E	Q16622.HS1	50	0
				Q16622.HS2	50	0
				Q16622.HS3	50	0
Solder Heat Resistance (SHR) <sup>1</sup>	J-STD-020	MSL-3	ADN4680E	Q16622.SH1	15	0
				Q16622.SH2	15	0
				Q16622.SH3	15	0
Temperature Cycling (TC) <sup>1</sup>	JESD22-A104	- 65C/+150C 2 Cyc/Hr, 500 Cycles	ADN4680E	Q16622.TC1	77	0
				Q16622.TC2	77	0
				Q16622.TC3	77	0
Temperature Humidity Bias (THB) <sup>1</sup>	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADN4680E	Q16622.TH1	77	0
				Q16622.TH2	77	0
				Q16622.TH3	77	0
Unbiased HAST (UHST) <sup>1</sup>	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADN4680E	Q16622.UH1	77	0
				Q16622.UH2	77	0
				Q16622.UH3	77	0

<sup>1</sup> These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

**Table 3: 0.35µm DMOS at TSMC Fab-10 Fab Qualification Test Results**

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, M1015	125°C, 48 Hours	ADP1612	Q8162.206	110	0
				Q8162.207	154	0
				Q8162.208	72	0
				Q8162.214	129	0
				Q8162.215	45	0
			Q8162.216	165	0	
			ADP1614	Q10687.EL1a	250	0
				Q10687.EL1b	250	0
				Q10687.EL1c	250	0
				Q10687.EL1d	250	0
				Q10687.EL2a	250	0
				Q10687.EL2b	250	0
				Q10687.EL2c	250	0
				Q10687.EL2d	250	0
				Q10687.EL3a	250	0
			Q10687.EL3c	250	0	
			Q10687.EL3d	250	0	
			ADP3624	Q8162.200	120	0
				Q8162.201	250	0
				Q8162.202	249	0
				Q8162.203	52	0
			ADP8140	Q9631.EL1a	290	0
				Q9631.EL1b	290	0
				Q9631.EL1c	290	0
				Q9631.EL1d	290	0
				Q9631.EL2a	290	0
				Q9631.EL2c	290	0
				Q9631.EL2d	290	0
Q9631.EL3a	290	0				
Q9631.EL3b	290	0				
Q9631.EL3d	290	0				
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=115°C, Biased, 1000 Hours	ADN4680E	Q16622.HO1	75*	0
				Q16622.HO2	77*	0
				Q16622.HO3	77*	0
	ADN4692E	125°C, Tj<135°C, Biased, 1000 Hours	Q9375.HO1	77	0	
			Q9375.HO2	77	0	
			Q9375.HO3	77	0	
ADN4697E	125°C, Tj<135°C, Biased, 1000 Hours	Q9375.HO1	77	0		
		Q9375.HO2	77	0		
		Q9375.HO3	77	0		
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADN4680E	Q16622.HS1	50	0
				Q16622.HS2	50	0
				Q16622.HS3	50	0
Temperature Humidity Bias (THB) <sup>1</sup>	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADN4680E	Q16622.TH1	77	0
				Q16622.TH2	77	0
				Q16622.TH3	77	0

<sup>1</sup> These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

\* Completed to 500 hours, 1000 hours due to complete 30<sup>th</sup> September 2021

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on [Analog Devices' web site](#).

## ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 5. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on [Analog Devices' web site](#)).

**Table 5: ADN4680E ESD Test Results**

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	48-LFCSP	JS-002	1Ω, Cpkg	±1250V	NA	C3
HBM	48-LFCSP	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±8000V	NA	3B

**Table 6: ADN4680E IEC 61004-2 ESD Test Results**

IEC 61000-4-2 ESD Test	Results
Bus pins IEC Air to GND	±10kV
Bus pins IEC Contact to GND	±8kV

## Latch-Up Test Results

Three samples of the ADN4680E were latch-up tested at  $T_A=25^{\circ}\text{C}$  per JEDEC Standard JESD78, Class I. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+200mA	-200mA	+3.6V

## Approvals

Reliability Engineer: Joan OConnell

## Appendix

### Post Temperature Cycling Wire Bond Pull Test Results:

PCL-3196 ADN4680E Q16622.WP1										
Unit	1		2		3		4		5	
Ball	Pull	Mode	Pull	Mode	Pull	Mode	Pull	Mode	Pull	Mode
1	6.85	C	7.50	C	6.76	C	6.61	C	6.30	C
2	6.85	C	7.40	C	6.62	C	6.56	C	6.91	C
3	7.01	C	7.34	C	6.66	C	6.44	C	6.18	C
4	7.46	C	7.27	C	4.97	C	6.41	C	6.34	C
5	6.34	C	7.49	C	6.85	C	6.66	C	6.56	C
6	6.66	C	6.70	C	6.40	C	5.94	C	7.02	C
7	6.80	C	7.49	C	6.54	C	6.24	C	6.18	C
8	7.09	C	7.00	C	6.97	C	6.85	C	6.11	C
MIN	6.34		6.70		4.97		5.94		6.11	
MAX	7.46		7.50		6.97		6.85		7.02	
AVE	6.88		7.27		6.47		6.46		6.45	
STDEV	0.33		0.29		0.63		0.28		0.35	

PCL-3197 ADN4680E Q16622.WP2_AP46579.10										
Unit	1		2		3		4		5	
Ball	Pull	Mode	Pull	Mode	Pull	Mode	Pull	Mode	Pull	Mode
1	3.27	C	4.61	C	1.21	A	4.06	C	5.30	C
2	3.10	C	4.06	C	4.41	C	4.26	C	6.87	C
3	4.70	C	3.99	C	3.81	C	5.00	C	7.02	C
4	3.28	C	5.53	C	5.94	C	4.55	C	6.50	C
5	2.92	C	4.74	C	4.36	C	5.10	C	6.18	C
6	3.72	C	3.81	C	3.48	C	3.04	C	5.96	C
7	4.61	C	3.94	C	3.57	C	4.61	C	5.05	C
8	3.03	C	3.83	C	3.26	C	3.59	C	6.20	C
MIN	2.92		3.81		1.21		3.04		5.05	
MAX	4.70		5.53		5.94		5.10		7.02	
AVE	3.58		4.31		3.76		4.28		6.14	
STDEV	0.71		0.60		1.33		0.70		0.69	

PCL-3198 ADN4680E Q16622.WP3_AP46580.10										
Unit	1		2		3		4		5	
Ball	Pull	Mode	Pull	Mode	Pull	Mode	Pull	Mode	Pull	Mode
1	7.10	C	4.57	C	5.39	C	4.60	C	4.88	C
2	6.68	C	5.58	C	6.54	C	5.76	C	5.20	C
3	6.38	C	5.88	C	6.27	C	6.27	C	4.95	C
4	5.90	C	5.74	C	6.54	C	5.19	C	5.68	C
5	6.27	C	5.49	C	5.81	C	6.35	C	5.53	C

6	7.85	C	5.58	C	5.95	C	6.58	C	5.07	C
7	6.71	C	6.13	C	5.70	C	7.17	C	5.92	C
8	6.47	C	5.33	C	4.82	C	3.65	C	4.09	C
MIN	5.90		4.57		4.82		3.65		4.09	
MAX	7.85		6.13		6.54		7.17		5.92	
AVE	6.67		5.54		5.88		5.70		5.17	
STDEV	0.59		0.46		0.59		1.16		0.57	