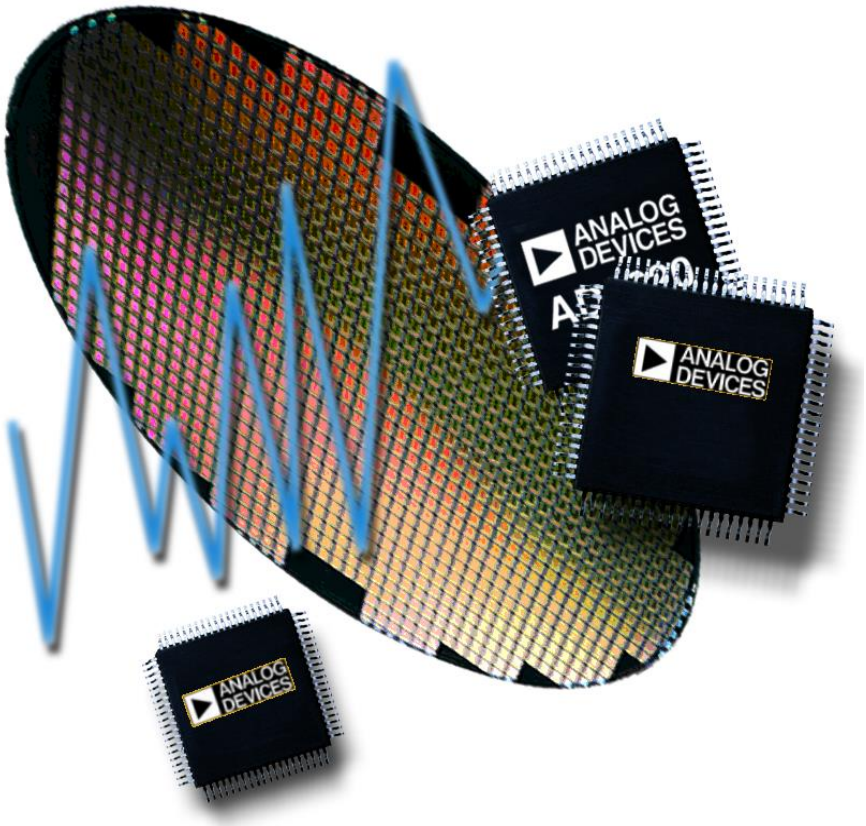

Reliability Report

Report Title: AD5770R New Product Qualification

Report Number: 13080

Revision: A

Date: 10 January 2019

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the AD5770R product in a 49-WLCSP and in a 48-LFCSP packages. The product is fabricated using the 0.18um CMOS technology at TSMC Fab 8 and then to be processed at ADLK backend for the Thin Film Precision Resistors (TFR). The LFCSP version is assembled in ASE-Korea with copper redistribution layer at ChipBond foundry.

The AD5770R is a 6-channel, 14-it resolution, low noise, programmable current output digital-to-analog (DAC) converter for photonics control applications. This chip incorporates a 1.25V on–chip voltage reference, a 2.5-kiloohm precision resistor for reference current generation, die temperature, output monitoring functions, fault alarm, and reset functions.

Table 1: AD5770R Product Characteristics

Die/Fab

Die Id	TMJL95/D
Die Size (mm)	4.00 x 4.00
Wafer Fabrication Site	TSMC Fab 8
Wafer Fabrication Process	0.18µm CMOS
Approximate Transistor Count	614918
Passivation Layer	undoped oxide/ Oxide & Nitride
Bond Pad Metal Composition	AlCu

Package/Assembly

Package	48-LFCSP
Body Size (mm)	6.00 x 6.00 x 0.75
Assembly Location	ASE (AEK)
Molding Compound	Sumitomo G700LYT
Wire Type	MKE PC Pd/Cu
Wire Diameter (mils)	0.80
Die Attach	Hitachi EN-4900GC
Lead Frame Material	Copper
Lead Finish	Matte Sn
RDL Layers	1
RDL Composition	TiW(0.32)/Cu(0.2)/Cu(21)/Ni(2)/Au(0.5)
RDL Repassivation	Polyimide
RDL Foundry	Chipbond 4 (CB4)
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Table 2: AD5770R Product Characteristics

Die/Fab

Die Id	TMJL95/D
Die Size (mm)	4.00 x 4.00
Wafer Fabrication Site	TSMC Fab 8
Wafer Fabrication Process	0.18µm CMOS
Approximate Transistor Count	614918
Passivation Layer	undoped oxide/ Oxide & Nitride
Bond Pad Metal Composition	AlCu

Package/Assembly

Package	49-WLCSP
Bump Pitch (mm)	0.50
Bump Diameter (mm)	0.30
Bumping Foundry	SCS
RDL Layers	1
RDL Composition	Ti(0.1)/Cu(0.2)/Cu(3)
RDL Repassivation	Polyimide
Under Bump Metallization	Ti(0.1)/Cu(0.2)/Cu(8.6)
Bumping Process	Ball drop/repassivation
Bump Composition	95.5Sn_4.0Ag_0.5Cu

Description / Results of Tests Performed

Tables 3 through 5 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1 through 2. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 3: LFCSP at ASE (AEK) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD5770R	Q13080.HS1	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD5766	Q11868.HA1	45	0
				Q11868.HA2	45	0
				Q11868.HA3	45	0
			AD5770R	Q13080.HA1	45	0
				Q13080.HA2	45	0
				Q13080.HA4	45	0
				Q13080.HA5	45	0
			AD9695	Q11437.HA1	32	0
				Q11437.HA2	32	0
			ADF7250	Q12261.3	77	0
			ADRF6650	Q12173.11R1	45	0
			ADRF6821	Q12175.13	45	0
				Q12175.5	45	0
Solder Heat Resistance (SHR) [1]	J-STD-020	MSL-3	AD5770R	Q13080.SH1	16	0
				Q13080.SH2	16	0
				Q13080.SH3	16	0
Temperature Cycling (TC) [1]	JESD22-A104	-65°C/+150°C, 1,000 Cycles	AD9512	Q12863.TC1	77	0
				Q12863.TC2	77	0
				Q12863.TC3	77	0
		-65°C/+150°C, 500 Cycles	AD5770R	Q13080.TC1	45	0
				Q13080.TC2	45	0
				Q13080.TC3	45	0
			AD9545	Q11804.10	45	0
				Q11804.11	45	0
				Q11804.9	45	0
			ADRF6821	Q12175.11	45	0
Temperature Humidity Bias (THB) [1]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	AD9545	Q11804.6	45	0
				Q11804.7	45	0
				Q11804.8	45	0
Unbiased HAST (UHST) [1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	AD5770R	Q13080.UH1	45	0
				Q13080.UH2	45	0
				Q13080.UH3	45	0
			ADF7250	Q12261.4	77	0
			ADRF6650	Q12173.14	30	0
				Q12173.3	30	0

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
				Q12173.8	45	0
			ADRF6795	Q12828.1	45	0
			ADuCM4150	QL12865UHS01	45	0
				QL12865UHS02	45	0
				QL12865UHS03	45	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 4: WLCSP at STATS (STA) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD80360	Q11029.1	32	0
			ADAS1020	Q12356.1	32	0
			ADP5025	Q9000.1	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST)	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD80360	Q11029.14	32	0
				Q11029.15	32	0
				Q11029.16	32	0
Temperature Cycling (TC)	JESD22-A104	-40°C/+125°C, 1 Cycles/Hour, 1,000 Cycles	AD5766	Q11868.TC2	45	0
				Q11868.TC3	45	0
				Q11868.TC4	45	0
			AD80360	Q11029.10	32	0
				Q11029.11	32	0
				Q11029.12	32	0
			ADAS1020	Q12356.5	32	0
				Q12356.6	32	0
				Q12356.7	32	0
			ADP5025	Q9000.2	45	0
				Q9000.3	45	0
				Q9000.4	45	0
Unbiased HAST (UHST)	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	AD5766	Q11868.UH1	45	0
				Q11868.UH2	45	0
				Q11868.UH3	45	0
			ADP5025	Q9000.5	45	0
				Q9000.6	45	0
				Q9000.7	45	0
Unbiased HAST (UHST) [1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	AD81005	Q11794.UB1	77	0
				Q11794.UB2	77	0
				Q11794.UB3	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 5: 0.18µm CMOS at TSMC Fab-8B Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, M1015	125°C, 48 Hours	AD7616	Q11187.22	170	0
				Q11187.24	170	0
				Q11187.25	170	0
				Q11187.27	170	0
			AD5235	Q8891.EL1a	230	0
				Q8891.EL2a	230	0
				Q8891.EL3a	230	0
			AD5700-1A	Q9206.19	241	0
				Q9206.20	239	0
				Q9206.21	421	0
			AD5144	Q10159.EL5	250	0
				Q10159.EL6	250	0
				Q10159.EL7	250	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	AD4000	Q11452.3	45	0
				Q11452.4	45	0
				Q11452.5	45	0
			AD4003	Q11452.12	77	0
				Q11452.13	77	0
				Q11452.14	77	0
			AD5770R	Q13080.HO1	45	0
				Q13080.HO2	45	0
				Q13080.HO3	45	0
				Q13080.HO4	45	0
			ADF7030	Q11148.1	77	0
				Q11148.2	77	0
				Q11148.3	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD4003	Q11452.24	77	0
			AD5592R	Q11193.HS1	77	0
			AD5770R	Q13080.HS1	45	0
			ADF7030	Q11148.14	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD4003	Q11452.15	77	0
				Q11452.20	77	0
				Q11452.21	77	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [2]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	AD4000	Q11452.1	45	0
			AD4003	Q11452.37	77	0
				Q11452.38	77	0
				Q11452.41	77	0
			AD5592R	Q10946.HA1	45	0
				Q10946.HA2	45	0
				Q10946.HA3	45	0
			AD5770R	Q13080.HA1	45	0
				Q13080.HA2	45	0
				Q13080.HA3	45	0
			AD7616	Q11187.10	32	0
				Q11187.14	32	0

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
			ADF7030	Q11148.11	77	0
				Q11148.7	77	0
				Q11148.8	77	0
			ADF7030-1	Q11148.29	77	0
				Q11148.30	77	0
				Q11148.31	77	0
Temperature Humidity Bias (THB) [2]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	AD5592R	Q11608.TH1	77	0
				Q11608.TH2	77	0
				Q11608.TH3	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 7. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 6: AD5770R ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	49-WLCSP	JESD22-C101E	1Ω, Cpkg	±1500V	NA	C3
HBM	49-WLCSP	ESDA/JEDEC JS-001-2011	1.5kΩ, 100pF	±1000V	±1500V	1C

Latch-Up Test Results

Three samples of the AD5770R were latch-up tested at T_A=25°C per JEDEC Standard JESD78, Class I. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+200mA	-200mA	+7.65V/+8.25V

Approvals

Reliability Engineer: Ryan Quintin

Additional Information

Data sheets and other additional information are available on Analog Devices' web site.