ANALOG DEVICES

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LTM4622A Datasheet Comparison

LTM4622A Electrical Characteristic

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel at T_A = 25°C, V_{IN1} = V_{IN2} = 12V, unless otherwise noted per the typical application shown in Figure 27.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: per Channel							
V_{IN1}	Input DC Voltage Range		●	3.6		20	V
V_{IN2}	Input DC Voltage Range	3.6V < V_{IN1} < 20V	●	1.5		20	V
$V_{OUT(RANGE)}$	Output Voltage Range	V_{IN1} = V_{IN2} = 3.6V to 20V	●	1.5		12	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic, R_{FB} = 40.2k, MODE = $INTV_{CC}$, V_{IN1} = V_{IN2} = 3.6V to 20V, I_{OUT} = 0A to 2A	●	1.477	1.50	1.523	V
V_{RUN}	RUN Pin On Threshold	RUN Threshold Rising RUN Threshold Falling		1.20 0.97	1.27 1.00	1.35 1.03	V V
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V, MODE = GND V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$ Shutdown, RUN1 = RUN2 = 0			7 500 45		mA µA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V, I_{OUT} = 2A			0.32		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V (Note 3)	●	0		2	A
$\Delta V_{OUT(Line)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN1} = V_{IN2} = 3.6V to 20V, I_{OUT} = 0A	●		0.01	0.1	%/V
$\Delta V_{OUT(Load)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 2A	●		0.2	1.0	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V			5		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V			30		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, No Load, TRACK/SS = 0.01µF, V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V			~~1.25~~ 5.5		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic, V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V			100		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic, V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V			20		µs
I_{OUTPK}	Output Current Limit	V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V		3	4		A
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.592	0.60	0.608	V
I_{FB}	Current at FB Pin	(Note 4)				±30	nA
R_{FBHI}	Resistor Between V_{OUT} and FB Pins			60.00	60.40	60.80	kΩ
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			~~1.25~~ 1.2		µA
t_{SS}	Internal Soft-Start Time	10% to 90% Rise Time (Note 4)			400	700	µs
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			20		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			45		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive			 –8 8	 –14 14	 % %
R_{PGOOD}	PGOOD Pull-Down Resistance	1mA Load			20		Ω
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN1} = V_{IN2} = 3.6V to 20V		3.1	3.3	3.5	V

LTM4622A Pin Functions

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (Pins C1, C2, B5, D5): Power Ground Pins for Both Input and Output Returns.

$INTV_{CC}$ (Pin C3): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. This pin is internally decoupled to GND with a 2.2µF low ESR ceramic capacitor. No additional external decoupling capacitor needed.

FREQ (Pin C4): Frequency is set internally to 1MHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

SYNC/MODE (Pin C5): Mode Select and External Synchronization Input. Tie this pin to ground to force continuous synchronous operation at all output loads. Floating this pin or tying it to $INTV_{CC}$ enables high efficiency Burst Mode operation at light loads. Drive this pin with a clock to synchronize the LTM4622A switching frequency. An internal phase-locked loop will force the bottom power NMOS's turn on signal to be synchronized with the rising edge of the clock signal. When this pin is driven with a clock, forced continuous mode is automatically selected.

V_{OUT1} (Pins D1, E1), V_{OUT2} (Pins A1, B1): Power Output Pins of Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

RUN1 (Pin D2), RUN2 (Pin B2): Run Control Input of Each Switching Mode Regulator Channel. Enables chip operation by tying RUN above 1.27V. Tying this pin below 1V shuts down the specific regulator channel. Do not float this pin.

V_{IN1} (Pins D3, E2), V_{IN2} (Pins A2, B3): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between BOTH V_{IN1} and V_{IN2} pins and GND pins. Please note the module internal control circuity is running off V_{IN1}. Channel 2 will not work without a voltage higher that 3.6V presents at V_{IN1}.

PGOOD1 (Pin D4), PGOOD2 (Pin B4): Output Power Good with Open-Drain Logic of Each Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±8% (typical) of the internal 0.6V reference.

TRACK/SS1 (Pin E3), TRACK/SS2 (Pin A3): Output Tracking and Soft-Start Pin of Each Switching Mode Regulator Channel. It allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal ~~1.4µA~~ 1.2uA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function. A default internal soft-start ramp forces a minimum soft-start time of 400µs.

FB1 (Pin E4), FB2 (Pin A4): The Negative Input of the Error Amplifier for Each Switching Mode Regulator Channel. Internally, this pin is connected to V_{OUT} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase® operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

COMP1 (Pin E5), COMP2 (Pin A5): Current Control Threshold and Error Amplifier Compensation Point of Each Switching Mode Regulator Channel. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V. Tie the COMP pins together for parallel operation. The device is internal compensated. Do not drive this pin.

LTM4622A Applications Information

APPLICATIONS INFORMATION

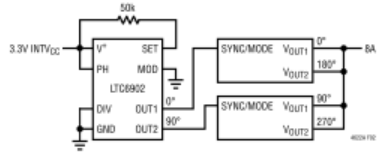

Figure 2. Example of Clock Phasing for 4-Phase Operation with LTC6902

good current sharing. This will balance the thermals on the design. Please tie RUN, TRACK/SS, FB and COMP pin of each paralleling channel together. Figure 31 shows an example of parallel operation and pin connection.

INPUT RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 3 shows this graph.

Soft-Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal ~~1.4µA~~ 1.2uA current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{\sim\sim 1.4\mu A\sim\sim\ 1.2uA}$$

where C_{SS} is the capacitance on the TRACK/SS pin. Current foldback and force continuous mode are disabled during the soft-start process.

The LTM4622A has internal 400µs soft-start time when TRACK/SS leave floating.

Output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 4 and Figure 5 show an example waveform and schematic of a Ratiometric

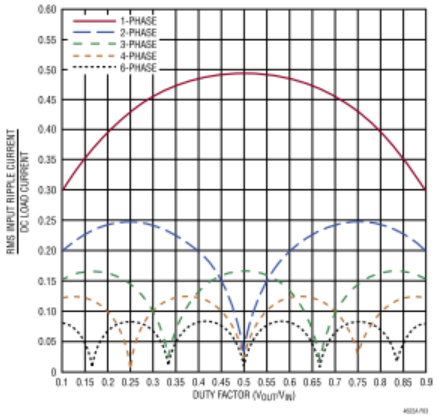

Figure 3. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

APPLICATIONS INFORMATION

tracking where the slave regulator's output slew rate is proportional to the master's.

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave

Figure 4. Output Ratiometric Tracking Waveform

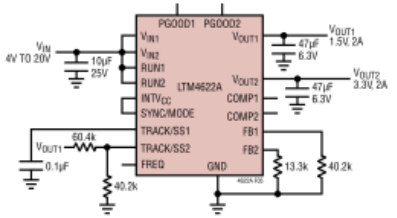

Figure 5. Example Schematic of Ratiometric Output Voltage Tracking

output voltage and the master output voltage should satisfy the following equation during the start-up.

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} =$$

$$V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 5.

Following the upper equation, the master's output slew rate (MR) and the slave's output slew rate (SR) in Volts/Time is determined by:

$$\frac{MR}{SR} = \frac{\dfrac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\dfrac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

For example, $V_{OUT(MA)}$ = 1.5V, MR = 1.5V/ms and $V_{OUT(SL)}$ = 3.3V, SR = 3.3V/ms. From the equation, we could solve out that $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 40.2k is a good combination for the Ratiometric tracking.

The TRACK pins will have the ~~1.5µA~~ 1.2uA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The Coincident output tracking can be recognized as a special Ratiometric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), as waveform shown in Figure 6.

From the equation, we could easily find out that, in the coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider.

Figure 6. Output Coincident Tracking Waveform