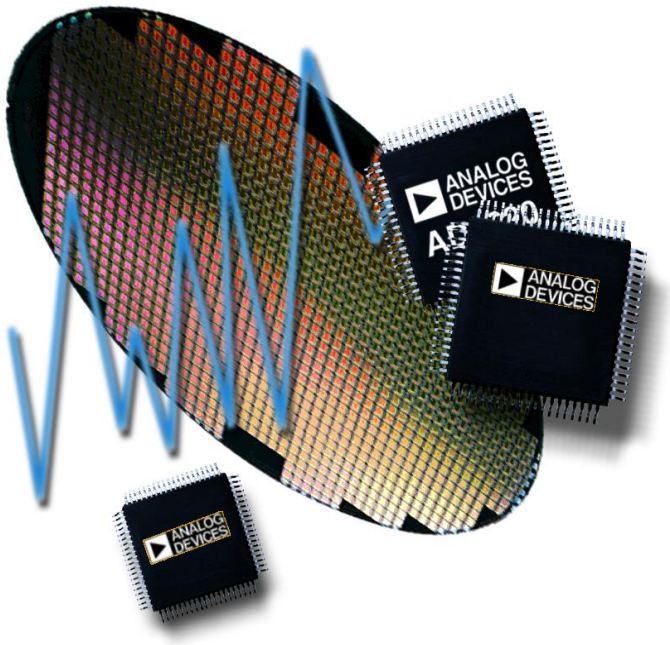

Reliability Report

Report Title: LTC3313 Assembly Process Change Automotive Grade 0 Qualification

Report Number: 21134

Revision: A

Date: 25 April 2024

Summary

This report documents the successful completion of the automotive reliability qualification requirements for the release of the LTC3313 product in a 18-LGA package with a 200um die thickness. The LTC3313 is a very small, low noise, monolithic step-down DC/DC converter capable of providing up to 12.5A of output current from a 2.25V to 5.5V input supply.

AECQ100 Qualification Test Methods and Summary

AEC Test Group	AEC Stress Test Name	Abbreviation	AEC Test #	Reference
Group A ACCELERATED ENVIRONMENT STRESS TESTS	Preconditioning	PC	A1	Table 2 and Table 4
	Temperature Humidity Bias or Biased-HAST	THB or HAST	A2	
	Autoclave or Unbiased HAST or Temperature Humidity (without Bias)	AC, UHST, or TH	A3	
	Temperature Cycle	TC	A4	
	Power Temperature Cycling	PTC	A5	
	High Temperature Storage Life	HTSL	A6	
Group B ACCELERATED LIFETIME SIMULATION TESTS	High Temperature Operating Life	HTOL	B1	Table 2 and Table 4
	Early Life Failure Rate	ELFR	B2	
	NVM Endurance, Data Retention, and Operational Life	EDR	B3	
Group C PACKAGE ASSEMBLY INTEGRITY TESTS	Wire Bond Shear	WBS	C1	C1, C2 are only applicable for wire bond package. C5 is only applicable for BGA package. C3, C4 and C6 are qualified and controlled with inline monitors and may be viewed on site at Analog Devices.
	Wire Bond Pull Strength	WBP	C2	
	Solderability	SD	C3	
	Physical Dimensions	PD	C4	
	Solder Ball Shear	SBS	C5	
	Lead Integrity	LI	C6	
Group D DIE FABRICATION RELIABILITY TESTS	Electromigration	EM	D1	Die Fabrication Reliability data may be viewed on-site at Analog Devices.
	Time Dependent Dielectric Breakdown	TDDB	D2	
	Hot Carrier Injection	HCI	D3	
	Negative Bias Temperature Instability	BTI	D4	
	Stress Migration	SM	D5	
Group E ELECTRICAL VERIFICATION TESTS	Pre- and Post-Stress Electrical Test	TEST	E1	Table 5 and Table 6
	Electrostatic Discharge Human Body Model	HBM	E2	
	Electrostatic Discharge Charged Device Model	CDM	E3	
	Latch-Up	LU	E4	
	Electrical Distributions	ED	E5	• For Tests E5, E6 and E7, ADI New Product Yield Analysis Testing Guidelines meet AEC Q100 requirements. • Results for Tests E7-E11 are available as applicable on a case by case basis. • Test E12 results may be viewed on-site at Analog Devices
	Fault Grading	FG	E6	
	Characterization	CHAR	E7	
	Electromagnetic Compatibility	EMC	E9	
	Short Circuit Characterization	SC	E10	
	Soft Error Rate	SER	E11	
	Lead (Pb) Free	LF	E12	
Group F DEFECT SCREENING TESTS	Process Average Test	PAT	F1	ADI New Product Yield Analysis Testing Guidelines meet AECQ100 Requirements.
	Statistical Bin/Yield Analysis	SBA	F2	
Group G CAVITY PACKAGE INTEGRITY TESTS	Mechanical Shock	MS	G1	<Applicable only for Cavity Packages>
	Variable Frequency Vibration	VFV	G2	
	Constant Acceleration	CA	G3	
	Gross/Fine Leak	GFL	G4	
	Package Drop	DROP	G5	
	Lid Torque	LT	G6	
	Die Shear	DS	G7	
	Internal Water Vapor	IWV	G8	

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- 0.25um DMOS

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data		
Generic/Root Part #	LTC3313	LTC3310S	LTC3311	LTC3309
Die Id	LTC3313	LTC3310	LTC3311	LTC3309
Die Size (mm)	2.51 x 2.41	1.65 x 2.41	1.65 x 2.41	1.68 x 1.68
Wafer Fabrication Site	TSMC	TSMC	TSMC	TSMC
Wafer Fabrication Process	0.25um DMOS	0.25um DMOS	0.25um DMOS	0.25um DMOS
Die Substrate	Si	Si	Si	Si
Metallization / # Layers	AlCu/5	AlCu/5	AlCu/5	AlCu/5
Polyimide	No	No	No	No
Passivation	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN

Die/Fab Test Results

Table 2: Die/Fab Test Results - 0.25µm DMOS at TSMC

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
Early Life Failure Rate (ELFR)	B2	AEC Q100-008	Ta=150°C, Biased, 48 Hours	LTC3310S	971845.1	0/800	RH
					971846.1	0/800	RH
					971847.1	0/800	RH
High Temperature Operating Life (HTOL)	B1	JESD22-A108	Ta=150C, Biased, 1,000 Hours	LTC3311	Q17525.1HTOL	0/77	RCH
				LTC3313	Q17829.1HO	0/77	RCH
					Q21134.1.HO1[3]	0/77	RCH
				LTC3310S	971845.1	0/77	RCH
					971846.1	0/77	RCH
					971847.1	0/77	RCH
				LTC3309	Z41896.1	0/77	RCH
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 2,000 Hours	LTC3310S	EO9302F.HTS	0/45	RH
				LTC3311	Q16488.1HTS	0/45	RH
				LTC3313	Q18223.1HTS	0/45	RH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	LTC3310S	EO9302K.BHAST	0/77	RH
					EO9303K.BHAST	0/77	RH
					EO9304K.BHAST	0/77	RH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[2]	A2	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	LTC3311	Q16488.1BHAST	0/77	RH
				LTC3313	Q18223.1BHAST	0/77	RH

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.
[2] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.
[3] Stress test with 200µm die.

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - LGA at ASE

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data			
Generic/Root Part #	LTC3313	LTC3311	LT8638S	LT8650SPA	LT8650S
Package	18-LGA	18-LGA	28-LGA	32-LGA	32-LGA
Body Size (mm)	3.00 x 3.00 x 0.95	3.00 x 3.00 x 0.94	5.00 x 4.00 x 0.94	6.00 x 4.00 x 0.94	6.00 x 4.00 x 0.94
Assembly Location	ASE	ASE	ASE	ASE	ASE
MSL/Peak Reflow Temperature(°C)	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C
Mold Compound	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E
Substrate Material	BT Resin	BT Resin	BT Resin	BT Resin	BT Resin
Lead Finish	Au	Au	Au	Au	Au

Package/Assembly Test Results

Table 4: Package/Assembly Test Results - LGA at ASE

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 2,000 Hours	LT8638S	Q20120.2HTS[2]	0/45	RH
				LTC3311	Q16488.1HTS	0/45	RH
				LTC3313	Q18223.1HTS	0/45	RH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	LT8638S	Q20120.1HAST[2]	0/77	RH
				LT8650S	Q20616.2HAST[2]	0/77	RH
					Q20616.3HAST[2]	0/77	RH
					Q20616.4HAST[2]	0/77	RH
				LT8650SPA	Q20156.1HAST	0/77	RH
					Q20156.2HAST	0/77	RH
					Q20156.3HAST	0/77	RH
				LTC3311	Q16488.1BHAST	0/77	RH
				LTC3313	Q18223.1BHAST	0/77	RH
Solder Heat Resistance (SHR)	A1	J-STD-020	MSL-3	LTC3313	Q21134.1.SHR[2]	0/77	R
Temperature Cycling (TC)[1]	A4	JESD22-A104	-65°C/+150°C, 2,000 Cycles	LTC3313	Q21134.2.TC1[2]	0/77	RH
					Q18223.1TC	0/77	RH
				LTC3311	Q16488.1TC	0/77	RH
				LT8638S	Q20120.1TC[2]	0/77	RH
					Q20120.3TC[2]	0/77	RH
				LT8650S	Q20616.1TC[2]	0/77	RH
					Q20616.3TC[2]	0/77	RH
					Q20616.4TC[2]	0/77	RH
Unbiased HAST (UHST)[1]	A3	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	LT8650S	Q20616.1UHAST[2]	0/77	R
					Q20616.2UHAST[2]	0/77	R
					Q20616.3UHAST[2]	0/77	R
					Q20616.4UHAST_A[2]	0/77	R
				LT8650SPA	Q20156.1UHAST	0/77	R
					Q20156.2UHAST	0/77	R
					Q20156.3UHAST	0/77	R

					Q20156.4UHAST	0/77	R
				LTC3311	Q16488.1UHAST	0/77	R
				LTC3313	Q18223.1UHAST	0/77	R

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.
[2] Stress test with 200µm die.

ESD and Latch-Up Test Results

Table 5: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class	eTest Temp
FICDM	LTC3313	18-LGA	JS-002	1Ω, Cpkg	±1250V	C3	RH
HBM	LTC3313	18-LGA	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	3A	RH

Table 6: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class	eTest Temp
JESD78	LTC3313[1]	+200mA, -200mA	+8.25V	150°C	II	RH

[1] Stress test with 200µm die.

Approvals

Reliability Engineer: Kristen Perron