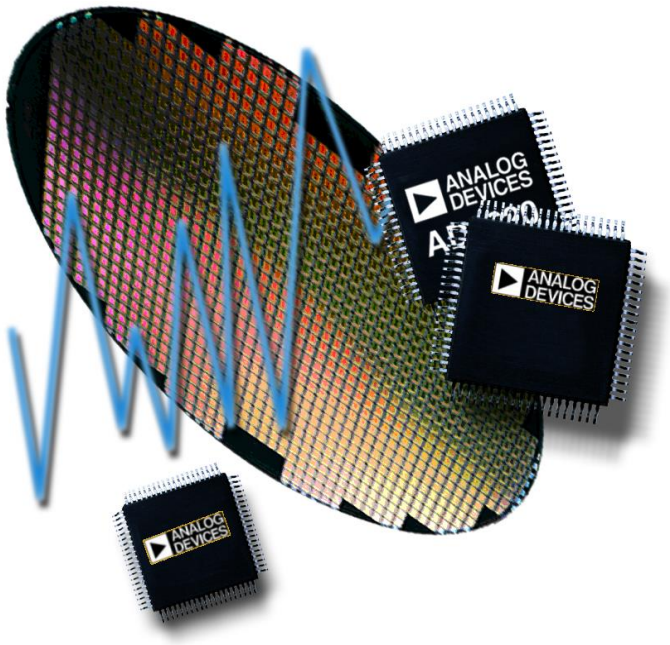

Reliability Report

Report Title: LT8625S Assembly Process Change Qualification

Report Number: 21474

Revision: A

Date: 18 March 2024

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the LT8625S product in a 20-LGA package with die thickness change from 450um to 200um, Cu pillar size of 85um, and SMT paste change from SnSb5 to SAC305. The LT8625S is a synchronous step-down regulator that features third-generation Silent Switcher technology which is uniquely designed to combine an ultralow noise reference with Silent Switcher architecture in order to achieve both high efficiency and excellent wideband noise performance.

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- 0.35µm DMOS

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data								
Generic/Root Part #	LT8625S	LT8625SP	LT8638S	LT8640S	LT8642S	LT8648S	LT8686S	LT8608	LT8650S	LT8650SP
Die Id	8625	8625	8638S	8640S	8642	8648	8686	8608	8650	8650
Die Size (mm)	1.77 x 1.57	1.57 x 1.77	2.59 x 4.02	1.65 x 2.82	1.67 x 2.70	6.20 x 2.70	3.20 x 1.75	1.13 x 1.43	1.75 x 3.88	1.75 x 3.88
Wafer Fabrication Site	E_VANG0108	E_VANG0108	E_VANG0108	E_VANG0108	E_VANG0108	E_VANG0108	E_VANG0108	E_VANG0108	E_VANG0108	E_VANG0108
Wafer Fabrication Process	0.35um DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS	0.35µm DMOS
Die Substrate	Si	Si	Si	Si	Si	Si	Si	Si	Si	Si
Metallization / # Layers	AlCu/2	AlCu/2	AlCu/3	AlCu/4	AlCu/2	AlCu/3	AlCu/3	AlSi/2	AlCu/3	AlCu/3
Polyimide	NA	No	No	No	No	No	No	No	No	No
Passivation	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN

Die/Fab Test Results

Table 2: Die/Fab Test Results - 0.35µm DMOS at Vanguard-Taiwan

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Early Life Failure Rate (ELFR)	JESD22-A108	Ta=125°C, 48 Hours	LT8642S	Q18281.4ELF	0/800
Early Life Failure Rate (ELFR)	AEC Q100-008	Ta=150C, 48 Hours	LT8608	Q20743.10_AUTO	0/800
Early Life Failure Rate (ELFR)	AEC-Q100-008	Ta=150C, 48 Hours	LT8650SP	Q17503.1ELFR	0/800
High Temperature Operating Life (HTOL)	JESD22-A108	Ta=125°C, Biased, 1,000 Hours	LT8625S	Q17330.1	0/77
		Ta=150C, Biased, 1,000 Hours	LT8625SP	Q17335.1HTOL	0/77
		125°C<Tj<135°C, Biased, 1,000 Hours	LT8640S	Q20149.1HTOL	0/77
		150°C<Tj<175°C, Biased, 1,000 Hours	LT8650S	Q20616.3HTOL	0/77
		Ta=150C, Biased, 1,000 Hours	LT8638S	Q20120.4HTOL	0/77
			LT8648S	Q20710.2HTOL	0/77
			LT8686S	Q20395.1HTOL	0/77
			LT8686S	Q17405.1BHTOL	0/77
			LT8686S	Q17405.2HTOL	0/77
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 2,000 Hours	LT8650S	Q20616.3HTS	0/77
			LT8638S	Q20120.2HTS	0/45
			LT8648S	Q20710.2HTS	0/45
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	LT8650S	Q20616.2HAST	0/77
				Q20616.3HAST	0/77
		110C 85%RH 17.7 psia, Biased, P264	LT8638S	Q20120.4HAST	0/77
		130C 85%RH 33.3 psia, Biased, 96 Hours		Q20120.1HAST	0/77
				Q20120.3HAST	0/77
			LT8686S	Q20395.1HAST	0/77
		130C 85%RH 33.3 psia, Biased, P192	LT8648S	Q20710.1HAST	0/77
				Q20710.2HAST	0/77
Temperature Humidity Bias (THB)[1]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	LT8650S	Q20616.3THB	0/77

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - 20-LGA at ASE (AEK)

Product Characteristics	Product(s) to be qualified	Product(s) used for Substitution Data					
Generic/Root Part #	LT8625S	LT8638S	LT8648S	LT8686S	LT8645S	LT8650S	LT7170
Package	20-LGA	28-LGA	36-LGA	32-LGA	32-LGA	36-LGA	24-LGA
Body Size (mm)	4.00 x 3.00 x 0.95	5.00 x 4.00 x 0.94	7.00 x 4.00 x 0.94	5.00 x 5.00 x 0.95	6.00 x 4.00 x 0.94	6.00 x 4.00 x 0.94	4.00 x 3.00 x 0.95
Assembly Location	ASE (AEK)	ASE (AEK)	ASE (AEK)	ASE (AEK)	ASE (AEK)	ASE (AEK)	ASE (AEK)
MSL/Peak Reflow Temperature(°C)	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C
Mold Compound	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E	Sumitomo G311E
Leadframe Material	BT Resin	BT Resin	BT Resin	BT Resin	BT Resin	BT Resin	BT Resin
Lead Finish	Au	Au	Au	Au	Au	Au	Au
Bumping Foundry	Chipbond	Chipbond	Chipbond	Chipbond	Chipbond	Chipbond	Chipbond
Bumping Process	Electroplating/ Cu Pillar	Electroplating/ Cu Pillar	Electroplating/ Cu Pillar	Electroplating/ Cu Pillar	Electroplating/ Cu Pillar	Electroplating/ Cu Pillar	Electroplating/ Cu Pillar

Package/Assembly Test Results

Table 4.1: Package/Assembly Test Results - LGA at ASE (AEK)

Test Name	Spec	Conditions	Generic/ Root Part #	Lot #	Fail/SS
Solder Heat Resistance (SHR)	J-STD-020	MSL-3	LT8625S	Q21474.1.SHR_POR	0/77
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 2,000 Hours	LT8650S	Q20616.3HTS	0/77
			LT8638S	Q20120.2HTS	0/45
			LT8648S	Q20710.2HTS	0/45
Temperature Cycling (TC)[1]	JESD22-A104	-65°C/+150°C, 1,000 Cycles	LT7170	Q20863.1TC	0/77
				Q20863.2TC	0/77
			LT8625S	Q21474.1.TC_POR	0/77
		-65C/+150C, 2,000 Cycles	LT8650S	Q20616.1TC	0/77
				Q20616.2TC	0/77
				Q20616.3TC	0/77
			LT8638S	Q20120.1TC	0/77
				Q20120.2TC	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	LT8650S	Q20616.2HAST	0/77
				Q20616.3HAST	0/77
				Q20616.4HAST	0/77
			LT8638S	Q20120.1HAST	0/77
				Q20120.3HAST	0/77
			LT8686S	Q20395.1HAST	0/77
		130C 85%RH 33.3 psia, Biased, P192	LT8648S	Q20710.1HAST	0/77
				Q20710.2HAST	0/77
Temperature Humidity Bias (THB)[1]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	LT8650S	Q20616.3THB	0/77

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Table 4.2: Package/Assembly Test Results - LGA at ASE (AEK)

Test Name	Spec	Conditions	Generic/ Root Part #	Lot #	Fail/SS
Unbiased HAST (UHST)[1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	LT8645S	Q20778.1UHAST	0/77
				Q20778.2UHAST	0/77
			LT8650S	Q20616.1UHAST	0/77
				Q20616.2UHAST	0/77
		130C 85%RH 33.3 psia, 96 Hours	LT8686S	Q20395.1UHAST	0/77
		110C 85%RH 17.7 psia, P264	LT8638S	Q20120.1UHAST	0/77
				Q20120.2UHAST	0/77
				Q20120.3UHAST	0/77
				Q20120.4UHAST	0/77

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 5: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	LT8625S	20-LGA	JS-002	1Ω, Cpkg	±2000V	C7
HBM	LT8625S	20-LGA	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	3A

Table 6: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class
JESD78	LT8625S	+100mA, -100mA	+18V/+4V/+6V/+23V	125°C	II

Approvals

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