ADP1071-1/-2 Datasheet Changes from Rev B to Rev C

30th May 2024

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Summary of the Changes: ABSOLUTE MAXIMUM RATINGS

Rev.B

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VIN, EN	66 V
VDD2	42 V
VREG1	16 V
VREG2	6 V
GATE	−0.3 V to +16 V
RT, CS, SYNC, SS2, FB, COMP, OVP, MODE, SR	6.5 V
AGND1, AGND2	±0.3 V
Operating Temperature Range	−40°C to +125°C
Common-Mode Transients[1]	±50 kV/µs
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C
Electrostatic Discharge (ESD)	
Charged Device Model (CDM)	250 V
Human Body Model (HBM)	1 kV

Rev.C

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 5. Absolute Maximum Ratings

PARAMETER	RATING
VIN, EN	66V
VDD2	42V
VREG1	16V
VREG2	6V
GATE	−0.3V to +16V
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RT, SYNC, SS2, FB, COMP, OVP, MODE, SR	6.5V
AGND1, AGND2	±0.3V
Operating Temperature Range	−40°C to +125°C
Common-Mode Transients[1]	±50kV/µs
Junction Temperature	150°C
Peak Solder Reflow Temperature SnPb Assemblies (10sec to 30sec)	240°C
Peak Solder Reflow Temperature RoHS Compliant Assemblies (20sec to 40sec)	260°C

Summary of the Changes: Pin Function Descriptions, LGA

Rev.B

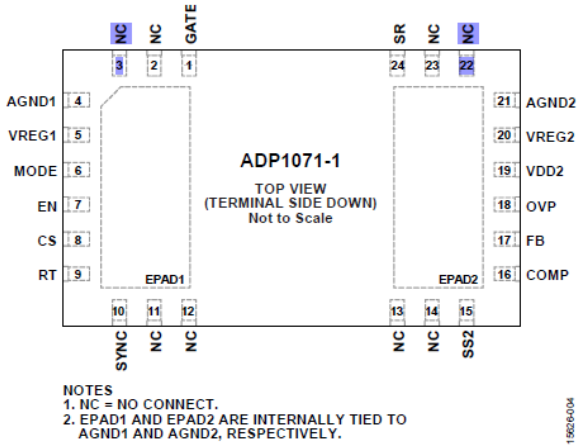

Figure 4. ADP1071-1 LGA Pin Configuration

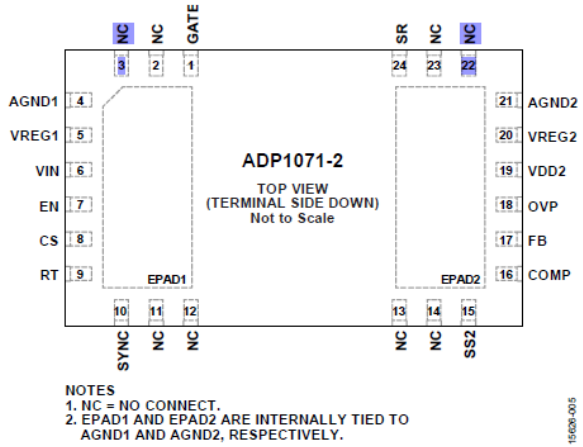

Figure 5. ADP1071-2 LGA Pin Configuration

Table 10. Pin Function Descriptions, LGA

Pin No.			
ADP1071-1	ADP1071-2	Mnemonic	Description
1	1	GATE	Driver Output for the Main Power MOSFET on the Primary Side. GATE is a multifunction pin. Connect a resistor from the GATE pin to AGND1 to set up the open loop soft start time.
2	2	NC	No Connect.
3	3	NC	No Connect.
4	4	AGND1	Ground for the Primary Side.
5	5	VREG1	8 V Regulated LDO Output for the MOSFET Driver. Connect 1 µF or greater from VREG1 to AGND1.

Rev.C

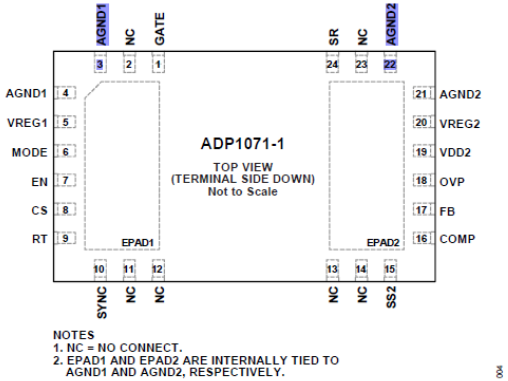

Figure 4. ADP1071-1 LGA Pin Configuration

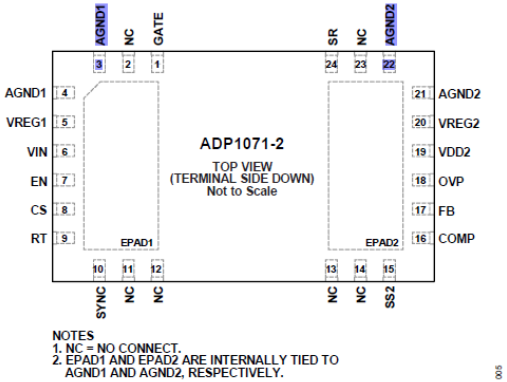

Figure 5. ADP1071-2 LGA Pin Configuration

Pin Function Descriptions, LGA

Table 10.Pin Description, LGA

PIN		Mnemonic	DESCRIPTION
ADP1071-1	ADP1071-2		
1	1	GATE	Driver Output for the Main Power MOSFET on the Primary Side. GATE is a multifunction pin. Connect a resistor from the GATE pin to AGND1 to set up the open loop soft start time.
2	2	NC	No Connect.
3, 4	3, 4	AGND1	Ground for the Primary Side.
5	5	V_{REG1}	8V Regulated LDO Output for the MOSFET Driver. Connect 1µF or greater from VREG1 to AGND1.

Summary of the Changes: Pin Function Descriptions, LGA

Rev.B

18	18	OVP	Output Overvoltage Protection. The OVP threshold is set at 1.36 V. Connect a resistive divider from the OVP pin to the output and AGND2.
19	19	VDD2	Input Supply on the Secondary Side. Connect VDD2 to the output voltage of the power supply for a self driven configuration. Connect a 4.7 µF capacitor from VDD2 to AGND2. The size of this capacitor can be reduced if the input voltage to VDD2 is guaranteed to be stable.
20	20	VREG2	5 V Regulated LDO Output for Internal Bias and Powering of the Drivers of the Synchronous Rectifiers. Do not use VREG2 as a reference or load. Connect a 1 µF capacitor from VREG2 to AGND2.
21	21	AGND2	Analog Ground on Secondary Side.
22	22	NC	No Connect.
23	23	NC	No Connect.

Rev.C

ADP1071-1	ADP1071-2		
			AGND2. The size of this capacitor can be reduced if the input voltage to V_{DD2} is guaranteed to be stable.
20	20	V_{REG2}	5V Regulated LDO Output for Internal Bias and Powering of the Drivers of the Synchronous Rectifiers. Do not use V_{REG2} as a reference or load. Connect a 1µF capacitor from V_{REG2} to AGND2.
21, 22	21, 22	AGND2	Analog Ground on Secondary Side.
23	23	NC	No Connect.

AHEAD OF WHAT'S POSSIBLE

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