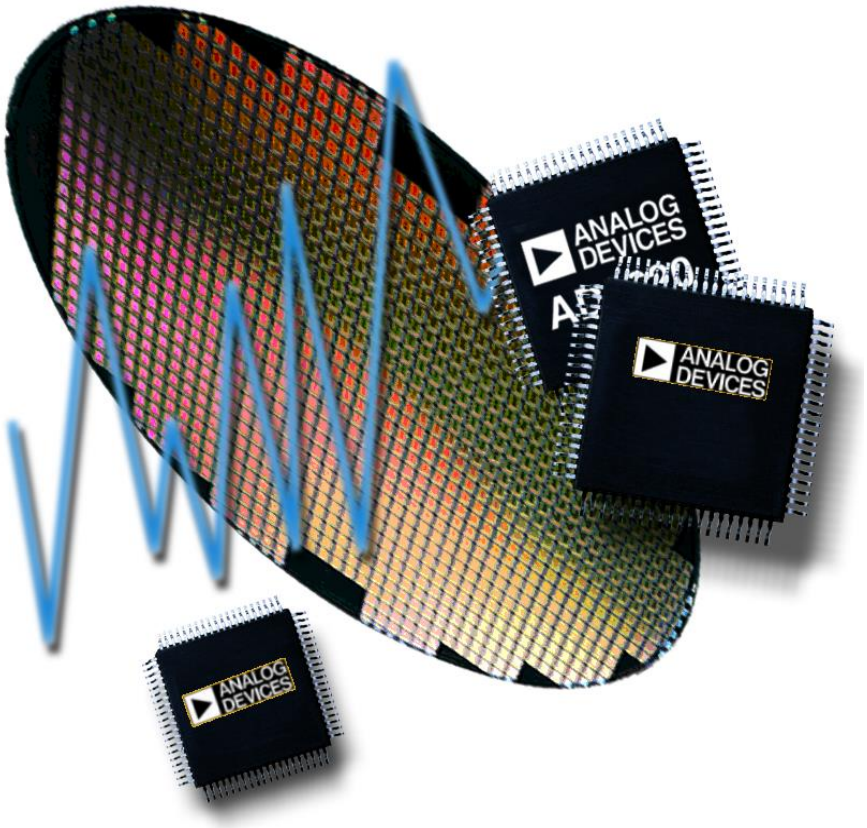

Reliability Report

Report Title: ADSP-2156x in BGA Automotive Grade 2 Cu Wire Qualification

Report Number: 17053

Revision: B

Date: 9 February 2023

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADSP-21566/21566W, ADSP-21567/21567W, ADSP-21569/21569W Rev 0.2 product in a 400-CSP_BGA package with Cu wire at SK3. The ADSP-2156x are the next generation SHARC DSP processor family.

This same ADSP-2156x Rev 0.2 family of products was previously released in a 400-CSP_BGA package with Au wire per qual 16972.

Table 1: ADSP-2156x Product Characteristics

Die/Fab

Die Id	TMKK81 A
Die Size (mm)	4.44 x 4.4
Wafer Fabrication Site	E_TSMC1512
Wafer Fabrication Process	CMOS
Approximate Transistor Count	20.0 million
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu(0.5%)

Package/Assembly

Package	400-CSP_BGA
Body Size (mm)	17.00 x 17.00 x 1.28
Assembly Location	STATS (SK3)
Solder Ball Diameter (mm)	0.45
Solder Ball Pitch (mm)	0.80
Molding Compound	Kyocera KE G2250HT-TU
Wire Type	PdCuAu 2N
Wire Diameter (mils)	0.8
Substrate Material	BT Resin / DS-7409HGB(G)
Solder Ball Composition	96.5Sn3Ag0.5Cu
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 through 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: CSP_BGA at STATS (SK3) with Cu Wire Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)[2]	JESD22-A103	150°C, 1,000 Hours	ADSP-21569	Q17053.1.3	45	0
				Q17053.2.3	45	0
				Q17053.3.3	45	0
Solder Heat Resistance (SHR) [1,2]	J-STD-020	MSL-3	ADSP-21569	Q17053.1.2	77	0
				Q17053.2.2	77	0
				Q17053.3.2	77	0
Temperature Cycling (TC) [1,2]	JESD22-A104	-55°C/+125°C, 2,000 Cycles	ADSP-21569	Q17053.1.2	77	0
				Q17053.2.2	77	0
				Q17053.3.2	77	0
Temperature Humidity Bias (THB) [1,2]	JESD22-A101	85°C, 85%RH, Biased, 2,000 Hours	ADSP-21569	Q17053.1.1	77	0
				Q17053.2.1	77	0
				Q17053.3.1	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] Units were tested pre and post stress and ambient and hot temperature

Table 3: ADSP-2156x CSP_BGA at STATS (SK3) with Au Wire Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Unbiased HAST (UHST) [1,2]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADSP-21569	Q13499.12	77	0
				Q13499.13	77	0
				Q13499.32	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] Pre- and post-stress electrical test was performed at room temperature.

Table 3: 28nm CMOS at TSMC Fab-15 Fab Qualification Test Results
Table 4: ADSP2156x CMOS at TSMC Fab-15 Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Operating Life (HTOL) [1,3]	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADSP-21569	Q13499.1	77	0
				Q13499.2	77	0
				Q13499.3	77	0
				Q16972.1.1	77	0
High Temperature Storage Life (HTSL) [1,2]	JESD22-A103	150°C, 1,000 Hours	ADSP-21565	Q13566.14	45	0
			ADSP-21569	Q13499.8	45	0
Power and Temp Cycling (PTC)[1,2]	JESD22-A105	-40°C/+105°C, P1000	ADSP-21565	Q16792.1.11	45	0
Early Life Failure Rate (ELFR) [2]	AEC Q100-008	Tj=125C, Biased, 48 Hours	ADSP-21569	Q16972.1.14	115	0
				Q16972.2.3	92	0
				Q16972.3.3	164	0
				Q16972.1.15	102	0
				Q16972.1.19	39	0
				Q16972.4.1	165	0
				Q16972.5.2	148	0
				Q16972.5.3	148	0
				Q16972.5.1	114	0
				Q16972.5.4	45	0
				Q16972.5.5	160	0
				Q16972.5.6	160	0
				Q16972.5.8	160	0
				Q16972.5.7	160	0
				Q16972.4.2	149	0
				Q16972.3.4	104	0
				Q16972.5.9	26	0
				Q16972.3.5	93	0
				Q16972.4.3	119	0
				Q16972.4.4	154	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] Pre- and post-stress electrical test was performed at room and hot temperatures.

[3] Pre- and post-stress electrical test was performed at room, hot, and cold temperatures.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 5. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 5: ADSP-21569 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	400-CSP_BGA	C Q100-011	1Ω, Cpkg	±750V	±1000V	C2b
HBM	400-CSP_BGA	ESDA/JEDEC JS-001-2011	1.5kΩ, 100pF	±3000V	±3500V	2

Latch-Up Test Results

Three samples of the ADSP-21565, ADSP-21569 were latch-up tested at T_A=105°C per JEDEC Standard JESD78, Class II. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+200mA	-200mA	2.842/5.205/2.37/1.185/1.582V

Approvals

Reliability Engineer: Carolyn Pipitone

Additional Information

Data sheets and other additional information are available on Analog Devices' web site