

LTM4668A/LTM4668 Data Sheet Revision

Data Sheet Specification Comparison LTM4668A

LTM4668A

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, per the typical application.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Switching Regulator Section: (Per Channel)							
V_{IN}	Input DC Voltage		● 2.7		17	V	
$V_{OUT(RANGE)}$	Output Voltage Range	$V_{IN} = 2.7\text{V to } 17\text{V}$ (Step-Down Only)	● 0.6		5.5	V	
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	$C_{IN} = 10\mu\text{F}$, $C_{OUT} = 47\mu\text{F}$ Ceramic $R_{FB} = 13.3\text{k}$, $MODE = INTV_{CC}/2$ $V_{IN} = 5\text{V to } 17\text{V}$, $I_{OUT} = 0\text{A to } 1.2\text{A}$	● 3.25	3.30	3.35	V	
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising	Change to 0.35V	0.55	0.7	0.9	V
$I_{Q(VIN)}$	Input Supply Bias Current	$V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $MODE = INTV_{CC}/2$ (CCM) $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $MODE = INTV_{CC}$ (Burst) $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $MODE = GND$ (PS) Shutdown, $RUN = 0$, $V_{IN} = 12\text{V}$		75 0.5 200 1		mA mA μA μA	
$I_{S(VIN)}$	Input Supply Current	$V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $I_{OUT} = 1.2\text{A}$		390		mA	
$I_{OUT(DC)}$	Output Continuous Current Range	$V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$ (Note 4)	0		1.2	A	
$\frac{\Delta V_{OUT}(\text{Line})}{V_{OUT}}$	Line Regulation Accuracy	$V_{OUT} = 3.3\text{V}$, $V_{IN} = 5\text{V to } 17\text{V}$, $I_{OUT} = 0\text{A}$	●	0.01	0.1	%/V	
$\frac{\Delta V_{OUT}(\text{Load})}{V_{OUT}}$	Load Regulation Accuracy	$V_{OUT} = 3.3\text{V}$, $I_{OUT} = 0\text{A to } 1.2\text{A}$	●	0.1	0.75	%	
$V_{OUT(AC)}$	Output Ripple Voltage	$I_{OUT} = 0\text{A}$, $C_{OUT} = 47\mu\text{F}$ Ceramic $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$		8		mV	
$\Delta V_{OUT(START)}$	Turn-On Overshoot	$I_{OUT} = 0\text{A}$, $C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$		30		mV	
t_{START}	Turn-On Time	$C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, No Load		0.8		ms	
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load $C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$		70		mV	
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load $C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$		30		μs	
I_{OUTPK}	Output Current Limit	$V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$		2		A	
V_{FB}	Voltage at V_{FB} Pin	$I_{OUT} = 0\text{A}$, $V_{OUT} = 3.3\text{V}$	● 0.591	0.60	0.609	V	
I_{FB}	Current at V_{FB} Pin	(Note 3)			± 10	nA	
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins		60.05	60.40	60.75	k Ω	
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)		60		ns	

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output	Change to -12%	-7.5	Change to 12%	%
		V_{FB} Ramping Negative	-11	7.5	11	%
		V_{FB} Ramping Positive				
R_{PGOOD}	PGOOD Resistance			275		Ω
V_{INTVCC}	Internal V_{CC} Voltage	$V_{IN} = 6\text{V}$ to 17V	4.7	5	5.3	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Up	2.3	2.5	2.7	V
UVLO(HYS)	UVLO Hysteresis			250		mV
f_{OSC}	Oscillator Frequency			2.25		MHz
SYNC	SYNC Capture Range		1500		3000	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4668A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4668AE is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full -40°C to 125°C internal operating temperature range are assured by design, characterization and correlation

with statistical process controls. The LTM4668AI is guaranteed to meet specifications over the full -40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: 100% tested at wafer level

Note 4: See output current derating curves for different V_{IN} , V_{OUT} and T_A .

Note 5: Guaranteed by design.

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$I_{OUT(DC)}$	Output Continuous Current Range	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$ (Note 4)	0		1.2	A	
$\frac{\Delta V_{OUT}(\text{Line})}{V_{OUT}}$	Line Regulation Accuracy	$V_{OUT} = 1.5\text{V}$, $V_{IN} = 2.7\text{V}$ to 17V , $I_{OUT} = 0\text{A}$	●	0.01	0.1	%/V	
$\frac{\Delta V_{OUT}(\text{Load})}{V_{OUT}}$	Load Regulation Accuracy	$V_{OUT} = 1.5\text{V}$, $I_{OUT} = 0\text{A}$ to 1.2A	●	0.1	0.75	%	
$V_{OUT(AC)}$	Output Ripple Voltage	$I_{OUT} = 0\text{A}$, $C_{OUT} = 47\mu\text{F}$ Ceramic $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$		7		mV	
$\Delta V_{OUT(START)}$	Turn-On Overshoot	$I_{OUT} = 0\text{A}$, $C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$		30		mV	
t_{START}	Turn-On Time	$C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$, No Load		0.8		ms	
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load $C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$		50		mV	
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load $C_{OUT} = 47\mu\text{F}$ Ceramic, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$		50		μs	
I_{OUTPK}	Output Current Limit	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$		2		A	
V_{FB}	Voltage at V_{FB} Pin	$I_{OUT} = 0\text{A}$, $V_{OUT} = 1.5\text{V}$	●	0.591	0.60	0.609	V
I_{FB}	Current at V_{FB} Pin	(Note 3)			± 10	nA	
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins			60.05	60.40	60.75	$\text{k}\Omega$
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)		60		ns	
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		-11	-8	Change to 12%	%
				8	11		%
R_{PGOOD}	PGOOD Resistance			275		Ω	
V_{INTVCC}	Internal V_{CC} Voltage	$V_{IN} = 6\text{V}$ to 17V		4.7	5	5.3	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Up		2.3	2.5	2.7	V
UVLO(HYS)	UVLO Hysteresis			250		mV	
f_{OSC}	Oscillator Frequency			1		MHz	
SYNC	SYNC Capture Range		500		1500	kHz	

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