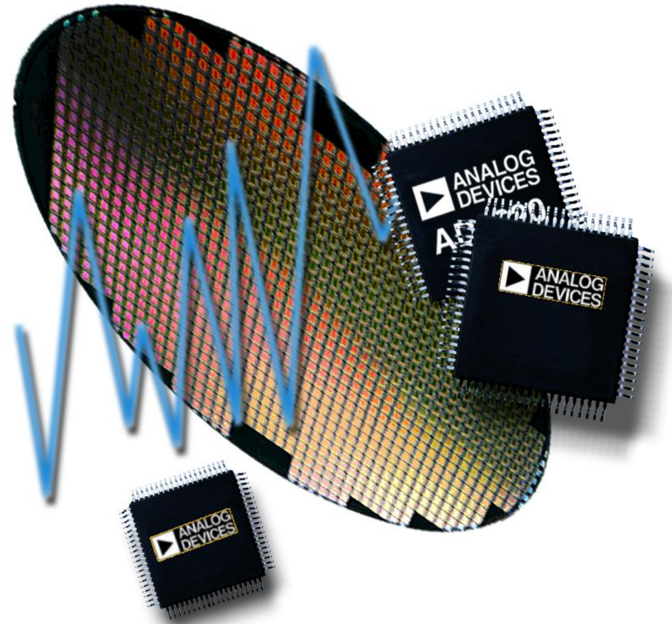

Reliability Report

Report Title: Qualification of HVBP2 and EP200 processes in Wilmington Wafer Fab Site

Report Number: 20828

Revision: A

Date: 28 March 2023

Summary

This report documents the reliability qualification requirements for the release of the HVBP2 and EP200 Wafer Fabrication Process in Analog Devices Wilmington Wafer Fabrication Facility. The products listed below were selected to cover the technology being released

The products are:

- The AD8226 is a Wide Supply Range, Rail to Rail Output Instrumentation Amplifier in an 8-SOIC package.
- The AD8676 is an Ultra Precision, 36V, 2.8nV/√Hz, Dual RRO Operational Amplifier in an 8-SOIC package.
- The ADTL084 is a JFET input amplifier ideal for various applications, including process control, industrial and instrumentation equipment, active filtering, data conversion, buffering, and power control and monitoring in a14-SOIC-N package

AECQ100 Qualification Test Methods and Summary

AEC Test Group	AEC Stress Test Name	Abbreviation	AEC Test #	Reference
Group A ACCELERATED ENVIRONMENT STRESS TESTS	Preconditioning	PC	A1	Table 2 and Table 4
	Temperature Humidity Bias or Biased-HAST	THB or HAST	A2	
	Autoclave or Unbiased HAST or Temperature Humidity (without Bias)	AC, UHST, or TH	A3	
	Temperature Cycle	TC	A4	
	Power Temperature Cycling	PTC	A5	
	High Temperature Storage Life	HTSL	A6	
Group B ACCELERATED LIFETIME SIMULATION TESTS	High Temperature Operating Life	HTOL	B1	Table 2 and Table 4
	Early Life Failure Rate	ELFR	B2	
	NVM Endurance, Data Retention, and Operational Life	EDR	B3	
Group C PACKAGE ASSEMBLY INTEGRITY TESTS	Wire Bond Shear	WBS	C1	• Test C2 (and C1 for Cu Wire) are shown in Table 4. • Tests C3-6 are qualified and controlled with inline monitors and may be viewed on-site at Analog Devices.
	Wire Bond Pull Strength	WBP	C2	
	Solderability	SD	C3	
	Physical Dimensions	PD	C4	
	Solder Ball Shear	SBS	C5	
	Lead Integrity	LI	C6	
Group D DIE FABRICATION RELIABILITY TESTS	Electromigration	EM	D1	Die Fabrication Reliability data may be viewed on-site at Analog Devices.
	Time Dependent Dielectric Breakdown	TDDB	D2	
	Hot Carrier Injection	HCI	D3	
	Negative Bias Temperature Instability	BTI	D4	
	Stress Migration	SM	D5	
Group E ELECTRICAL VERIFICATION TESTS	Pre- and Post-Stress Electrical Test	TEST	E1	Table 5 and Table 6
	Electrostatic Discharge Human Body Model	HBM	E2	
	Electrostatic Discharge Charged Device Model	CDM	E3	
	Latch-Up	LU	E4	
	Electrical Distributions	ED	E5	• For Tests E5, E6 and E7, ADI New Product Yield Analysis Testing Guidelines meet AEC Q100 requirements. • Results for Tests E7-E11 are available as applicable on a case by case basis. • Test E12 results may be viewed on-site at Analog Devices
	Fault Grading	FG	E6	
	Characterization	CHAR	E7	
	Electromagnetic Compatibility	EMC	E9	
	Short Circuit Characterization	SC	E10	
	Soft Error Rate	SER	E11	
	Lead (Pb) Free	LF	E12	
Group F DEFECT SCREENING TESTS	Process Average Test	PAT	F1	ADI New Product Yield Analysis Testing Guidelines meet AECQ100 Requirements.
	Statistical Bin/Yield Analysis	SBA	F2	
Group G CAVITY PACKAGE INTEGRITY TESTS	Mechanical Shock	MS	G1	<Applicable only for Cavity Packages>
	Variable Frequency Vibration	VFV	G2	
	Constant Acceleration	CA	G3	
	Gross/Fine Leak	GFL	G4	
	Package Drop	DROP	G5	
	Lid Torque	LT	G6	
	Die Shear	DS	G7	
	Internal Water Vapor	IWV	G8	

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- <2.5um^2 Bipolar

Product Characteristics	Product(s) to be qualified		
Generic/Root Part #	AD8226	AD8676	ADTL084
Die Id	8226 0	8676 0	TL084 0
Die Size (mm)	1.65 x 1.42	1.49 x 1.9	1.43 x 1.25
Wafer Fabrication Site	ADI-Wilmington	ADI-Wilmington	ADI-Wilmington
Wafer Fabrication Process	<2.5um^2 Bipolar	<2.5um^2 Bipolar	<2.5um^2 Bipolar
Die Substrate	Si	Si	Si
Metallization / # Layers	AlCu (0.5%)/2	AlCu (0.5%)/2	AlCu (0.5%)/2
Polyimide	No	No	No
Passivation	Doped-Oxide/OxyNitride	Doped-Oxide/OxyNitride	Doped-Oxide/OxyNitride

Die/Fab Test Results

Table 2A

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD8226	Q19702.1.HS1_RES	0/77	R
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	130°C 85%RH 33.3 psia, Biased, 96 Hours	AD8226	Q19702.1.HA1_RES	0/77	R
				Q19702.2.HA2_RES	0/77	R
				Q19702.3.HA3_RES	0/77	R
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 500 Hours	AD8226	Q19702.1.HO1_RES	0/77	R
				Q19702.2.HO2_RES	0/77	R
				Q19702.3.HO3_RES	0/77	R

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Table 2B

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
Early Life Failure Rate (ELFR)	B2	AEC Q100-008	Ta=125°C, 48 Hours	AD8676	Q19671.1.EL1A_RES	0/400	RH
					Q19671.1.EL1B_RES	0/400	RH
					Q19671.2.EL2A_RES	0/400	RH
					Q19671.2.EL2B_RES	0/400	RH
					Q19671.3.EL3A_RES	0/399	RH
					Q19671.3.EL3B_RES	0/400	RH
					Q19671.3.EL3C_RES	0/5	RH
High Temperature Operating Life (HTOL)	B1	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	AD8676	Q19671.1.HO1_RES	0/77	RHC
					Q19671.2.HO2_RES	0/77	RHC
					Q19671.5.HO3_RES	0/77	RHC
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130°C 85%RH 33.3 psia, Biased, 96 Hours	AD8676	Q19671.3.HA3_RES	0/77	RH
					Q19671.4.HA4_RES	0/77	RH
					Q19671.5.HA5_RES	0/77	RH

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Table 2C

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
High Temperature Operating Life (HTOL)	B1	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADTL084	Q19700.1.HO1_RES	0/77	RHC
					Q19700.2.HO2_RES	0/77	RHC
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 2,000 Hours	ADTL084	Q19700.1.HS1_RES	0/77	RH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	110°C 85%RH 17.7 psia, Biased, 264 hours	ADTL084	Q19700.1.HA1_RES	0/77	RH
					Q19700.2.HA2_RES	0/77	RH
					Q19700.3.HA3_RES	0/77	RH

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - 8-SOIC_N at ASE (AET)

Product Characteristics	Product(s) to be qualified		
Generic/Root Part #	AD8226	ADTL084	AD8676
Package	8-SOIC_N	14-SOIC_N	8-SOIC_N
Body Size (mm)	4.00 x 5.00 x 1.50	4.00 x 8.75 x 1.50	4.00 x 5.00 x 1.50
Assembly Location	ASE (AET)	ASE (AET)	Amkor (AP1)
MSL/Peak Reflow Temperature(°C)	1 / 260°C	1 / 260°C	1 / 260°C
Mold Compound	Hitachi CEL 9240HF10AK	Hitachi CEL 9240HF10AK	Sumitomo G600
Die Attach/Underfill/TIM	Hitachi EN 4900GC Conductive	Hitachi EN 4900GC Conductive	Ablestik 84-1 LMISR4 Conductive
Leadframe Material	Copper	Copper	Copper
Lead Finish	Matte Tin	Matte Tin	Matte Tin
Wire Bond Material/Diameter (mils)	Tanaka GPG-2 2N Gold / 1.00	Tanaka GPG-2 2N Gold / 1.00	2N Gold/1.2

Package/Assembly Test Results

Table 4A: Package/Assembly Test Results - SOIC_N at ASE (AET)

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	AD8226	Q19702.1.HS1_RES	0/77	R
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	130°C 85%RH 33.3 psia, Biased, 96 Hours	AD8226	Q19702.1.HA1_RES	0/77	R
				Q19702.2.HA2_RES	0/77	R
				Q19702.3.HA3_RES	0/77	R
Solder Heat Resistance (SHR)	J-STD-020	MSL-1	AD8226	Q19702.1.SH1_RES	0/11	R
				Q19702.2.SH2_RES	0/11	R
				Q19702.3.SH3_RES	0/11	R
Temperature Cycling (TC)[1]	JESD22-A104	-65°C/+150°C, 1,000 Cycles	AD8226	Q19702.1.TC1_RES	0/77	R
				Q19702.2.TC2_RES	0/77	R
				Q19702.3.TC3_RES	0/77	R
Unbiased HAST (UHST)[1]	JESD22-A118	130°C 85%RH 33.3 psia, 96 Hours	AD8226	Q19702.1.UH1_RES	0/77	R
				Q19702.2.UH2_RES	0/77	R
				Q19702.3.UH3_RES	0/77	R

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Table 4B: Package/Assembly Test Results - SOIC_N at ASE (AET)

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
High Temperature Storage Life (HTSL)	A6	JESD22-A103	150°C, 2,000 Hours	ADTL084	Q19700.1.HS1_RES	0/77	RH
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	110°C 85%RH 17.7 psia, Biased, 264 hours	ADTL084	Q19700.1.HA1_RES	0/77	RH
					Q19700.2.HA2_RES	0/77	RH
					Q19700.3.HA3_RES	0/77	RH
Solder Heat Resistance (SHR)	A1	J-STD-020	MSL-1	ADTL084	Q19700.1.SH1_RES	0/11	R
					Q19700.2.SH2_RES	0/11	R
					Q19700.3.SH3_RES	0/11	R
Temperature Cycling (TC)[1]	A4	JESD22-A104	-65°C/+150°C, 1,000 Cycles	ADTL084	Q19700.1.TC1_RES	0/77	H
					Q19700.3.TC2_RES	0/77	H
					Q19700.5.TC3_RES	0/77	H
Unbiased HAST (UHST)[1]	A3	JESD22-A118	130°C 85%RH 33.3 psia, 96 Hours	ADTL084	Q19700.1.UH1_RES	0/77	R
					Q19700.2.UH2_RES	0/77	R
					Q19700.3.UH3_RES	0/77	R
Wire Bond Pull	C2	MIL-STD-883, M2011	Post TCT, Single Duration	ADTL084	Q19700.1.WP1_RES	0/10	R
					Q19700.2.WP2_RES	0/10	R

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

Table 4C: Package/Assembly Test Results - SOIC_N at AMKOR (AP1)

Test Name	AEC #	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS	eTest Temp
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	A2	JESD22-A110	130°C 85%RH 33.3 psia, Biased, 96 Hours	AD8676	Q19671.3.HA3_RES	0/77	RH
					Q19671.4.HA4_RES	0/77	RH
					Q19671.5.HA5_RES	0/77	RH
Solder Heat Resistance (SHR)	A1	J-STD-020	MSL-1	AD8676	Q19671.3.SH3_RES	0/11	R
Temperature Cycling (TC)[1]	A4	JESD22-A104	-65°C/+150°C, 1,000 Cycles	AD8676	Q19671.5.TC3_RES	0/77	H
					Q19671.6.TC6_RES	0/77	H
					Q19671.7.TC7_RES	0/77	H
Unbiased HAST (UHST)[1]	A3	JESD22-A118	130°C 85%RH 33.3 psia, 96 Hours	AD8676	Q19671.3.UH3_RES	0/77	R
					Q19671.4.UH4_RES	0/77	R
					Q19671.5.UH5_RES	0/77	R
Wire Bond Pull	WBP	MIL-STD-883, M2011	Post TCT, Single Duration	AD8676	Q19671.1.WP3_RES	0/10	R

[1] These samples were subjected to preconditioning at MSL 1 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 5: AD8676 ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class	eTest Temp
FICDM	AD8226	8-SOIC_N	JS-002	1Ω, Cpkg	±1250V	C3	R
HBM	AD8226	8-SOIC_N	JS-001	1.5kΩ, 100pF	±1000V	1C	R
FICDM	ADTL084	14-SOIC_N	JS-002	1Ω, Cpkg	±1250V	C3	RH
HBM	ADTL084	14-SOIC_N	JS-001	1.5kΩ, 100pF	±4000V	3A	RH
FICDM	AD8676	8-SOIC_N	JS-002	1Ω, Cpkg	±1250V	C3	RH
HBM	AD8676	8-SOIC_N	JS-001	1.5kΩ, 100pF	±2000V	2	RH

Table 6: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class	eTest Temp
JESD78	AD8226	+150ma, -150ma	+14.3V	25°C	I	R
JESD78	ADTL084	+200mA, -200mA	+24V	25°C	I	R
JESD78	AD8676	+150ma, -150ma	+24V	125°C	II	RH

Approvals

Reliability Engineer: Denis Belisle