TEST

PRODUCT

QUALIFICATION

REPORT

TITLE:

ADAU1850 Test Correlation Report for JC3 & UT1

PCN Number: 21_0236

REVISION: A

DATE: 14Dec, 2021

PROJECT BACKGROUND:

The ADAU1850 is currently undergoing production testing at the UT1(UTAC). It is a business strategic decision to qualify JC3(JCAP) to be additional test site to ensure continuity in supply. But for wafer fab and RDL process, they are all completed in TSMC and ship to UT1 and JC3 for probing test.

SUMMARY:

The ADAU1850 is a codec with three inputs and one output that incorporates one digital signal processor. The path from the analog input to the DSP core to the analog output is optimized for low latency and is ideal for noise canceling earphones. With the addition of a few passive components, the ADAU1850 provides a complete headset solution.

The ADAU1850 is a low power audio codec with an optimized audio processing core, making it ideal for noise canceling applications that require high quality audio, low power, small size, and low latency. The serial audio port is compatible with I2S, left justified, right justified, and time division multiplexing (TDM) modes, with tristating for interfacing to digital audio data. The operating voltage of AVDD and HPVDD is 1.8 V, and an internal regulator is used to generate the digital supply voltage.

The input signal path includes flexible configurations that can accept differential or single-ended analog microphone inputs. AIN2 supports single-ended analog microphone inputs only. Each input signal has its own programmable gain amplifier (PGA) for volume adjustment. The ADCs and DAC are high quality, 24-bit sigma-delta (Σ-Δ) converters that operate at a selectable 12 kHz to 768 kHz sampling rate and the ADCs also support 8 kHz or 16 kHz sampling rate in voice wake-up mode. The ADCs and DAC have an optional high-pass filter with a cutoff frequency of 1 Hz, 4 Hz, or 8 Hz and fine step digital soft volume controls.

The DAC output is capable of differentially driving a headphone earpiece speaker with 16 Ω impedance or higher. There is also the option to change to line output mode when the output is loaded differentially with ≥10 kΩ.

Test product transfer qualification was performed according to Analog Devices Specification to ensure two test sites are statistically equivalent. Same tester platform, test hardware is used in both sites, there is no change to the form, fit, function, quality and reliability of the product.

This report documents the successful completion of the product test transfer requirements for the release of ADAU1850 in JC3.

TEST AND PRODUCT INFORMATION:

Device: ADAU1850

Package: 0.4mm pitch, 2.957mm * 1.757mm WLCSP

Leads: 28 balls

Affected products:

Generics	FGs
ADAU1850	ADAU1850-W
	ADAU1850BCBZRL

Tester Platform: MFLEX-MS

Device Interface Board: P-69342 / P-75493

Test socket: P-71015

DESCRIPTION AND TEST RESULTS:

Below tables provide description of the qualification tests conducted and corresponding test results for ADAU1850. All the units have undergone electrical tests on both the sending and receiving sites on the same test platform. Any device that will not meet the electrical qualification requirements will mean failure of the qualification and require solid corrective actions and a repeat of the qualification process. Qualification activities performed, and acceptance criteria is shown on Table 1 below:

Table 1: *Qualification Activities and Acceptance Criteria*

Qualification Activity	Purpose	Sample Quantity	Accept Criteria
Device Repeatability Correlation	To check if the devices have stable performance from repeatability test and correlated for UT1 and JC3	4pcs units for each test site (Quad Sites Testing)	* Mean Shift ≤ 5% * CPK≥1.67 * Or other specified
Device Parametric Distribution Correlation	To check if the devices from UT1 and JC3 has the correlated parametric distribution for all tested items	100pcs units for each test site (Quad Sites Testing)	* Mean Shift ≤ 5% * CPK≥1.67 * Or other specified

Raw data and analysis report were analyzed and summarized in Table3 (Device Repeatability Correlation) and Table4(Device Parametric Distribution Correlation).

Table 2: *Lot Details for Correlation*

Device PN BACKEND SITE	FAB LOT# WAFER ID#	ASSEMBLY LOT#	DATE CODE
ADAU1850 **UT1**	P64188_#06	5521582.1	2146
ADAU1850 **JC3**	P64189_#07	5524512.1	2139

Table 3: *Device Repeatability Correlation Result*

Generic	Package	Lot Number	Repeatability Correlated between UT1 and JC3?
ADAU1850	28L -WLCSP	5521582.1(UT1)/5524512.1(JC3)	YES

Table 4: *Device Parametric Distribution Correlation Result*

Generic	Package	Lot Number	Parametric Distribution Correlated between UT1 and JC3?
ADAU1850	28L -WLCSP	5521582.1(UT1)/5524512.1(JC3)	YES

APPROVALS:

Technical Review Board No. TRB-65076- Add JC3 as new MP site for ADAU1850 WLCSP Testing

ADDITIONAL INFORMATION:

Homepage: https://www.analog.com/en/index.html

Product datasheet: https://www.analog.com/media/en/technical-documentation/data-sheets/adau1850.pdf

Customer Service: https://www.analog.com/en/support/technical-support.html