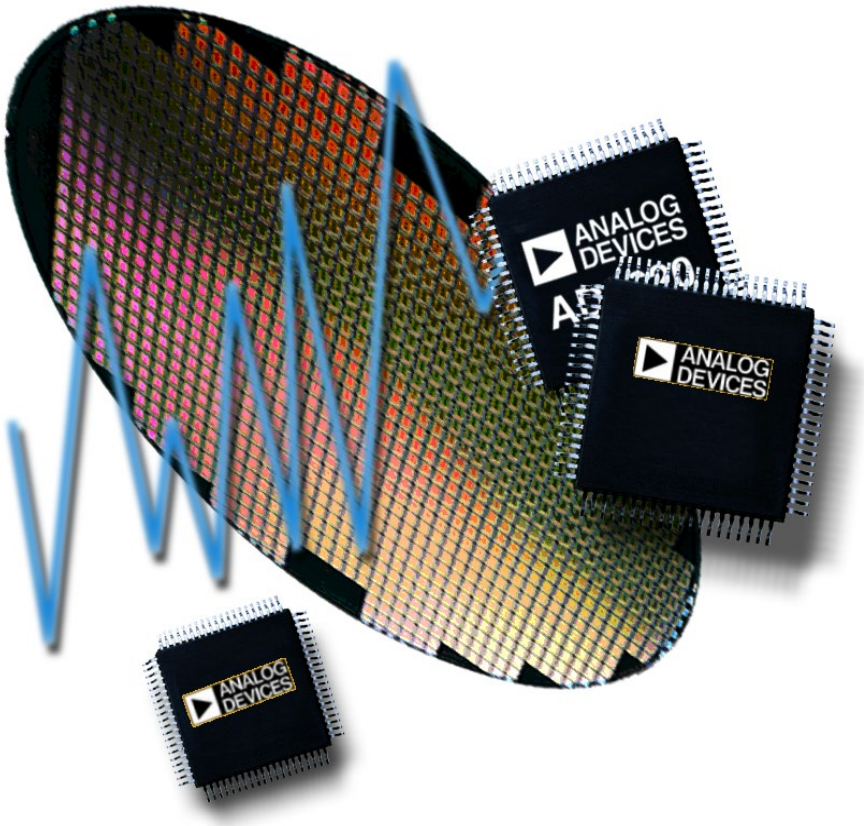

Reliability Report

Report Title: ADAU1850 Die Revison Qualification

Report Number: 19072

Revision: A

Date: 6 January 2022

Summary

This report documents successful completion of the reliability qualification requirements for the release of the ADAU1850 product in a 28-WLCSP package. The ADAU1850 is a three ADC, one DC, low-power codec with audio/fast DSPs. This die revision was performed to (1) to improve performance in single input mode and (2) to be applicable to case without external 24.576MHz as system clock.

Table 1: ADAU1850 Product Characteristics

Die/Fab

Die Id	TMPV51/A
Die Size (mm)	2.997 x 1.797
Wafer Fabrication Site	TSMC-Fab 14
Wafer Fabrication Process	40nm CMOS
Approximate Transistor Count	10,000
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu

Package/Assembly

Package	28-WLCSP
Bump Pitch (mm)	0.4
Bump Diameter (mm)	0.24
Bumping Foundry	TSMC-Fab 14
RDL Composition	Ti(0.05)/Cu(0.3)/Cu(4)
RDL Repassivation	Layer 1: PBO (7.5) Layer 2: PBO (7.5)
Under Bump Metallization	Ti(0.05)/Cu(0.3)/Cu(8.6)
Bumping Process	Cu RDL Bump
Bump Composition	95.5Sn_4.0Ag_0.5Cu
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 through 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: WLCSP at TSMC Fab-14 Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADAU1860	Q17772.1.HS1	45	0
Temperature Cycling (TC)	JESD22-A104	-40°C/125°C, Soak3, 10-14°C/min, 1,000 Cycles	ADAU1860	Q17772.1.TC1	45	0
				Q17772.2.TC2	45	0
				Q17772.3.TC3	45	0
				Q18938.1.TC1	45	0
			ADAU1850	Q17771.1.TC1	45	0
				Q17771.2.TC2	45	0
				Q17771.3.TC3	45	0
Unbiased HAST (UHST)	JESD22-A118	130°C 85%RH 33.3 psia, 96 Hours	ADAU1860	Q17772.1.UH1	45	0
				Q17772.2.UH2	45	0
				Q17772.3.UH3	45	0
				Q18938.1.UH1	77	0
			ADAU1850	Q17771.1.UH1	45	0
				Q17771.2.UH2	45	0
				Q17771.3.UH3	45	0
Temperature Humidity Bias (THB)	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADAU1787	Q13146.5	45	0
				Q13146.6	45	0
				Q13146.7	45	0
				Q15092.15	45	0
				Q15093.8	45	0
				Q16587.8	45	0

Table 3: 40nm CMOS at TSMC Fab-14 Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, M1015	125°C, 48 Hours	ADAU1787	Q13146.17	40	0
				Q13146.18	40	0
				Q13146.19	40	0
				Q13146.20	40	0
				Q13146.21	40	0
				Q13146.22	40	0
				Q13146.23	40	0
				Q13146.24	40	0
				Q13146.25	39	0
				Q13146.26	39	0
				Q13146.27	39	0
				Q13146.28	39	0
				Q13146.29	39	0
				Q13146.30	39	0
				Q13146.31	39	0
				Q13146.32	39	0
				Q13146.33	32	0
				Q13146.34	213	0
				Q13146.35	213	0
				Q13146.36	211	0
				Q13146.37	30	0
				Q13146.40	175	0
				Q13146.41	208	0
				Q13146.42	208	0
				Q13146.43	76	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADAU1860	Q17772.1.HO1	45	0
				Q17772.2.HO2	45	0
				Q17772.3.HO3	45	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADAU1860	Q17772.1.HS1	45	0
Temperature Humidity Bias (THB)[1]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADAU1787	Q13146.5	45	0
				Q13146.6	45	0
				Q13146.7	45	0
				Q15092.15	45	0
				Q15093.8	45	0
				Q16587.8	45	0

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 4. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 4: ADAU1850 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	56-WLCSP	JS-002	1Ω, Cpkg	±1250V	NA	C3
HBM	56-WLCSP	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	NA	3A

Latch-Up Test Results

Three samples of the ADAU1850 were latch-up tested at T_A=25°C per JEDEC Standard JESD78, Class I. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+200mA	-200mA	1.8V, 2.7V

Approvals

Reliability Engineer: Arnold Naniong

Additional Information

Data sheets and other additional information are available on Analog Devices' web site