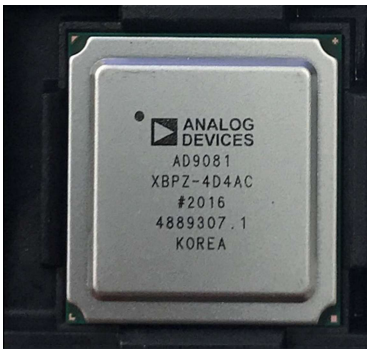
OVERVIEW

This document summarizes the changes made to the AD9082 and the impact to the user. The changes summarized are those from the r1.0 revision to the r2.0 revision.

PACKAGE MARKING



Example of MxFE package marking.

The package marking for the r2.0 version is shown in Figure 1.

Figure 1.

Where

dddd – is the date code of assembly. The starting date code for r2.0 devices is #2043 or later.

LLLLLLL – is the wafer lot code

PART ID READ FROM SPI MAP

Addr	Name	Bits	Bit Name	Description	Register	Access
0x004	SPI_ProdIDL	[7:0]	ProdIDL	Product ID Low	**0x82 – AD9082**	R
0x005	SPIPRrodIDH	[7:0]	ProdIDH	Product ID High	**0x90 – AD9082**	R
0x006	SPI_ChipGrade	[3:0]	DEV_REVISION	Device Revision	**0x3 – R2**; (R1R=0x2)	R

Summary of Changes

Revision Number	Change	Description of Change	Impact
R2.1	DVDD_RT on-chip bypass capacitance	Add additional on-chip bypass capacitance to DVDD_RT Supply	Reduce supply noise on this domain
R2.2	ADC supply monitor	Fix bug where ADC supply monitor always indicated ADC's powered on.	Improve boot initialization process robustness where all supply domains are verified to be on early in process before continuing
R2.3	Temperature Monitoring Unit (TMU functionality	Enabled TMU functionality.	Provides ability to readback on-chip die temperature
R2.4	Serdes Lane Rate Improvement	Design and layout changes to increase SERDES lane rate support to 24.75 GBPS	Allows for higher output bandwidth modes of operation since R1 is rated for 16.22 GBPS
R2.5	Serdes CTLE Improvement	Additional programmability added to support short channel operation. Change to biasing control.	Improves SERDES operation and flexibility.
R2.6	Slew rate detector added to Tx Power Amplifier Protection Feature	Ability to monitor slew rate of digital Tx signal envelope and prevent fault condition should slew rate exceed threshold	Increase robustness of PA protection circuit.
R2.7	SYNCBOUT1+/- flexibity	SYNCBOUT1+/- can be configured as input signal when not used to support 2nd JESD204B link	When configured as an input, these pins can be used for DAC main datapath paging for Fast Frequency Hopping applications where DAC's will be assigned different hop frequencies