

Minor Silicon and Package Laminate Changes to ADRV9026

Qualification Results Summary for the ADRV9026 B0/R2 Revision

QUALIFICATION RESULTS			
TEST	SPECIFICATION	SAMPLE SIZE	STATUS
High Temperature Operating Life (HTOL)*	JEDEC <i>JESD22-A108</i>	1x32	Pass
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3x25	Pass
Temperature/Humidity/Bias (THB)*	JEDEC <i>JESD22-A101</i>	3x25	Pass
High Temperature Storage Life (HTSL)	JEDEC <i>JESD22-A103</i>	1x25	Pass
Latch-Up	JEDEC <i>JESD78</i>	1x12	Pass
Electrostatic Discharge <i>Human Body Model</i>	ESDA/JEDEC <i>JS-001</i>	3/voltage	Pass +/- 1kV, 1C
Electrostatic Discharge <i>Charged Device Model</i>	JEDEC <i>JS-002</i>	3/voltage	Pass +/- 250V, C1

*These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.