ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

ADuCM320/ ADuCM320i ADuCM322/ADuCM322i PCN

11/30/2018

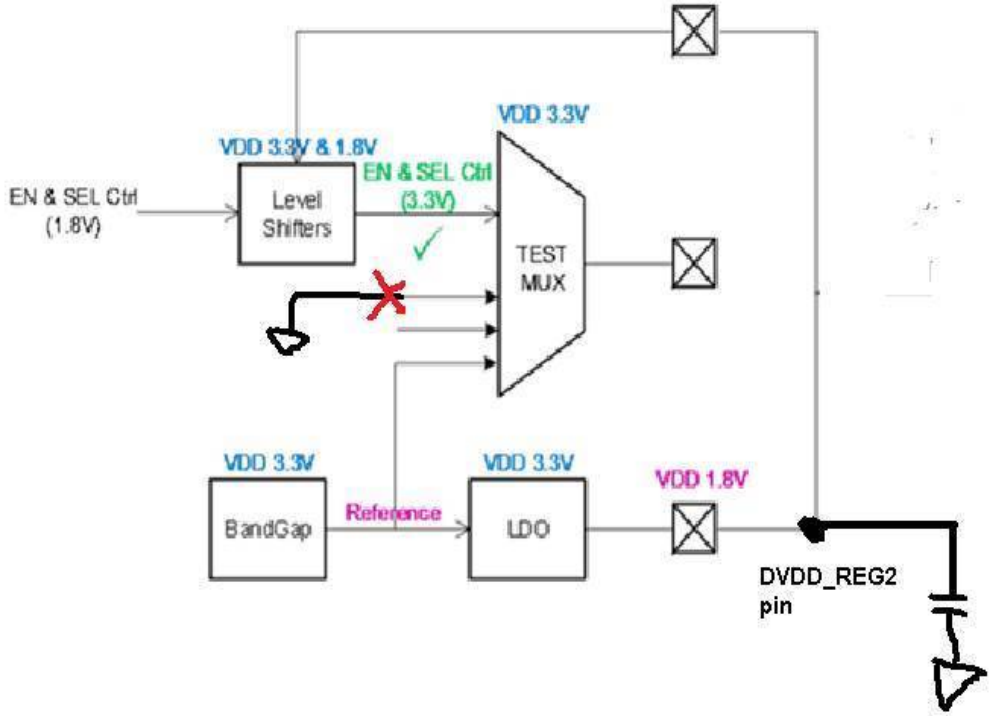
Analog Devices Confidential Information—Not for External Distribution

Background for Silicon Iteration

- A small number of ADuCM32x devices had a Power-up issue
  - Low ppm failure (<10ppm)
  - Failures mainly at low temperatures (<0C) and >50C
  - Failing devices susceptible to Power up problems especially with slow VDD ramp rates
- Issue identified with digital die 1.8V regulator (LDO)
  - Test screen for old silicon revision identified to provide interim cover
    - But not guaranteed to screen all weak parts.
- Silicon edit identified to fully fix the issue
  - All revisions of ADuCM310/ADuCM32x fixed
  - Characterization is complete
- ADI ready to release new revision of ADuCM310/ADuCM32x to production
  - Future shipments will use revised digital die with silicon fix for this issue.

Details on Silicon Change

- Cut a single track to disconnect a grounded input to a Test Mux – see the red “x” below to indicate the location.
- When the 3.3V DVDD power supply is rising from 0V towards the Power-On reset threshold voltage, the enable and select signals to the Test MUX shown below are undefined.
- In some corner cases on previous silicon, this sometimes resulted in the output of the Bandgap being shorted to the GND input of the MUX.
- This meant that the digital LDO did not get a valid bandgap voltage and did not power up correctly.
- The digital LDO output is 1.8V and is required for the Cortex-M3 and other digital peripherals to operate properly.
- In the failing cases, this 1.8V rail did not come up properly and led to the Cortex-M3 never executing user code



Verification

- ATE Verifications Complete: No Issues
  - **Purpose:**
    - To ensure new silicon performance matches previous revision
  - Tested 30x ADuCM320 devices with the ATE production test program at -40C, 25C, 85C
  - Also tested 30x ADuCM310 devices with the ATE production test program at -40C, 25C, 105C

- Bench Verifications Complete: No Issues
  - Power-On reset verification testing completed
  - **Purpose:**
    - To verify silicon change fixed previous Power-on reset issue
  - Tested 3x ADuCM310's, 3x ADuCM320s
    - No ADuCM320i parts were tested (the digital die is common with ADuCM310)
    - Test involved Power cycling parts with random VDD ramp rates from 0.15mS to 750mS
    - All tests repeated in gradual sweep covering all temperatures between -40C to 125C
    - Typically >50,000 tests per unit (total of 528,000 tests)