

PCN 18_0020

AD5671R/75R & AD5675 & AD5672R/76R & AD5676 Timing Specification Changes

This PCN converts data sheet timing specifications that will be changed from the released REV B AD5671R/75R & AD5675 & AD5672R/76R & AD5676 data sheets to the REV C AD5671R/75R & AD5675 & REV D AD5672R/76R & AD5676 data sheets. The old and new specifications are listed in the tables below.

The Rev B AD5671R/75R & AD5675 timing specifications were:

TIMING CHARACTERISTICS

$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$, $1.8\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$, all specifications $-40^{\circ}\text{C to } +125^{\circ}\text{C}$, unless otherwise noted.

Table 5.

Parameter ^{1,2}	Min	Max	Unit	Description
t_1	0.92		μs	SCL cycle time
t_2	0.11		μs	t_{HIGH} , SCL high time
t_3	0.44		μs	t_{LOW} , SCL low time
t_4	0.04		μs	$t_{HD,STA}$, start/repeated start hold time
t_5	40		ns	$t_{SU,DAT}$, data setup time
t_6^3	-0.04		μs	$t_{HD,DAT}$, data hold time
t_7	-0.045		μs	$t_{SU,STA}$, repeated start setup time
t_8	0.195		μs	$t_{SU,STO}$, stop condition setup time
t_9	0.12		μs	t_{BUF} , bus free time between a stop condition and a start condition
t_{10}^4	0		ns	t_r , rise time of SCL and SDA when receiving
$t_{11}^{4,5}$	$20 + 0.1C_B$		ns	t_f , fall time of SCL and SDA when transmitting/receiving
t_{12}	20		ns	LDAC pulse width
t_{13}	0.4		ns	SCL rising edge to LDAC rising edge
t_{14}	4.8		ns	RESET minimum pulse width low, $1.8\text{ V} \leq V_{LOGIC} \leq 2.7\text{ V}$
	6.2		ns	RESET minimum pulse width low, $2.7\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$
t_{15}	132		ns	RESET activation time, $1.8\text{ V} \leq V_{LOGIC} \leq 2.7\text{ V}$
	80		ns	RESET activation time, $2.7\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$
t_{SP}^6	0		ns	Pulse width of suppressed spike
C_B^5		400	pF	Capacitive load for each bus line

¹ See Figure 2.

² Guaranteed by design and characterization; not production tested.

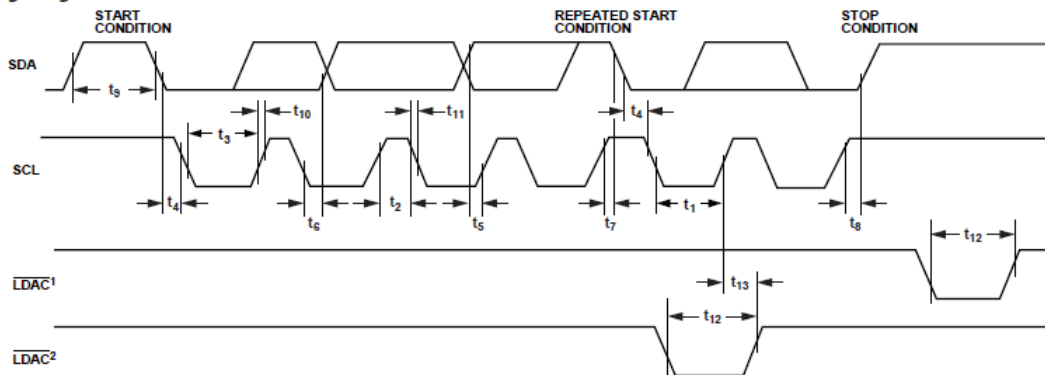
³ A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the SCL falling edge.

⁴ t_r and t_f are measured from $0.3 \times V_{DD}$ to $0.7 \times V_{DD}$.

⁵ C_B is the total capacitance of one bus line in pF.

⁶ Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

Timing Diagrams



NOTES
¹ ASYNCHRONOUS LDAC UPDATE MODE.
² SYNCHRONOUS LDAC UPDATE MODE.

Figure 2. 2-Wire Serial Interface Timing Diagram

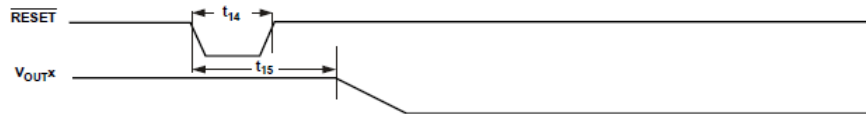


Figure 3. RESET Timing Diagram

The Rev C AD5671R/75R & AD5675 timing specifications are:

TIMING CHARACTERISTICS

$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$, $1.62\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$, all specifications $-40^\circ\text{C to } +125^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter ¹	Min	Max	Unit	Description
t_1	2.5		μs	SCL cycle time
t_2	0.6		μs	t_{HIGH} , SCL high time
t_3	1.3		μs	t_{LOW} , SCL low time
t_4	0.6		μs	$t_{HD,STA}$, start/repeated start hold time
t_5	100		ns	$t_{SU,DAT}$, data setup time
t_6^2	0	0.9	μs	$t_{HD,DAT}$, data hold time
t_7	0.6		μs	$t_{SU,STA}$, repeated start setup time
t_8	0.6		μs	$t_{SU,STO}$, stop condition setup time
t_9	1.3		μs	t_{BUF} , bus free time between a stop condition and a start condition
t_{10}^3	0	300	ns	t_{R} , rise time of SCL and SDA when receiving
t_{11}^3	$20 + 0.1C_B$	300	ns	t_{F} , fall time of SCL and SDA when transmitting/receiving
t_{12}	20		ns	\overline{LDAC} pulse width
t_{13}	400		ns	SCL rising edge to \overline{LDAC} rising edge
t_{14}	8		ns	\overline{RESET} minimum pulse width low, $1.62\text{ V} \leq V_{LOGIC} \leq 2.7\text{ V}$
	10		ns	\overline{RESET} minimum pulse width low, $2.7\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$
t_{15}	90		ns	\overline{RESET} activation time, $1.62\text{ V} \leq V_{LOGIC} \leq 2.7\text{ V}$
	90		ns	\overline{RESET} activation time, $2.7\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$
t_{SP}^4	0	50	ns	Pulse width of suppressed spike
C_B		400	pF	Capacitive load for each bus line

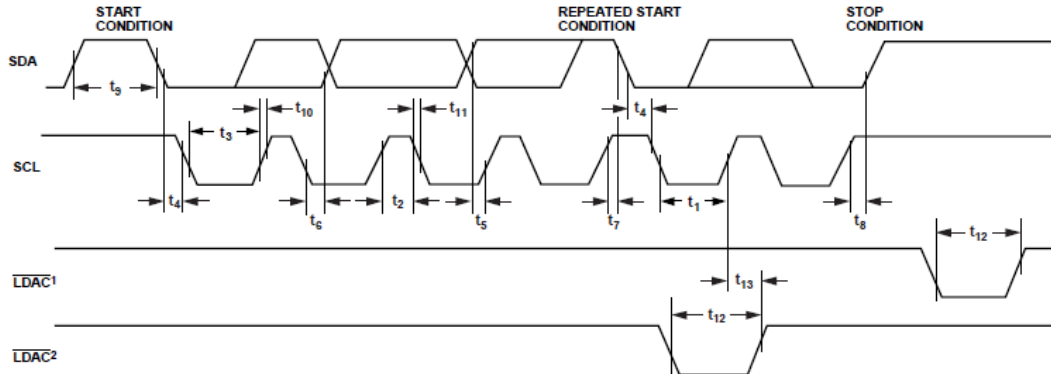
¹ See Figure 2 and Figure 3.

² A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the SCL falling edge.

³ t_R and t_F are measured from $0.3 \times V_{DD}$ to $0.7 \times V_{DD}$.

⁴ Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

Timing Diagrams



NOTES
¹ ASYNCHRONOUS \overline{LDAC} UPDATE MODE.
² SYNCHRONOUS \overline{LDAC} UPDATE MODE.

Figure 2. 2-Wire Serial Interface Timing Diagram

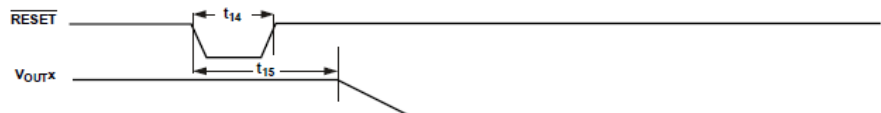


Figure 3. RESET Timing Diagram

The write timing specifications for the AD5672R/76R and AD5676 Rev. B were:

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.8 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$, and $V_{REFIN} = 2.5 \text{ V}$. All specifications -40°C to $+125^\circ\text{C}$, unless otherwise noted. Maximum SCLK frequency is 50 MHz at $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.8 \text{ V} \leq V_{LOGIC} \leq V_{DD}$. Guaranteed by design and characterization; not production tested.

Table 5.

Parameter	$1.8 \text{ V} \leq V_{LOGIC} < 2.7 \text{ V}$		$2.7 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$		Unit	Description
	Min	Max	Min	Max		
t_1	20		20		ns	SCLK Cycle Time
t_2	4		1.7		ns	SCLK High Time
t_3	4.5		4.3		ns	SCLK Low Time
t_4	15.1		10.1		ns	$\overline{\text{SYNC}}$ to SCLK Falling Edge Setup Time
t_5	0.8		0.8		ns	Data Setup Time
t_6	0.1		-0.8		ns	Data Hold Time
t_7	0.95		1.25		ns	SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge
t_8	9.65		6.75		ns	Minimum $\overline{\text{SYNC}}$ High Time (Single, Combined, or All Channel Update)
t_9	4.75		9.7		ns	$\overline{\text{SYNC}}$ Falling Edge to SCLK Fall Ignore
t_{10}	4.85		5.45		ns	$\overline{\text{LDAC}}$ Pulse Width Low
t_{11}	41.25		25		ns	SCLK Falling Edge to $\overline{\text{LDAC}}$ Rising Edge
t_{12}	26.35		20.3		ns	SCLK Falling Edge to $\overline{\text{LDAC}}$ Falling Edge
t_{13}	4.8		6.2		ns	$\overline{\text{RESET}}$ Minimum Pulse Width Low
t_{14}	132		80		ns	$\overline{\text{RESET}}$ Pulse Activation Time
	5.15		5.18		μs	Power-Up Time ¹

¹ Time to exit power-down to normal mode of AD5672R/AD5676R operation, 32nd clock edge to 90% of DAC midscale value, with output unloaded.

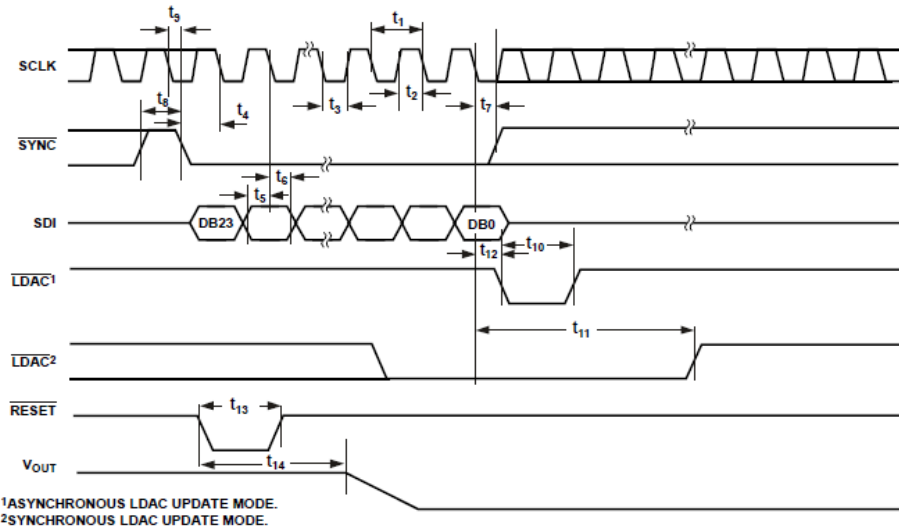


Figure 2. Serial Write Operation

The write timing specifications for the AD5672R/76R and AD5676 Rev. D are:

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.62 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$; $V_{REFIN} = 2.5 \text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 5.

Parameter	Symbol	1.62 V ≤ V _{LOGIC} < 2.7 V		2.7 V ≤ V _{LOGIC} ≤ 5.5 V		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	t ₁	20		20		ns
SCLK High Time	t ₂	8		8		ns
SCLK Low Time	t ₃	10		12		ns
SYNC to SCLK Falling Edge Setup Time	t ₄	15		11		ns
Data Setup Time	t ₅	2		3		ns
Data Hold Time	t ₆	2		2		ns
SCLK Falling Edge to SYNC Rising Edge	t ₇	4		4		ns
Minimum SYNC High Time	t ₈	15		12		ns
SYNC Rising Edge to SYNC Rising Edge (DAC Register Updates)	t ₉	870		830		ns
SYNC Falling Edge to SCLK Fall Ignore	t ₁₀	4		4		ns
LDAC Pulse Width Low	t ₁₁	8		8		ns
SYNC Rising Edge to LDAC Rising Edge	t ₁₂	25		25		ns
SYNC Rising Edge to LDAC Falling Edge	t ₁₃	25		25		ns
LDAC Falling Edge to SYNC Rising Edge	t ₁₄	840		800		ns
Minimum Pulse Width Low	t ₁₅	8		10		ns
RESET Activation Time	t ₁₆	90		90		ns
Power-Up Time ¹		5.5		5.5		μs

¹ Time to exit power-down to normal mode of AD5672R/AD5676R operation, SYNC rising edge to 90% of DAC midscale value, with output unloaded.

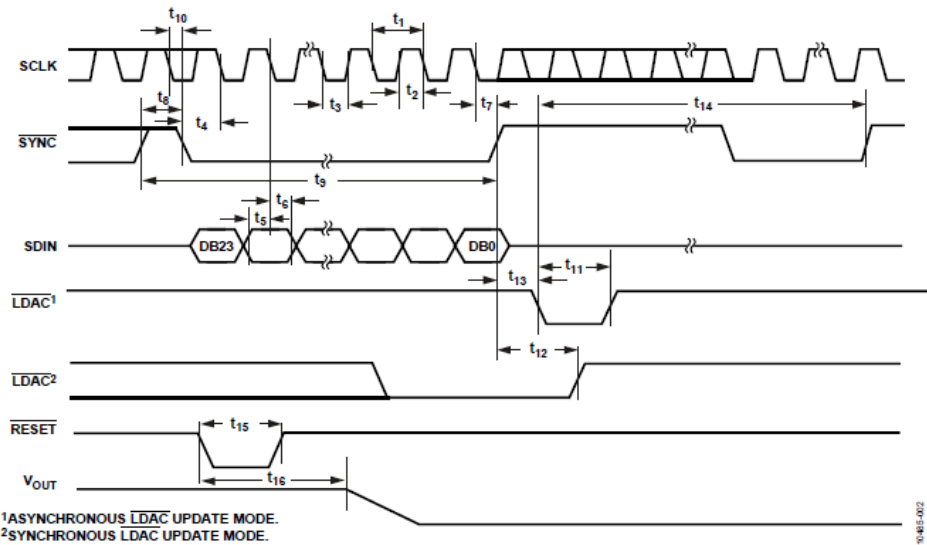


Figure 2. Serial Write Operation

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The daisy-chain and readback timing specifications for the AD5672R/76R and AD5676 Rev. B were:

DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_r = t_f = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.8 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$, $V_{REF} = 2.5 \text{ V}$. All specifications -40°C to $+125^\circ\text{C}$, unless otherwise noted. Maximum SCLK frequency is 25 MHz or 15 MHz at $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.8 \text{ V} \leq V_{LOGIC} \leq V_{DD}$. Guaranteed by design and characterization; not production tested.

Table 6.

Parameter	1.8 V \leq V _{LOGIC} < 2.7 V		2.7 V \leq V _{LOGIC} \leq 5.5 V		Unit	Description
	Min	Max	Min	Max		
t ₁	120		83.3		ns	SCLK Cycle Time
t ₂	33		25.3		ns	SCLK High Time
t ₃	2.8		3.25		ns	SCLK Low Time
t ₄	75		50		ns	SYNC to SCLK Falling Edge
t ₅	1.2		0.5		ns	Data Setup Time
t ₆	0.3		0.4		ns	Data Hold Time
t ₇	16.2		13		ns	SCLK Falling Edge to SYNC Rising Edge
t ₈	55.1		45		ns	Minimum SYNC High Time
t ₁₀	21.5		22.7		ns	SDO Data Valid from SCLK Rising Edge
t ₁₁	24.4		20.3		ns	SCLK Falling Edge to SYNC Rising Edge
t ₁₂	85.5		54		ns	SYNC Rising Edge to SCLK Rising Edge

Circuit Diagram and Daisy-Chain and Readback Timing Diagrams

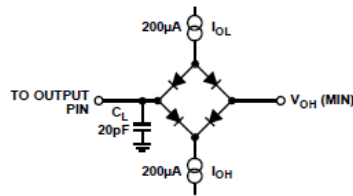


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

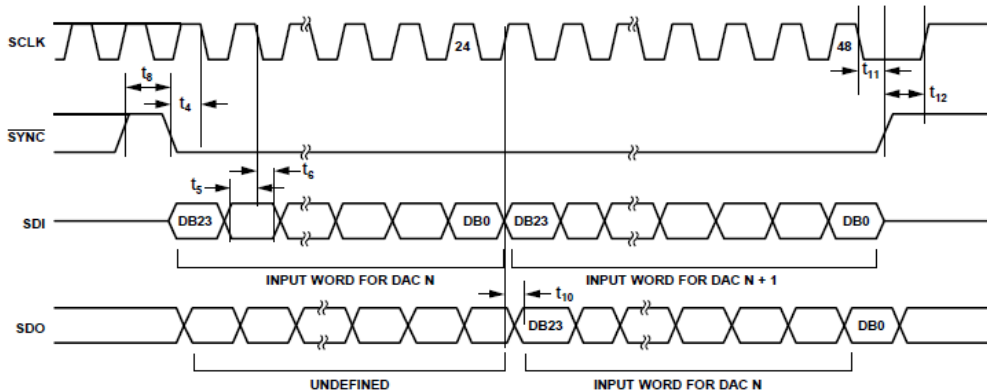


Figure 4. Daisy-Chain Timing Diagram

The daisy-chain and readback timing specifications for the AD5672R/76R and AD5676 Rev. D are:

DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.62 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$; $V_{REF} = 2.5 \text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted. $V_{DD} = 2.7 \text{ V}$ to 5.5 V .

Table 5.

Parameter	Symbol	1.62 V ≤ V _{LOGIC} < 2.7 V		2.7 V ≤ V _{LOGIC} ≤ 5.5 V		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	t ₁	130		110		ns
SCLK High Time	t ₂	33		23		ns
SCLK Low Time	t ₃	12		7		ns
SYNC to SCLK Falling Edge	t ₄	80		80		ns
Data Setup Time	t ₅	2		2		ns
Data Hold Time	t ₆	2		2		ns
SCLK Falling Edge to SYNC Rising Edge	t ₇	35		10		ns
Minimum SYNC High Time	t ₈	55		30		ns
SDO Data Valid from SCLK Rising Edge	t ₉	60		50		ns
SYNC Rising Edge to SCLK Falling Edge	t ₁₀	2		6		ns
SYNC Rising Edge to SDO Disable	t ₁₁	40		35		ns

Circuit and Timing Diagrams

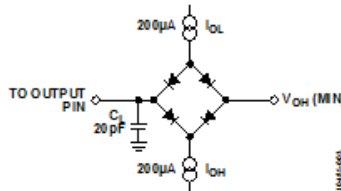


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

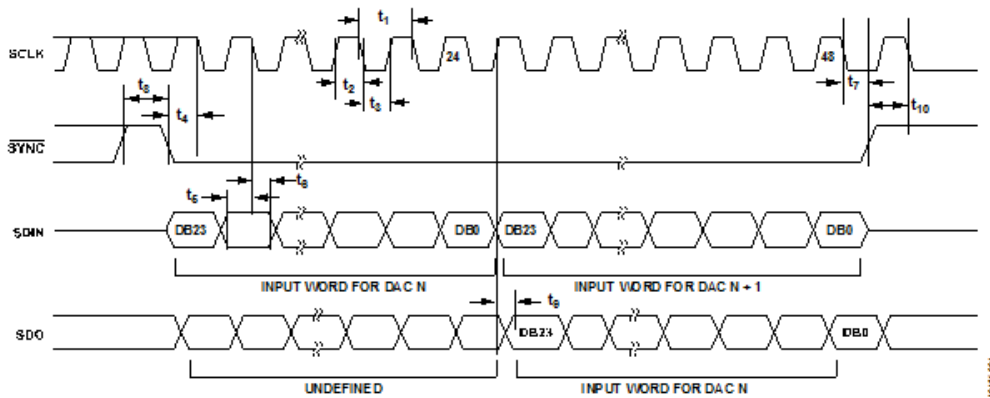


Figure 4. Daisy Chain Timing Diagram