

ADV7181D DDR Timing Specification Update

► Current DDR Timing Specification in ADV7181D Datasheet Rev. A:

Table 4.

Parameter ¹	Symbol	Description	Min	Typ	Max	Unit
DDR (CP) ^{4,5}	t ₁₅	Positive clock edge to end of valid data	$-4 + T_{LLC}/4$			ns
	t ₁₆	Positive clock edge to start of valid data	$0.25 + T_{LLC}/4$			ns
	t ₁₇	Negative clock edge to end of valid data	$-2.95 + T_{LLC}/4$			ns
	t ₁₈	Negative clock edge to start of valid data	$-0.5 + T_{LLC}/4$			ns

⁴ CP timing figures obtained using maximum drive strength value (0xFF) in Register Subaddress 0xF4.

⁵ DDR timing specifications dependent on LLC output pixel clock; $T_{LLC}/4 = 9.25$ ns at LLC = 27 MHz.

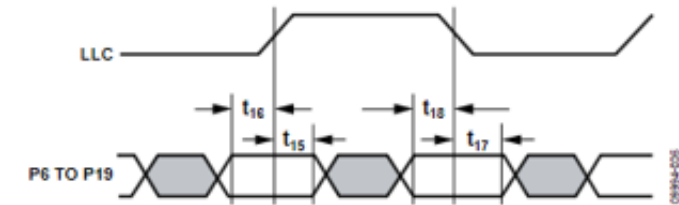


Figure 5. Pixel Port and Control DDR Output Timing (CP Core)

► DDR Timing Specification that will be in ADV7181D Datasheet Rev. B

Parameter ^{1,2}	Symbol	Test Conditions	Min	Typ	Max	Unit
Data Output Transition Time DDR (CP) ^{5,6}	t ₁₅	Positive clock edge to end of valid data	1.9			ns
Data Output Transition Time DDR (CP) ^{5,6}	t ₁₆	Start of valid data to positive clock edge	1.7			ns
Data Output Transition Time DDR (CP) ^{5,6}	t ₁₇	Negative clock edge to end of valid data	1.4			ns
Data Output Transition Time DDR (CP) ^{5,6}	t ₁₈	Start of valid data to negative clock edge	1.7			ns

⁵ CP timing figures obtained using maximum drive strength value (0x3F) in Register Subaddress 0xF4.

⁶ Guaranteed by characterization up to 75 MHz pixel clock.

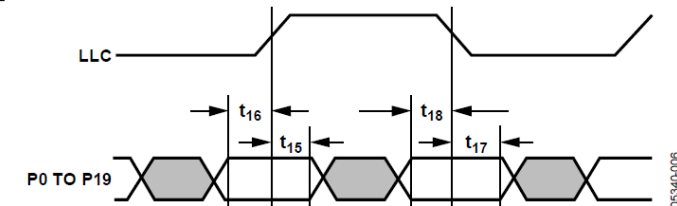


Figure 5. Pixel Port and Control DDR Output Timing (CP Core)