



Product/Process Change Notice - PCN 16_0137 Rev. A

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******* ATTENTION: THIS PCN IS BEING CANCELLED! *******

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

Note: Revised fields are indicated by a red field name. See Appendix B for revision history.

PCN Title: AD9557 and AD9558 die change

Publication Date: 01-Nov-2016

Effectivity Date: Effective upon publication.

Revision Description:

We have determined that a change in the register map is too impactful to many of our customers and will be revising the design to address that issue; another PCN will be issued when ready.

Description Of Change

- 1 New die revision in register 0x000A is 50H
- 2 Removed connection in spare gate cell to reduce current
- 3 APLL VCO design changed to allow more margin over temp with less jitter variation
- 4 A reset on the RF Divider was added to ensure that the RF Divider always powers up in a known state
- 5 VCO calibration fixes to prevent APLL calibration failure and enhance the accuracy of the calibration
- 6 APLL lock detector changed to avoid potential false "loss of lock" indication
- 7 Unintended connection between 1.8V and 3.3V supplies resulted in a current flow during power up. Logic changes and POR enhancements were added to address this
- 8 Added clock gating to prevent possible internal runt pulse
- 9 Reduced internal fan-out improving internal edge rates
- 10 Timer circuit to initiate change
- 11 Added another trigger for digital resets
- 12 Comb/Integrator structure removed from rate conversion circuit
- 13 Changed internal resets to be synchronous
- 14 Digital functionality added to ensure I/O update is functional after setup and updates
- 15 EEPROM flushing state
- 16 Ensure time-stamp generation is not performed until full cycle of calibration

Reason For Change

- 1 Done to help differentiate from the prior version
- 2 Excess static current was drawn in a spare gate
- 3 To enhance the robustness of the part over temperature and guarantee more consistent jitter performance.
- 4 The RF Divider was not functionally robust
- 5 The APLL calibration fails in a very small number of cases on existing silicon, requiring the user to reissue a calibration
- 6 Analysis of the APLL lock detector circuit revealed potential for declaration of false "unlock" events due to a metastable event.
- 7 The feed through caused the other supply to hold a non-zero voltage when it should have been at ground.
- 8 Eliminates a flaw which might have resulted in the device losing lock
- 9 Eliminates a state in which higher jitter would occur
- 10 If user set terminal value of timer to less than its present state, timer would have to roll over before triggering activity
- 11 Prevents a possible cause of lock-up
- 12 CCI had potential to induce an offset between the input and output
- 13 Asynchronous resets could cause some unpredictable behavior
- 14 Improve I/O update functionality
- 15 improve EEPROM readback interaction with reset
- 16 Improve accuracy of Time Stamp generation

Impact of the change (positive or negative) on fit, form, function & reliability

1 If customer reads the die id register, their software may need updating to reflect the new value stored therein
2 Approximately 25 uA less current should be needed to run the device
3 No Impact from this change
4 Reliability of the RF Divider has improved
5 No Impact from this change
6 No Impact from this change
7 No Impact from this change
8 Improves robustness
9 Improves jitter performance
10 Faster response times in certain conditions
11 Improves robustness
12 Improves performance
13 Improves reliability of functionality
14 More reliable performance
15 Eliminates a potential issue when using EEPROM
16 Eliminates potential for extended acquisition time of the DPLL

Product Identification *(this section will describe how to identify the changed material)*

New die revision in register 0x000A is 50H
Older revisions will have a value <50H in this register

Summary of Supporting Information

Qualification has been performed per Industry Standard Test Methods. See attached Qualification Results Summary.

Supporting Documents

Attachment 1: Type: Qualification Results Summary

ADI_PCN_16_0137_Rev_A_AD9557_Die_Revision_PCN_Qual_Table .pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

Americas:	PCN_Americas@analog.com	Europe:	PCN_Europe@analog.com	Japan:	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Existing Parts - Product Family / Model Number (4)				
AD9557 / AD9557BCPZ	AD9557 / AD9557BCPZ-REEL7	AD9558 / AD9558BCPZ	AD9558 / AD9558BCPZ-REEL7	

Appendix B - Revision History			
Rev	Publish Date	Effectivity Date	Rev Description
Rev. -	04-Aug-2016	02-Nov-2016	Initial Release
Rev. A	01-Nov-2016	01-Nov-2016	We have determined that a change in the register map is too impactful to many of our customers and will be revising the design to address that issue; another PCN will be issued when ready.

Analog Devices, Inc.

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