

A New ESD Model: The Charged Strip Model

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Abstract – Microelectronics packaging and testing are increasingly being conducted on devices in strip form. Once charged, strips may discharge through a pin on one IC. The resulting damage is simulated by a new ESD test method: the Charged Strip Model (CSM). CSM withstand voltages are inversely proportional to strip capacitances. Thus, IC's that are immune to Charged Device Model (CDM) damage may be susceptible to CSM damage. Since CSM discharge events may have far more energy than other real-world ESD events, CSM damage can be easily mistaken for EOS damage. CSM damage can be minimized via appropriate strip designs and actions to minimize strip charging during manufacturing.

I. Introduction

The Charged Device Model (CDM) has become a widely accepted and important ESD testing standard in the microelectronics industry. Numerous references have attested to its relevance in modeling “real-world” failures resulting from accumulated charge build-up on packages / die during normal handling and automated manufacturing operations [May94, Reiner95, Wall96, Olney96].

However, the CDM method as described in the ESDA and JEDEC test standards does not describe all instances where charge can build up and discharge through IC devices. One example comes from descriptions of a similar model, called the Charged Board Model (or CBM) [Pierce88, Boxleitner91]. Pierce calculates the discharge fail energy purely based on the difference in capacitance between that of a typical IC and that of a board capacitively coupled (80 pF) to the IC. The CBM failure energy level was shown to decrease as the board capacitance increased (either with a decrease in plate-to-plate distance or an increase in the total board area).

Packaging and testing of high volume IC's has been undergoing dramatic change. For decades, IC assembly facilities have used leadframes consisting of one or several rows of wire-bonded dice that are subsequently encapsulated in plastic molding compound. Figures 1a & 1b show an example of such a leadframe after the encapsulation process. More recently, these leadframes have been enlarged to

comprise numerous rows of wire-bonded dice on what is termed a matrix leadframe or “strip” for short. Regardless of the number of rows of packages, the leadframe has traditionally been designed such that every pin on each package is shorted together to the metal “rails” that comprise the edges of the strip, as shown in Figure 1b. This design ensures that ESD damage cannot occur during processing of the strip prior to singulation (i.e., cutting the strip into individual devices) since all pins on each device are always at equipotential. During the singulation operation, ESD damage is not a potential issue as long as both the strip and singulation tool are grounded. Once singulated, however, each device is susceptible to CDM damage.



Figure 1a: 2 x 36 leadframe strip of 5-lead SOT packages.

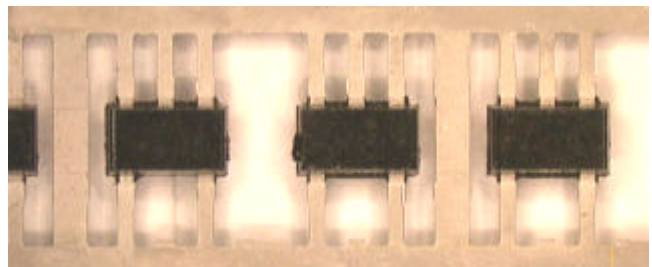


Figure 1b: Magnified view of the above. All pins are shorted together prior to singulation of each 2.9 mm x 1.6 mm x 1.1 mm SOT.

To increase assembly and test throughput for high-volume IC's in popular packages such as the Quad Flat Pack (QFP), Small Outline Integrated Circuit (SOIC), Shrink Small Outline Package (SSOP), Small Outline Transistor (SOT), and Chip-Scale Package (CSP), the semiconductor industry is rapidly transitioning to conducting both package assembly and electrical testing with the devices still attached to the strip. To facilitate Automatic Test Equipment (ATE) testing of devices in strip form, the device leads are electrically isolated from the metal strip via isolation cuts. However, the individual devices stay attached to the strip via die paddle tie bars at the package ends. Figures 2a & 2b show an example of a strip after the isolation cut process. ATE testing of the isolated devices on the strip is conducted using commercially-available systems that simultaneously contact and test numerous devices in parallel, indexing through the full strip until all devices are tested. Due to the parallel testing and reduced indexing time, strip testing provides much higher throughput than conventional ATE testing of singulated devices. Test results are stored in a strip map (analogous to a wafer map). After test, device leads are trimmed and formed as necessary; devices are marked; and finally the electrically good devices are singulated according to the strip map results.

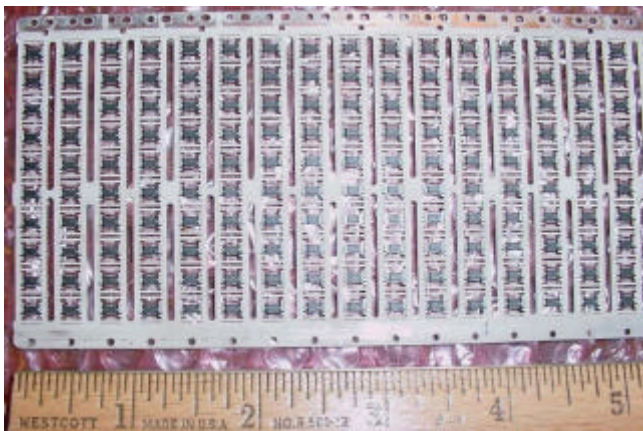


Figure 2a: Portion of a 10 x 30 leadframe strip of 8-lead CSP's.

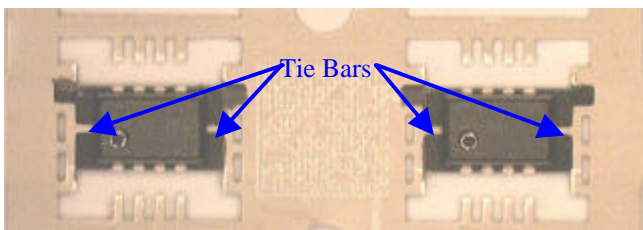


Figure 2b: Magnified view of the above. All 8 leads are isolated on each 3.0 mm x 2.0 mm x 0.9 mm CSP, facilitating ATE testing in strip form.

As with leadframe-based packages, laminate-based packages are typically assembled in strip form. Laminate packages are now starting to migrate to strip testing. On some laminate package strip designs, the laminate plating process requires that each solder ball on each package is electrically shorted together to a common plating stub. Figures 3a & 3b show an example of a mini-Ball Grid Array (mBGA) strip where all the solder balls are shorted together. As with traditional leadframe strips, this laminate design ensures that ESD damage cannot occur during processing of the strip prior to the singulation of individual devices since all solder balls on each device are always at equipotential. During the singulation operation, ESD damage is not a potential issue as long as the strip and singulation tool are at the same potential.

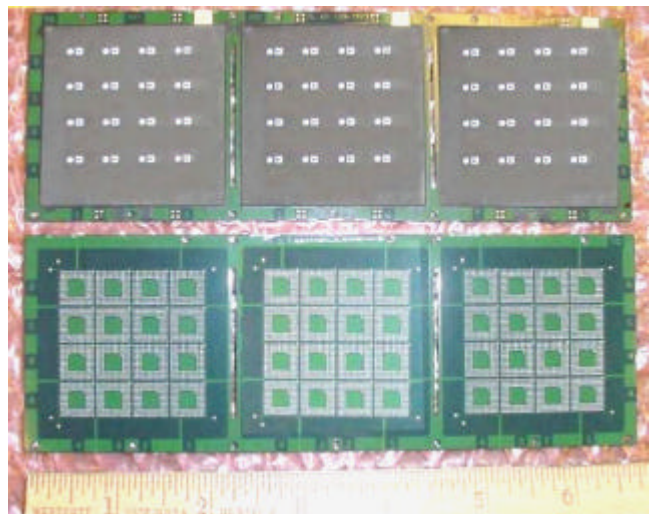


Figure 3a: Top & bottom views of 3 x (4 x 4) laminate strips of 109-ball mini-BGA packages.

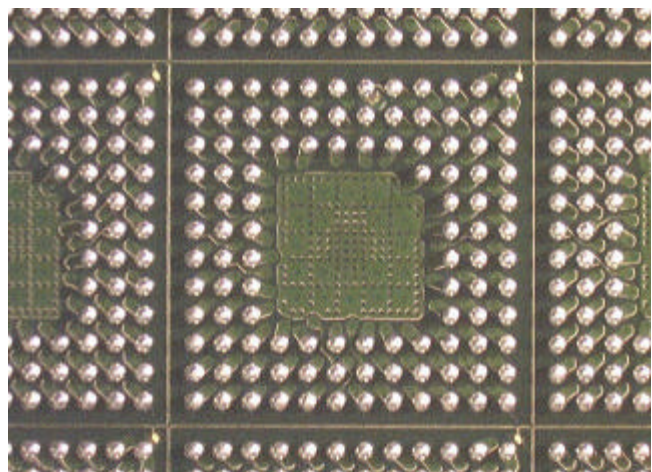


Figure 3b: Magnified view of the above. Although not optically apparent, all solder balls are shorted together prior to singulation of each 10 mm x 10 mm x 1.4 mm mini-BGA.

On other laminate package strip designs, the solder balls are not all shorted together. Figures 4a & 4b show an example of a Plastic Ball Grid Array (PBGA) strip where the solder balls are not shorted together. While this strip design is conducive for strip testing, it also makes the devices on each strip susceptible to ESD damage since the solder balls on each device are not always at equipotential.

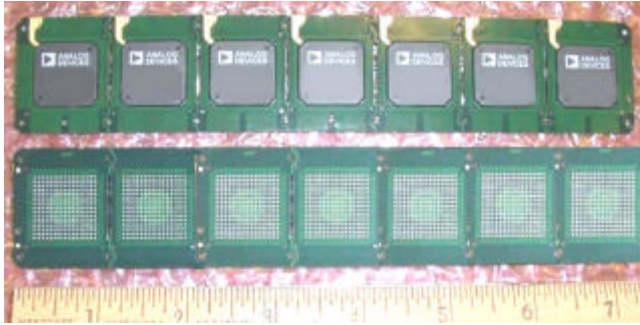


Figure 4a: Top and bottom views of 1 x 7 laminate strips of 225-ball PBGA packages.

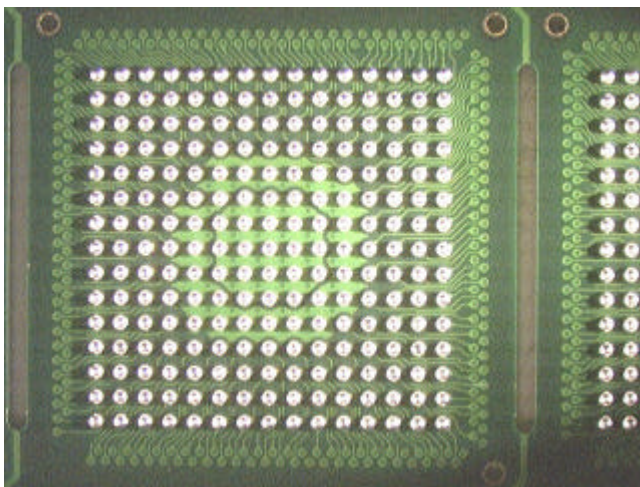


Figure 4b: Magnified view of the above. All solder balls are electrically isolated on each 23 mm x 23 mm x 2.3 mm PBGA.

II. Objectives of this Work

This work documents for the first time an enhanced discharge event for IC's packaged or tested in strip form, and a new test method which is not adequately described by existing CDM test standards. Using two unrelated case studies, this work:

- Describes a new ESD model (the CSM) and associated test method to simulate the damage seen on real-world IC failures in strip form as compared to single packaged devices;
- Discusses the relationship between device-level (CDM) and strip-level (CSM) ESD withstand voltages for a given product;

- Describes the relationship between strip capacitances and CSM withstand voltages for a given laminate strip design and a given leadframe strip design;
- Identifies permanent corrective actions for automated strip packaging and testing equipment to eliminate real-world CSM failures.

III. Real-World ESD Failures

III.a. Case Study 1

During 1999, several electrical test lots of a deep submicron CMOS DSP IC had a relatively high failure rate during handler-based ATE testing due to excessive tri-state I/O leakage ($>10 \mu\text{A}$). This DSP IC was available in two package styles: a leadframe-based Quad Flat Pack (QFP) and a laminate-based Plastic Ball Grid Array (PBGA). Interestingly, the leakage failures only occurred on the PBGA version, which was packaged and handled as a strip of 225-ball PBGA packages connected as a 1 x 7 laminate strip as shown in Figures 4a & 4b. Unlike the PBGA strip, the QFP strip had all pins shorted together by a common leadframe. Thus, the DSP IC's on the QFP strip were immune to ESD damage prior to singulation, while the same IC's on the PBGA strip were susceptible to ESD damage prior to singulation. After singulation of the seven devices on each PBGA strip, electrical testing was conducting using conventional single-site ATE testing. As an experiment, units from one PBGA lot were split, with hand testing conducted on half the units and standard handler-based testing conducted on the remaining units. Both splits had comparable leakage failure rates, confirming that the PBGA leakage failures occurred during processing in strip form prior to handler-based ATE testing.

Failure Analysis (FA) of samples of the DSP IC PBGA leakage failures revealed emission sites at the tips of several drain fingers of the large, identical MOS transistors within the I/O ESD protection circuitry. Subsequent de-processing showed that these leakage (emission) sites were due to ESD-induced silicon damage at the tips of the drain fingers (see Figure 5). This was unexpected since both the 225-ball PBGA and 240-lead QFP versions of this DSP IC were inherently highly robust to device-level ESD events, passing at least 3000V Human Body Model (HBM), 200V Machine Model (MM), and 1000V Charged Device Model (CDM) testing to the applicable ESDA standards.

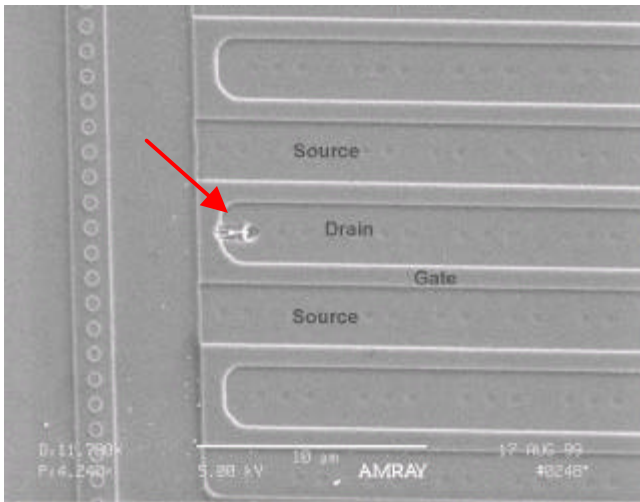


Figure 5: Scanning Electron Microscope (SEM) image of drain-to-well MOSFET junction damage on a real-world DSP IC PBGA leakage failure. Note: The sample was deprocessed to the silicon level and subjected to a brief decoration (Wright) etch.

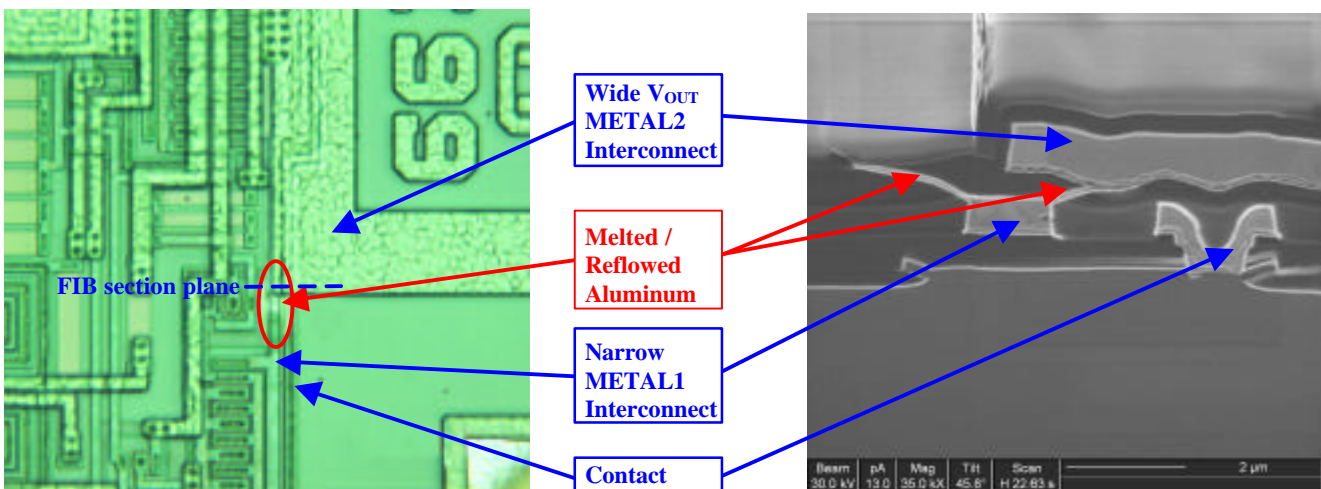
III.b. Case Study 2

In 2001, during the formal qualification process for a new strip test process for leadframe-based Chip Scale Packages (CSP's) as shown in Figures 2a & 2b, several 10 x 30 strips had a single non-functional device during QC electrical testing. The qualification vehicle was a 2.5 GHz logarithmic detector and controller (denoted the "RF IC") fabricated on a proprietary advanced junction-isolated bipolar process. This RF IC was previously only available in an 8-lead micro-SOIC package. Interestingly, electrical failures had never occurred during QC electrical testing on the high-volume micro-SOIC version. Unlike the CSP strip, the micro-SOIC strip had all pins shorted together by a common leadframe. Thus, similar to the

situation in Case Study 1, the RF IC's on the micro-SOIC strip were immune to ESD damage prior to singulation, while the same IC's on the CSP strip were susceptible to damage prior to singulation.

FA of two RF IC CSP QC failures revealed resistive shorts between the V_{OUT} and V_{POS} pins. This was caused by melted / reflowed aluminum at an enhanced electric field point at a corner of a METAL2 interconnect over a METAL1 interconnect, as shown in Figures 6a & 6b. Based on the severity of this damage, these failures were initially suspected to be due to ATE-induced electrical overstress (EOS). However, other potential causes were subsequently explored since this RF IC had never had EOS problems in the micro-SOIC package. Although ESD was considered a possibility, this product was inherently robust to device-level ESD events, passing at least 2000V HBM, 200V MM, and 1500V CDM testing in both the 8-lead CSP and the 8-lead micro-SOIC packages to the applicable ESDA standards. This was consistent with the FA history of no previous real-world ESD failures on this product.

Further review of the strip map QC test results for this CSP strip test qualification process unexpectedly showed that both RF IC failures occurred at the exact same DUT position on the 10 x 30 strip. Moreover, the failing DUT was one of the ten DUTs that was first contacted after the strip was advanced by the test chuck and then plunged to the ten contactors. This pointed to initial tester contact with the strip as the likely cause of the QC failures and, more specifically, to contactor-induced strip discharge (as opposed to EOS) as the root cause of failure.



Figures 6a & 6b: Top-down optical microscope (left photo) and corresponding Focused Ion Beam cross-sectional (right photo) images of the melted / reflowed aluminum on a real-world RF IC CSP failure.

IV. CSM Test Method Development

IV.a. Overview

The well-defined Charged Device Model (CDM) simulates a charged component discharging just before it comes in contact with a conductive object that is at or near ground potential. Detailed test methods [ESDA99], [JEDEC00] exist for conducting CDM testing using commercially-available systems. These test methods and systems were developed in terms of singulated components. In an attempt to duplicate the ESD damage documented in Case Studies 1 & 2, a Charged Strip Model (CSM) test environment was developed and implemented. The CSM simulates a charged strip of IC packages (either laminate-based or leadframe-based) discharging just before contact is made with a conductive object that is at or near ground potential. The CSM test methods that were developed varied based on the strip design and the pin counts of the packages. Since a strip of packaged IC's can be expensive, the test methods minimized the number of strips required while maximizing the useful information obtained from each strip.

For each case study, a KeyTek Verifier Robotic CDM test system was used to develop a new test method for strips. This test system has a field charging plate with a diameter of 127 mm (5") covered by a thin (13 μm) Mylar tape dielectric layer. This system conforms to [ESDA99] and produces discharge waveforms that pass waveform verification testing as described in [ESDA99] with both the 4 pF and 30 pF verification modules. Field-induced charging (rather than direct charging) was used since it was unclear if direct charging would be fully effective on laminate-based packages. For some strip sizes, the [ESDA99] 7:1 ratio requirement for charging plate area to component (strip) area was not met, but this was an inherent limitation of the existing commercial systems that are targeted for testing relatively small single components.

IV.b. Case Study 1

Since the complete 1 x 7 PBGA strip (measuring 35 mm x 188 mm) was larger than the field charging plate, Field-Induced Charged Strip Model (FICSM) testing on the full strip was not possible. Consequently, three strips from the same wafer fabrication and assembly lots were cut into four

smaller strips as follows: 1 x 1 (a singulated device); 1 x 2; 1 x 3; and 1 x 4. The 1 x 4 strip measured 35 mm x 107 mm, while the other strips were proportionally smaller.

The PBGA CSM test method was as follows:

1. The 1 x 4 PBGA strip was centered on the charging plate (see Figure 7).
2. Three I/O pins (solder balls) on the DSP IC device positioned over the center of the charging plate were FICSM tested at $\pm 100\text{V}$ consistent with the methodology in [ESDA99]. More specifically, the charging plate was set to +100V and then one I/O pin was discharged. This was repeated two more times. Then the charging plate was set to -100V and the same I/O pin was discharged. This was repeated two more times. This same six-discharges-per-pin sequence was conducted for two other I/O pins (solder balls) on the PBGA.
3. Using the same device, three new (untested) I/O pins on the same device were subjected to FICSM testing at $\pm 200\text{V}$.
4. This procedure was repeated on 54 additional I/O pins on the same device on the 1 x 4 strip, with three I/O's tested at $\pm 300\text{V}$; three I/O's tested at $\pm 400\text{V}$; and so on until the last group of three I/O's was tested at $\pm 2000\text{V}$.
5. Steps 1-4 were repeated on the three other cut strips. On the 1 x 3 strip, a total of 20 different I/O groups of three pins each were tested in 100V increments up to $\pm 2000\text{V}$. The same was done on the 1 x 2 strip, and finally likewise on the 1 x 1 singulated device.

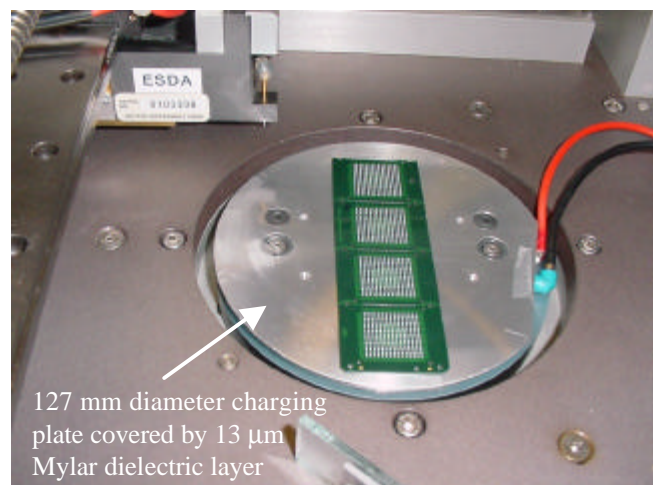


Figure 7: CSM test method setup for the 1 x 4 PBGA strip.

IV.c. Case Study 2

Since the complete 10 x 30 CSP strip (measuring 70 mm x 250 mm) was much larger than the field charging plate, FICSM testing on the full strip was not possible. Consequently, two strips from the same wafer fabrication and assembly lots were cut into ten smaller strips as follows: 1 x 10; 2 x 10; 3 x 10; ...; 10 x 10. The 10 x 10 strip measured 70 mm x 83 mm, while the other strips were proportionally smaller.

The CSP CSM test method was as follows:

1. The 10 x 10 CSP strip was centered on the charging plate (see Figure 8).
2. Each pin in-turn on the top-row, center-column RF IC device was FICSM tested at $\pm 100V$ consistent with the methodology in [ESDA99]. More specifically, the charging plate was set to +100V and then pin 1 was discharged. This was repeated two more times. Then the charging plate was set to -100V and pin 1 was discharged. This was repeated two more times. This same six-discharges-per-pin sequence was conducted for the other seven pins on the CSP.
3. Each pin in-turn on the 2nd-row, center-column device was subjected to FICSM testing at $\pm 200V$.
4. As indicated in Figure 8, this procedure was repeated on 18 additional devices on the 10 x 10 strip, with device #3 tested at $\pm 300V$; device #4 tested at $\pm 400V$; and so on until device #20 was tested at $\pm 2000V$.
5. Steps 1-4 were repeated on every other cut strip. (20 units on the 9 x 10 strip were tested in 100V increments; 20 units on the 8 x 10 strip were tested in 100V increments; and so on until 20 units on two separate 1 x 10 strips were tested in 100V increments up to $\pm 2000V$).

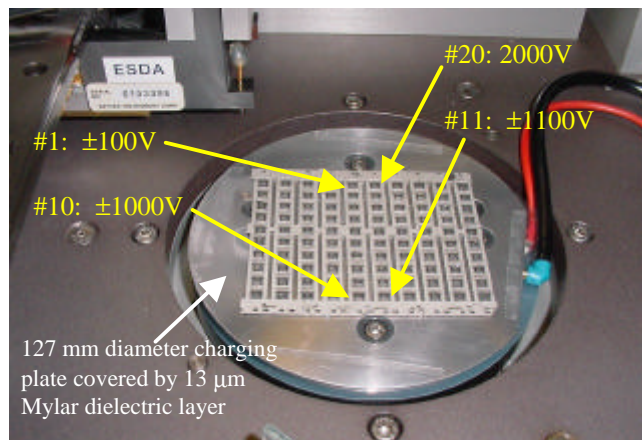


Figure 8: CSM test method setup for the 10 x 10 CSP strip.

V. CSM Test Results

V.a. Case Study 1

The four DSP IC PBGA strips (1 x 1; 1 x 2; 1 x 3; and 1 x 4) subjected to CSM testing were analyzed via extensive bench testing and curve tracer analysis. (Due to the non-standard size of the cut strips, ATE testing was not possible.) Regardless of the strip size, the first failure for excessive tri-state leakage ($>10 \mu A$) occurred at $\pm 1300V$. Thus, the CDM results (for the 1 x 1 device) were the same as the CSM results (for the three progressively larger strips). This result can be explained in terms of the relevant capacitances. The predominant capacitance during the PBGA CDM / CSM testing was the capacitance between the die substrate and the charging plate. Measurements of this capacitance showed it was consistently 30 pF, regardless of which PBGA on which strip was measured. This was due to the laminate design whereby all solder balls on each package are electrically isolated from other packages (Figure 4b).

Failure Analysis of the three I/O pins on the 1 x 1; 1 x 2; 1 x 3; and 1 x 4 PBGA strips subjected to $\pm 1300V$ CSM testing revealed consistent silicon damage (see Figure 9) on the tips of several drain fingers of the large, identical MOS transistors within the I/O ESD protection circuitry. This was the same failure mechanism and failure site as seen on the real-world PBGA strip failures (reference Figure 5) as well as the QFP and PBGA CDM failures. Thus, both CDM (singulated device) and CSM (multiple devices) testing produced the same results, successfully simulating the real-world CSM failures.

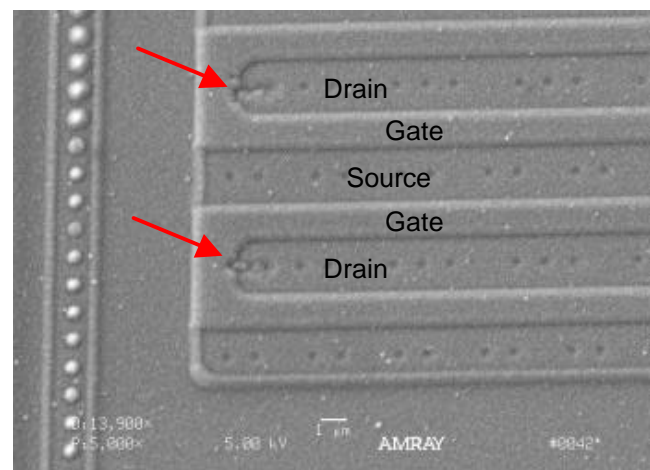


Figure 9: SEM image of drain-to-well MOSFET junction damage on a DSP IC PBGA leakage failure stressed at $\pm 1300V$ CSM. Note: The sample was deprocessed to the silicon level and subjected to a brief decoration (Wright) etch.

V.b. Case Study 2

The ten RF IC CSP strips (1 x 10; 2 x 10; 3 x 10; ...; 10 x 10) subjected to CSM testing were analyzed via extensive bench testing and curve tracer analysis. (Due to the non-standard size of the cut strips, ATE strip testing was not possible.) As expected, the CSM withstand voltage for the devices on a given strip decreased as the strip size / capacitance increased. More specifically, as shown in Figure 10, the CSM withstand voltage for excessive input leakage ($>10 \mu\text{A}$ at 3.3V) was $\pm 2000\text{V}$ on the 2 x 10 strip, but only $\pm 1000\text{V}$ on the 10 x 10 strip. This result can be explained in terms of the relevant capacitances. The predominant capacitance during the CSP testing was the capacitance between the die paddles / tie bars / leadframe and the charging plate. Measurements of this capacitance showed it was directly proportional to the strip size (see Figure 10), with the strip capacitance of the 10 x 10 strip (13 pF) measuring ten times that of the 1 x 10 strip (1.3 pF). This was due to the leadframe design whereby each CSP die paddle is connected by the same metal leadframe to every other CSP die paddle on the strip (Figure 2b).

Although the graph in Figure 10 shows an inverse linear relationship between the strip size and the CSM withstand voltage, this relationship cannot be used to accurately predict the CSM withstand voltage for the 10 x 30 strip that had real-world QC failures. As the strip continues to increase in size, the resistance of the metal leadframe becomes increasingly important, as will be discussed in Section VIII. Consequently, while the FICSM withstand voltage will continue to

decrease with increasing strip size, the rate at which the withstand voltage drops will slow, with this voltage approaching some asymptotic value as strip size continues to increase. Unfortunately, due to the physical limitations of the charging plate size on commercial CDM systems, CSM testing could not be conducted on CSP strips larger than 10 x 10. Thus, it was not possible to determine the FICSM withstand voltage for devices on the full 10 x 30 CSP strip used during production ATE strip testing.

On the nine CSP strips with devices failing in the $\pm 1100\text{V}$ to $\pm 2000\text{V}$ CSM range, FA revealed silicon junction damage (see Figure 11) on the ESD protection diodes for the input pins with excessive leakage. However, even on the 10 x 10 CSP strip stressed at $\pm 2000\text{V}$ CSM, the output pin showed no leakage. Consequently, CSM testing was conducted from $\pm 2100\text{V}$ to $\pm 3000\text{V}$ on the output pins on different devices on a new 10 x 10 CSP strip. FA of the output pins showed resistive shorts between the V_{OUT} and V_{POS} pins for devices stressed above $\pm 2100\text{V}$, with the value of the resistive short approximately matching that of the QC failures at $\pm 2900\text{V}$. These resistive shorts were caused by melted / reflowed aluminum at an enhanced electric field point at a corner of a METAL2 interconnect over a METAL1 interconnect, as shown in Figures 12a & 12b. This was the same failure mechanism and failure site as seen on the real-world CSP strip failures (reference Figures 6a & 6b). Thus, this CSM testing perfectly simulated the real-world strip failures.

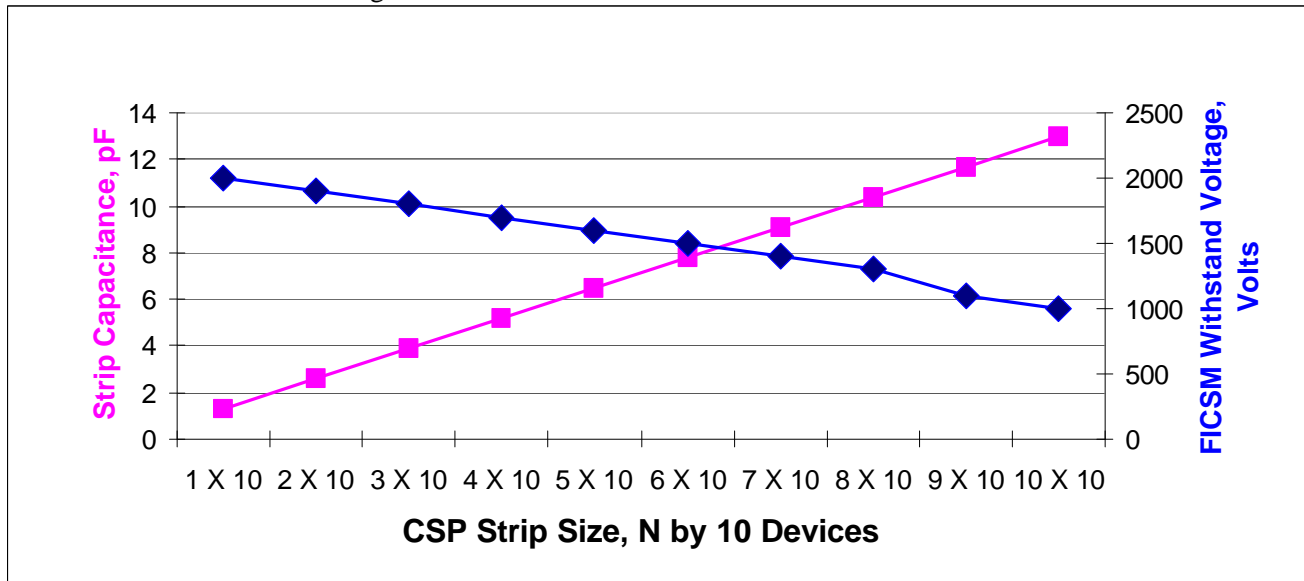


Figure 10: RF IC CSP measured strip capacitance and FICSM withstand voltage as a function of strip size.

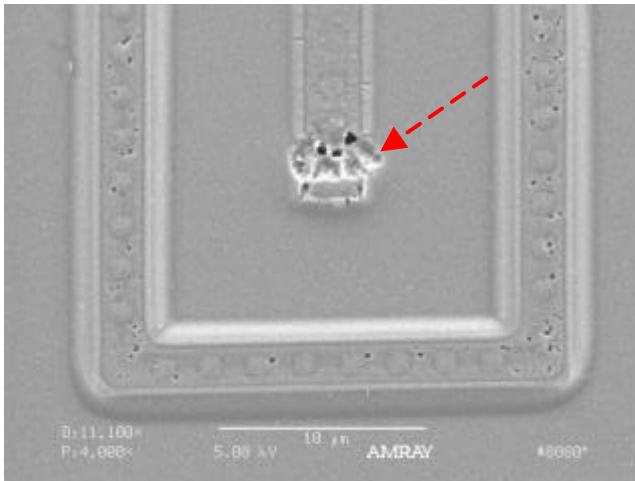
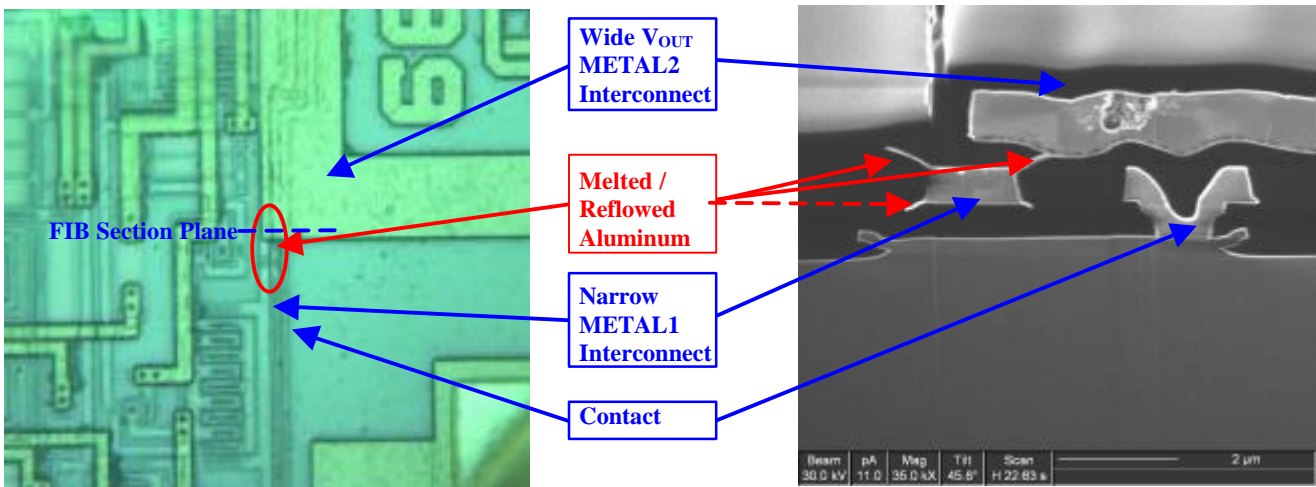


Figure 11: SEM image (upper left photo) of typical junction damage around the P+ diffusion contacts to the ESD protection diodes of RF IC leakage failures stressed above the FICSM withstand voltages shown in Figure 10. Note: This sample was deprocessed to the silicon level and subjected to a brief decoration (Wright) etch.

VI. Case Study Summaries

Table 1 summarizes the real-world ESD failures and the corresponding Field-Induced Charged Strip Model (FICSM) and Field-Induced Charged Device Model (FICDM) results for the two unrelated products used as case studies.



Figures 12a & 12b: Top-down optical microscope (left photo) and corresponding Focused Ion Beam cross-sectional (right photo) images of the melted / reflowed aluminum on an RF IC 10 x 10 CSP failure stressed at $\pm 2900V$ CSM.

Table 1: Case Study summaries

Case Study	Package	Real-World ESD Failure Mode & Mechanism	FICSM ESD Failure Mode & Mechanism	FICSM Charging Voltage to Replicate Real-World Failures	FICDM Charging Voltage to Replicate Real-World Failures
1. DSP IC	225-ball PBGA	On a 1 x 7 strip, excessive I/O tri-state leakage due to MOSFET drain-to-well junction damage (Figure 5)	On strips, excessive I/O tri-state leakage due to MOSFET drain-to-well junction damage (Figure 9)	$\pm 1300V$ (regardless of strip size)	$\pm 1300V$
2. RF IC	8-lead CSP	On a 10 x 30 strip, resistive short between V_{OUT} & V_{POS} due to melted / reflowed aluminum (Figures 6a & 6b)	On a 10 x 10 strip, resistive short between V_{OUT} & V_{POS} due to melted / reflowed aluminum (Figures 12a & 12b)	$\pm 2900V$ (10 x 10 strip)	Unknown (Beyond $\pm 4000V$ test system capability)

VII. Elimination of Real-World Failures

VII.a. Case Study 1

An investigation of the DSP IC PBGA strip processing showed that the PBGA strip marking (branding) operation was the most likely source of the ESD damage shown in Figure 5. While the QFP version of this product could also be subjected to high static fields during the strip marking operation, the leadframe design (with all pins shorted together) ensured that ESD damage could not occur prior to device singulation. High static charges measured during the strip marking operation were due to non-optimized ionizer placement. As a corrective action, the ionizers were permanently positioned much closer to the strips during the marking operation. Since this corrective action was taken in February 2001, no DSP IC PBGA lots have had significant tri-state leakage failure rates.

VII.b. Case Study 2

Bellmore [Bellmore01] considers the ESD environment of the automated device handler as a major contributor to charge buildup within a tested electronic component. A review of the RF IC strip test system revealed that the test chuck was designed to keep the strip-under-test electrically isolated from the handler ground. This design was intended to provide an optimal configuration for ATE testing. However, this design allowed significant charge to build up on the strip, especially during long test chuck movements. Therefore, the strip discharged when plunged to the tester pogo pin contactors that were initially at handler ground potential.

An examination of the tester pogo pin contactors revealed that one contactor (corresponding to the V_{OUT} pin of device 5 of the first row of 10 devices parallel tested on the strip) was slightly elevated off the normal plane of the remaining contactor pogo pins. This one pogo pin thus consistently made contact with the V_{OUT} pin of device 5 before the other contactor pogo pins, causing the full charge stored on the ~ 39 pF 10×30 CSP strip to be discharged through this pin. On the QC failures, this resulted in the severe ESD damage shown in Figures 6a & 6b.

Subsequent analysis showed that the RF IC ATE testing was not affected if the strip-under-test was electrically connected to the handler ground. Thus, the corrective action was simple: The test chuck was

redesigned to provide a constant metallic path to the handler ground while the strip was moving (Figure 13), thus preventing the metal strip from charging. The effectiveness of this corrective action was proven by subsequent testing of hundreds of thousands of RF IC packages in strip form with no QC electrical failures (0 PPM).

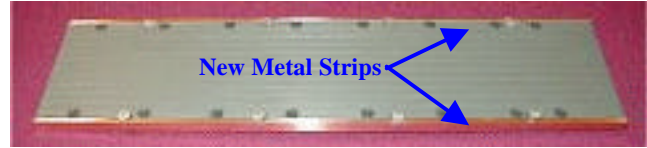


Figure 13: Redesigned test chuck showing new metal strips along edges to provide a path to handler ground.

VIII. Discussion of Results

Real-world failures and CSM simulation results show that leadframe packages ATE tested in strip form after electrically isolating the leads are highly susceptible to CSM discharge events. As indicated in Table 1 Case Study 2, CSM discharges at the strip level are more severe than CDM discharges at the singulated device level. More specifically, CSM discharges result in melted / reflowed aluminum on the RF IC strip, while CDM discharges did not result in any damage on the singulated version of the RF IC, even when stressed up to ± 4000 V.

This is a serious issue; it shows that even products with excellent single-package CDM results may suffer CSM yield loss due to automated strip handling if steps are not taken to ensure that no strip charging / discharging occurs in the manufacturing / testing environment.

One of the capacitances that charges up during an automated CDM charging event is the pin-to-package capacitance [Lee00]. Additional capacitances are the pin-to-leadframe capacitances and the package-to-leadframe capacitances. With the RF IC strip, the die attach paddles on all packages were connected together via tie bars and the common leadframe. Thus, the total package-to-charging plate capacitance approximates the sum of all the individual package-to-charging plate capacitances.

However, there is a series resistance of the leadframe connection between a zapped package and all the other packages that are charged on the strip. As a result, the effective RC delay from each package's package-to-leadframe capacitance to the discharge pin of a particular package varies by distance. Figure 14 shows this simplified strip model.

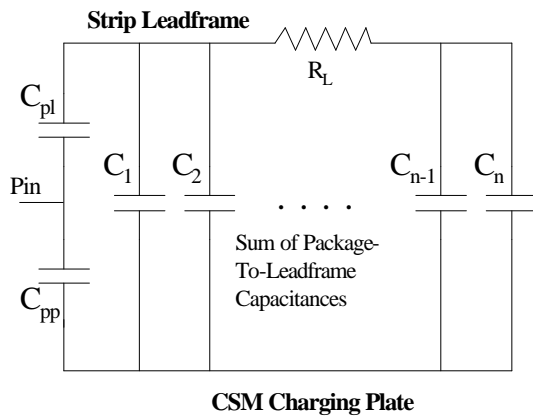


Figure 14: Simplified Strip – Package Capacitances schematic.

C_1 through C_n represent the charging-plate-to-leadframe capacitances of each package in the strip. Capacitance C_{pl} represents the simplified effective capacitance from the zapped pin to the strip leadframe. Capacitance C_{pp} represents the simplified effective capacitance from the zapped pin to the CSM charging plate. Resistor R_L is an effective resistance that should be viewed as the leadframe resistance between the zapped package and any other package on the strip. This resistance is a variable and varies with distance from the zapped package.

The net effect of this circuit is an extended duration capacitive discharge, with the peak current range lasting longer due to the delay from the resistance component across the leadframe capacitance matrix. The discharge peak current lasts for a longer time in

FICSM mode than for single-device FICDM mode, possibly up to 1 ns for the 10 x 30 strip, compared to the 100 ps time frame of FICDM peak current.

To illustrate this, oscilloscope measurements of discharges from a 4 pF CDM verification module; a 1 x 10, 8-lead CSP strip; and a 10 x 10, 8-lead CSP strip (reference Figure 8) were compared. These 500V discharge waveforms are shown in Figure 15 as three reconstructed waveforms in a plot from a Tektronix TDS694C oscilloscope (3 GHz BW, 10 Gsample/sec sampling rate).

The positive-going first peak area of the discharge waveform is longer in duration (around 400 ps) for the 10 x 10 CSP strip compared to less than 100 ps for the 4 pF verification module and slightly over 200 ps for the 1 x 10 CSP strip. Although the observed ~100 ps rise time value for the 4 pF verification module has been reported to be due to an artifact of the module design, and ~200-400 ps rise times have been measured on actual packaged devices [Henry96] [Henry99], the peak current is markedly higher and the duration of the peak current is significantly longer for the 10 x 10 CSP strip.

One unexpected result from these waveforms is the decrease in the magnitude of the second (i.e., negative) peak with the CSP strip discharge compared to the first (i.e., positive) peak. Upon review, however, this is not surprising. As the sum of the package-to-leadframe capacitances increases relative to the single-package capacitance, this summed capacitance begins to dominate the discharge, and contributes more

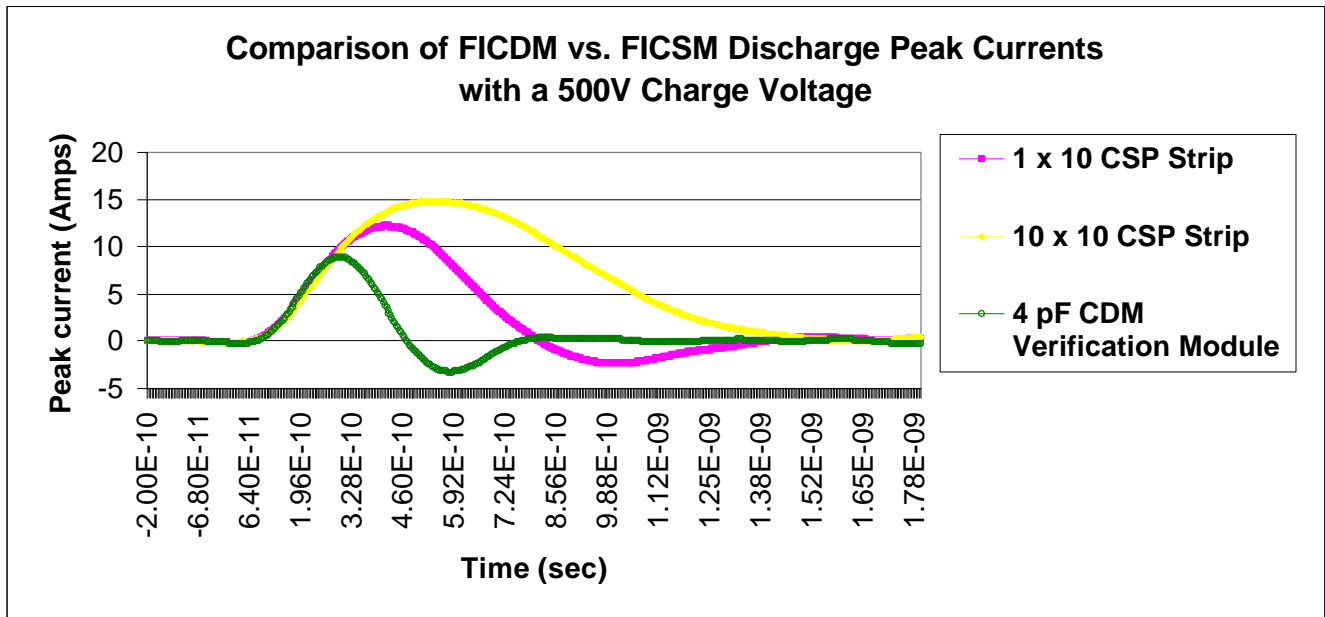


Figure 15: Comparison of FICDM vs. FICSM discharge peak currents showing enhanced FICSM strip discharge.

positively to the total peak current. This, we believe, is a characteristic of CSM discharges that is not reflected in the CDM standards, and may warrant review by an ESD Association committee in the future.

This increase in CSM discharge energy shifts the energy profile further along the Wunsch-Bell curve in terms of damage effects. At higher peak current I , the total time required to reach an EOS level of energy E would be less than that for lower peak currents, from the relation $E \approx V * I * \text{time}$. This explanation is consistent with the failure signatures (EOS-like damage) documented in Case Study 2 for both real-world and simulated CSM discharge events.

It was not possible to perform CSM testing on the full 10 x 30 RF IC strip due to the size of the charging plate on the CDM tester. However, from the oscilloscope waveforms, it is clear that an even higher and longer duration first peak CSM discharge occurs, with a nearly negligible negative-going second peak. This would shift the positive energy level further along the Wunsch-Bell curve. Thus, the CSM withstand voltage would further decrease, and failure modes that could be mistaken for EOS would become more evident.

With the DSP IC PBGA strip, the CSM withstand voltage of devices assembled in strip form did not appreciably differ from the single-device CDM results. This was because, unlike with the CSP strip, no electrical connection existed between the individual packages that comprised the PBGA strip. Thus, CSM damage occurred with the same failure mode and mechanism as with the CDM damage. The relative severity of the observed junction damage is attributed to the relatively high package capacitance (30 pF) of each 225-ball PBGA.

Work is ongoing to determine if a strip device's susceptibility to discharge damage can be estimated based on the corresponding single-package CDM results along with measurements of the strip capacitance relative to the single-package capacitance.

IX. Recommendations

Based on these results, it is recommended that IC manufacturers review their strip designs and automated handling procedures for both leadframe-based and laminated-based packages. While the PBGA strip that was the subject of Case Study 1 had a laminate design that made the strip no more susceptible to ESD damage than a singulated package, other

laminate designs exist where this is not the case. For example, if the die attach paddles for laminate-based packages are interconnected at the strip level, devices on strips will be much more susceptible to ESD damage than singulated devices. In terms of leadframe-based devices that are tested in strip form, it is extremely important to implement optimal measures to prevent strip charging and discharging. It is recommended that an ESD Association committee be chartered with reviewing existing guidelines for preventing ESD damage to determine if they are sufficient for safeguarding strip processing. Finally, as part of the package development and electrical characterization processes, package assembly foundries and semiconductor companies involved in strip-level manufacturing should pay close attention to the strip package-to-leadframe capacitances.

X. Conclusions

An enhanced discharge mechanism, introduced here as the Charged Strip Model (CSM), has been disclosed and documented for the first time. This new ESD model simulates a charged strip of IC packages (either laminate-based or leadframe-based) discharging just before contact is made with a conductive object that is at or near ground potential. Key findings / conclusions from this work are as follows:

1. Using a commercial CDM test system, CSM test methods have been developed that are highly effective at simulating real-world CSM failures.
2. To improve ATE test throughput, the semiconductor industry is rapidly transitioning to strip testing for both leadframe and laminate packages. Real-world CSM failures will therefore increase unless proper safeguards are taken against this new ESD threat.
3. Leadframe-based devices ATE tested in strip form are much more susceptible to ESD damage before singulation than after singulation. For a given charge voltage, such strips are subjected to a much higher energy level CSM discharge than their single-package counterparts subjected to a CDM discharge. This is due to the much higher capacitance of a strip than a single package.
4. Some IC failures that the semiconductor industry historically attributed to EOS were probably due to the CSM. However, since this model was not previously described, previous CSM failures would not be recognized as such.

5. Before attributing IC failures to EOS, the possibility of CSM ESD damage should be explored. As appropriate, CSM testing should be conducted to simulate real-world IC damage.
6. For strip-tested leadframe devices, CSM withstand voltages decrease as strip sizes (i.e., strip capacitance) increase. Devices that are effectively immune to CDM damage at the singulated package level may be highly susceptible to CSM damage at the strip level. Given the relatively large capacitance of strips, on-chip ESD protection methodologies will probably never be adequate to completely protect IC's from CSM damage. One area of possible future work is to develop on-strip protection methodologies.
7. The key to eliminating real-world CSM failures is to implement controls to ensure that strip charging does not occur. For a device with a relatively low CDM withstand voltage, the corresponding CSM withstand voltage for a large strip may be much less than 100V. Consequently, traditional environmental safeguards against CDM damage may be insufficient.
8. Existing commercial CDM test systems are not adequate for conducting CSM testing of large strips. Future generations of such test systems should include larger charging plates (both circular and rectangular) and modified vacuum / hold-down systems to facilitate CSM testing.
9. The ESDA and JEDEC CDM standards [ESDA99, JEDEC00] do not describe the enhanced CSM discharge. The first peak discharge waveform is enhanced due to the increased sum of the package-to-leadframe capacitances, which can dominate the discharge. Consideration should be given to developing a formal CSM standard test method.

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