FEATURES

General-purpose PLL evaluation board excluding VCO, loop filter, and TCXO
Contains ADF4001 200 MHz frequency synthesizer IC
Accompanying software allows complete control of synthesizer functions from a PC

EVALUATION KIT CONTENTS

EV-ADF4001SD1Z board
CD that includes
  Self-installing software that allows users to control the board and exercise all functions of the device
  Electronic version of the ADF4001 data sheet
  Electronic version of the UG-092 user guide

ADDITIONAL EQUIPMENT

PC running Windows XP or more recent version
SDP-S board (system demonstration platform, serial only)
T-package VCO
0805 resistors and capacitors
Spectrum analyzer
Oscilloscope (optional)

DOCUMENTS NEEDED

ADF4001 data sheet

REQUIRED SOFTWARE

Analog Devices Int-N software (Version 7 or higher)
ADIsimPLL

GENERAL DESCRIPTION

This board is designed to allow the user to evaluate the performance of the ADF4001 frequency synthesizer for phase-locked loops (PLLs). Figure 1 shows the board, which contains the ADF4001 synthesizer, an SMA connector for the reference input, power supplies, and an RF output. There is also a footprint for a loop filter and a VCO on board.

The evaluation kit also contains software that is compatible with Windows® XP and later versions to allow easy programming of the synthesizer.

This board requires an SDP-S (system demonstration platform-serial) board (shown in Figure 1, but not supplied with the kit). The SDP-S allows software programming of the ADF4001 device.
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# REVISION HISTORY

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QUICK START GUIDE

Follow these steps to quickly evaluate the ADF4001 device:

1. Solder the VCO (T-package compatible).
2. Solder the loop filter components (design with ADIsimPLL™).
3. Connect the reference frequency to J11.
4. Install the system development platform (SDP) drivers.
5. Install the Int-N software.
6. Connect the SDP-S motherboard to the PC and to the EV-ADF4001SD1Z.
7. Follow the hardware driver installation procedure.
8. Connect the power supplies to banana connectors (6 V to 12 V).
9. Run the Int-N software.
10. Select the SDP board and the ADF4001 device in the Select Device and Connection tab of the software front panel window.
11. Click the Main Controls tab. Update all registers.
12. Connect the spectrum analyzer to J2.
13. Measure the results.
EVALUATION BOARD HARDWARE

The evaluation board requires the use of an SDP-S motherboard to program the device. This is not included and must be purchased separately. The EV-ADФ4001SD1Z schematics are shown in Figure 21, Figure 22, and Figure 23.

POWER SUPPLIES

The board is powered from external banana connectors. The voltage can vary between 6 V and 12 V. The power supply circuit provides 3.0 V or 5 V to the ADФ4001 VDD and allows the user to choose either 3.0 V or 5 V for the ADФ4001 Vf. The default settings are 3.0 V for the ADФ4001 VDD and 5 V for the ADФ4001 Vf. Note that VDD should never exceed 5.5 V. This can damage the device.

External power supplies can be used to directly drive the device. In this case, the user must insert SMA connectors as shown in Figure 2.

INPUT SIGNALS

The necessary reference input can be sourced from an external generator. A low noise, high slew rate reference source is best for achieving the stated performance of the ADФ4001. This reference source can be connected to Connector J11. If preferred, the edge mount connector, J5, can be inserted and used instead. A third option is to solder a footprint-compatible TCXO to Footprint Y2. To use this option, connect 0 Ω links to R16 and R14.

Digital SPI signals are supplied through the SDP connector, J1. Using the SDP-S platform is recommended. The SDP_B can also be used, but Resistor R57 must be removed on the SDP-B board. Some additional spurious low frequencies may appear if the SDP-B connector is used.

OUTPUT SIGNALS

All components necessary for LO generation can be inserted on board. The PLL is made up of the ADФ4001 synthesizer, a passive loop filter, and the VCO. The package containing the VCO must be a T-package (or similar). A low-pass filter must be inserted between the charge pump output and the VCO input. In this case, the user must insert the relevant parts as shown in Figure 2. The VCO output is available at RFOUT through a standard SMA connector, J2. The MUXOUT signal can be monitored at Test Point T8 or at SMA Connector J3.
DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This board is shipped without a TCXO, low-pass filter, or a VCO. Users must insert suitable components to complete a PLL. Link positions are outlined in Table 1.

Table 1. Link Positions and Function

<table>
<thead>
<tr>
<th>Link</th>
<th>Position</th>
<th>Options</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>A</td>
<td>R1A</td>
<td>Not used</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>RSET</td>
<td>Normal operation</td>
</tr>
<tr>
<td>LK2</td>
<td>A</td>
<td>GND</td>
<td>Hardware power-down</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>VDD</td>
<td>Normal operation</td>
</tr>
<tr>
<td>LK3</td>
<td>(Vco)</td>
<td>A</td>
<td>5 V</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>3 V</td>
<td>Normal operation (5 V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Normal operation (3 V)</td>
</tr>
<tr>
<td>LK4</td>
<td>(Vcvo)</td>
<td>A</td>
<td>5 V</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>3 V</td>
<td>VCO supply (5 V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VCO supply (3 V)</td>
</tr>
<tr>
<td>LK5</td>
<td>(Vf)</td>
<td>A</td>
<td>5 V</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>3 V</td>
<td>Vf supply (5 V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vf supply (3 V)</td>
</tr>
</tbody>
</table>

SYSTEM DEMONSTRATION PLATFORM (SDP)

The system demonstration platform (SDP) is a series of controller boards, interposer boards, and daughter boards that can be used for easy low cost evaluation of Analog Devices, Inc., components and reference circuits. It is a reusable platform whereby a single controller board can be reused in various daughter board evaluation systems.

Controller boards connect to the PC via USB 2.0 and provide a range of communication interfaces on a 120-pin connector. The pinout for this connector is strictly defined. This 120-pin connector's receptacle is on all SDP daughter boards, component evaluation boards, and Circuits from the Lab reference circuit boards. There are two controller boards in the platform: the SDP-B, which is based on the Blackfin® ADSP-BF527, and the SDP-S, which is a serial interface only controller board. The SDP-S has a subset of the SDP-B functionality.

Interposer boards route signals between the SDP 120-pin connector and a second connector. When the second connector is also a 120-pin connector, the interposer can be used for signal monitoring of the 120-pin connector signals. Alternatively, the second connector allows SDP platform elements to be integrated into a second platform, for example, the BeMicro SDK. More information on the SDP can be found at www.analog.com/sdp.
SOFTWARE INSTALLATION
Use the following steps to install the SDP drivers and Int-N software.

1. Install the SDP drivers by double-clicking SDPDrivers.exe and following the relevant installation instructions. See the UG-291 for further instructions on installation of the SDP-S platform or the UG-277 if the SDP-B platform is used.

2. Install the Analog Devices Int-N software by double-clicking ADI_Int-N_Setup.msi.
   If you are using Windows XP, follow the instructions in the Windows XP Software Installation Guide section (see Figure 3 to Figure 7).
   If you are using Windows Vista or Windows 7, follow the instructions in the Windows Vista and Windows 7 Software Installation Guide section (see Figure 8 to Figure 12).
   Note that the software requires Microsoft Windows Installer and Microsoft .NET Framework 3.5 (or higher).
   The installer connects to the Internet and downloads Microsoft .NET Framework automatically. Alternatively, before running ADI_Int-N_Setup.msi, both the installer and .NET Framework can be installed from the CD provided.

3. Connect your SDP board (black) or USB adapter board (green) by USB. If you are using an SDP board, the drivers install automatically, and you are ready to run the software. If you are using a USB adapter board on Windows XP, follow the steps in the Windows XP Driver Installation Guide section (see Figure 13 to Figure 16). On Windows Vista or Windows 7, the drivers install automatically.

Windows XP Software Installation Guide

![Figure 3. Windows XP Int-N Software Installation, Setup Wizard](image3.png)

1. Click Next.

![Figure 4. Windows XP Int-N Software Installation, Select Installation Folder](image4.png)

2. Choose an installation directory and click Next.
3. Click Next.

4. Click Continue Anyway.

5. Click Close.
3. Click **Next**.

4. Click **Install**.

5. Click **Close**.

---

**Windows XP Driver Installation Guide**

1. Choose **Yes, this time only** and click **Next**.

2. Click **Next**.

   Note that Figure 14 may list *Analog Devices RFG.L Eval Board* instead of *ADF4xxx USB Adapter Board*.
3. Click **Continue Anyway**.

4. Click **Finish**.
EVALUATION BOARD SOFTWARE

The control software for the EV-ADF4001SD1Z accompanies the EV-ADF4001SD1Z on a CD. To install the software, see the Software Installation section.

To run the software, click the ADI PLL Int-N file on the desktop or in the Start menu.

On the Select Device and Connection tab, choose your device and your connection method, and click Connect.

Confirm that SDP board connected, ADF4xxx USB Adapter Board connected, or Analog Devices RFG.L Eval Board connected is displayed at the bottom left of the window (see Figure 17). Otherwise, the software has no connection to the evaluation board.

Note that, when connecting the board, it takes about 5 sec to 10 sec for the status label to change.

Under the File menu, the current settings can be saved to, and loaded from, a text file.

![Figure 17. Software Front Panel Display—Select Device and Connection](image-url)
The **Main Controls** tab controls the PLL settings (see Figure 18). Use the **Reference Frequency** text box to set the correct reference frequency and the reference frequency divider. The default reference on the software window is at 10 MHz.

Use the **RF Settings** section to control the output frequency. You can type the desired output frequency in the **RF VCO Output Frequency** text box (in megahertz).

In the **Registers** tab, you can manually input the desired value to be written to the registers.

In the **Sweep and Hop** tab, you can make the device sweep a range of frequencies or hop between two set frequencies. In the **Latches/Registers** section at the bottom of the window, the values to be written to each register are displayed. If the background on the text box is green, the value displayed is different from the value actually on the device. Click **Write R CounterLatch** or **Write N Counter Latch** to write that value to the device.

![Figure 18. Software Front Panel Display—Main Controls](image-url)
EVALUATION AND TEST
To evaluate and test the performance of the ADF4001, use the following procedure:

1. Ensure that a VCO and loop filter are inserted on the board. Use ADIsimPLL to generate the loop filter component values.

2. Install the SDP-S software drivers. Connect the evaluation board to a PC using the supplied USB cable. Follow the hardware driver installation procedure that appears.

3. Connect the SDP-S connector to the EV-ADF4001SD1Z.

4. Connect a reference signal to J11 (or J5, if an edge mount connector is inserted).

5. Connect a spectrum analyzer to Connector J2.

6. Run the Int-N software.

7. Select the SDP board and the ADF4001 device in the Select Device and Connection tab of the software front panel window.

8. In the software window, set the VCO center frequency (Figure 19 uses a 200 MHz VCO). Set the PFD frequency as defined in ADIsimPLL, and program the reference frequency to equal that supplied to Connector J11 (or the TCXO). See Figure 20 for the suggested setup.

9. Measure the output spectrum. Figure 19 shows a 200 MHz output.
EVALUATION BOARD SCHEMATICS AND ARTWORK

Figure 21. Evaluation Board Schematic (Page 1)
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Figure 23. Evaluation Board Schematic (Page 3)
### BILL OF MATERIALS

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<tr>
<th>Reference Designator</th>
<th>Part Description</th>
<th>Manufacturer/Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C3</td>
<td>Capacitor, 0805</td>
<td>User supplied</td>
</tr>
<tr>
<td>C4, C6, C10</td>
<td>Capacitor, 0402, 0.1 μF, 16 V</td>
<td>AVX CM105X7R104K16AT</td>
</tr>
<tr>
<td>C5, C7, C9, C11, C13</td>
<td>Capacitor, 0603, 10 pF, 50 V, SMD</td>
<td>AVX 0603S100JAT2A</td>
</tr>
<tr>
<td>C8, C12</td>
<td>Capacitor, Case A, 1 μF, 50 V</td>
<td>AVX TJA105K016R</td>
</tr>
<tr>
<td>C14, C15</td>
<td>Capacitor, 0603, 1 nF, 50 V</td>
<td>AVX 0603C103JAT2A</td>
</tr>
<tr>
<td>C16, C17, C18, C19</td>
<td>Capacitor, 0603, 100 pF, 50 V</td>
<td>AVX TJA475K010R</td>
</tr>
<tr>
<td>C20, C23</td>
<td>Capacitor, 0603, 1 nF, 50 V</td>
<td>AVX 0603C103JAT2A</td>
</tr>
<tr>
<td>C21, C24</td>
<td>Capacitor, Case A, 4.7 μF, 10 V</td>
<td>AVX TJA475K010R</td>
</tr>
<tr>
<td>C22, C25</td>
<td>Capacitor, 0603, 10 nF, 50 V</td>
<td>AVX 0603C103JAT2A</td>
</tr>
<tr>
<td>C26, C27</td>
<td>Capacitor, 0603, 10 nF, 50 V</td>
<td>AVX 0603C103JAT2A</td>
</tr>
<tr>
<td>D1</td>
<td>LED, green</td>
<td>OSRAM LGR971-Z</td>
</tr>
<tr>
<td>D2</td>
<td>Diode, DO41, 1 A, 50 V</td>
<td>Multicomp 1N4001</td>
</tr>
<tr>
<td>D3, D5</td>
<td>SD103C, 6.2 V</td>
<td>ON Semiconductor MBR0520LT1G</td>
</tr>
<tr>
<td>D4</td>
<td>LED, red</td>
<td>Avago HSMS-C170</td>
</tr>
<tr>
<td>J1</td>
<td>120-way connector, 0.6 mm pitch</td>
<td>Hirose FX8-120S-SV(21)</td>
</tr>
<tr>
<td>J2</td>
<td>Jack, SMA, SMA_EDGE</td>
<td>Johnson Components 142-0701-851</td>
</tr>
<tr>
<td>J3, J4, J10</td>
<td>Jack, SMA, receptacle straight PCB</td>
<td>Not inserted</td>
</tr>
<tr>
<td>J5, J6, J7, J8, J9</td>
<td>Jack, SMA, receptacle straight PCB</td>
<td>Not inserted</td>
</tr>
<tr>
<td>J11</td>
<td>Jack, SMA, receptacle straight PCB</td>
<td>PONOMA 72963</td>
</tr>
<tr>
<td>LK1, LK3, LK4, LK5</td>
<td>Jumper-2\SIP3, Link-3P</td>
<td>Harwin M20-9990345 and M7566-05</td>
</tr>
<tr>
<td>GND</td>
<td>Black 4 mm banana socket</td>
<td>Harwin M20-9990245 and M7566-05</td>
</tr>
<tr>
<td>VSUPPLY</td>
<td>Red 4 mm banana socket</td>
<td>Deltron 571-0100-01</td>
</tr>
<tr>
<td>R1A</td>
<td>Resistor, 0805</td>
<td>Deltron 571-0500-01</td>
</tr>
<tr>
<td>R1</td>
<td>Resistor, 0805</td>
<td>User supplied</td>
</tr>
<tr>
<td>R2</td>
<td>Resistor, 0805</td>
<td>User supplied</td>
</tr>
<tr>
<td>R3</td>
<td>Resistor, 0805, 5.1 kΩ, ±1%, 0.1 W</td>
<td>Multicomp MC 0.1 0805 1% 5K1</td>
</tr>
<tr>
<td>R4, R5, R6, R23, R29, R42</td>
<td>Resistor, 0603, 330 Ω</td>
<td>Multicomp MC 0.063W 0603 1% 330R</td>
</tr>
<tr>
<td>R7, R8, R9</td>
<td>Resistor, 0603, 18 Ω</td>
<td>Multicomp MC 0.063W 0603 1% 18R</td>
</tr>
<tr>
<td>R10, R17</td>
<td>Resistor, 0603, 51 Ω</td>
<td>Multicomp MC 0.063W 0603 1% 51R</td>
</tr>
<tr>
<td>R11</td>
<td>Resistor, 0603, 100 Ω</td>
<td>Multicomp MC 0.0625W 0402 1% 100R</td>
</tr>
<tr>
<td>R12, R13, R24, R25, R26</td>
<td>Resistor, 0603, 10 kΩ</td>
<td>Multicomp MC 0.063W 0603 1% 10K</td>
</tr>
<tr>
<td>R14, R16, R18, R28, R36</td>
<td>Resistor, 0603, 0 Ω</td>
<td>Multicomp MC 0.063W 0603 1% 0R</td>
</tr>
<tr>
<td>R15, R22, R27, R32, R33, R37, R46</td>
<td>Resistor, 0603, 0 Ω</td>
<td>Not inserted</td>
</tr>
<tr>
<td>R19, R20</td>
<td>Resistor, 0603, 330 kΩ, ±1%, 0.063 W</td>
<td>Multicomp MC 0.063W 0603 1% 330K</td>
</tr>
<tr>
<td>R21</td>
<td>Resistor, 0603, 4.7 kΩ, ±1%, 0.063 W</td>
<td>Multicomp MC 0.063W 0603 1% 4K7</td>
</tr>
<tr>
<td>R30</td>
<td>Resistor, 0402</td>
<td>Not inserted</td>
</tr>
<tr>
<td>R31, R34</td>
<td>Resistor, RC31, 0402, 100 kΩ</td>
<td>YAGEO (Phycomp) RC0402JR-07100KL</td>
</tr>
<tr>
<td>S1</td>
<td>Switch, PCB, SPDT, 20 V</td>
<td>APEM TL36P0050</td>
</tr>
<tr>
<td>T1 to T14</td>
<td>Test point, PCB, red PK, 100</td>
<td>Vero 20-313137</td>
</tr>
<tr>
<td>U1</td>
<td>ADF4001, 16-lead TSSOP</td>
<td>ADF4001BRUZ</td>
</tr>
<tr>
<td>U3</td>
<td>ADP3300, 6-lead SOT-23</td>
<td>ADP3300ART-5</td>
</tr>
<tr>
<td>U2</td>
<td>ADP3300, 6-lead SOT-23</td>
<td>ADP3300ART-3</td>
</tr>
<tr>
<td>U4</td>
<td>32k FC serial EEPROM, MSOP8</td>
<td>Microchip 24LC32A-I/MS</td>
</tr>
<tr>
<td>Y1</td>
<td>VCO19V-XXXXXT</td>
<td>Not inserted</td>
</tr>
<tr>
<td>Y2</td>
<td>Low profile/temperature compensated crystal oscillator, OSC_TCXO, 10 W</td>
<td>Not inserted</td>
</tr>
</tbody>
</table>

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## RELATED LINKS

<table>
<thead>
<tr>
<th>Resource</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADF4001</td>
<td>Product Page, 200 MHz Clock Generator PLL</td>
</tr>
<tr>
<td>ADP3300</td>
<td>Product Page, High Accuracy anyCAP® 50 mA Low Dropout Linear Regulator</td>
</tr>
</tbody>
</table>
I2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement.

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