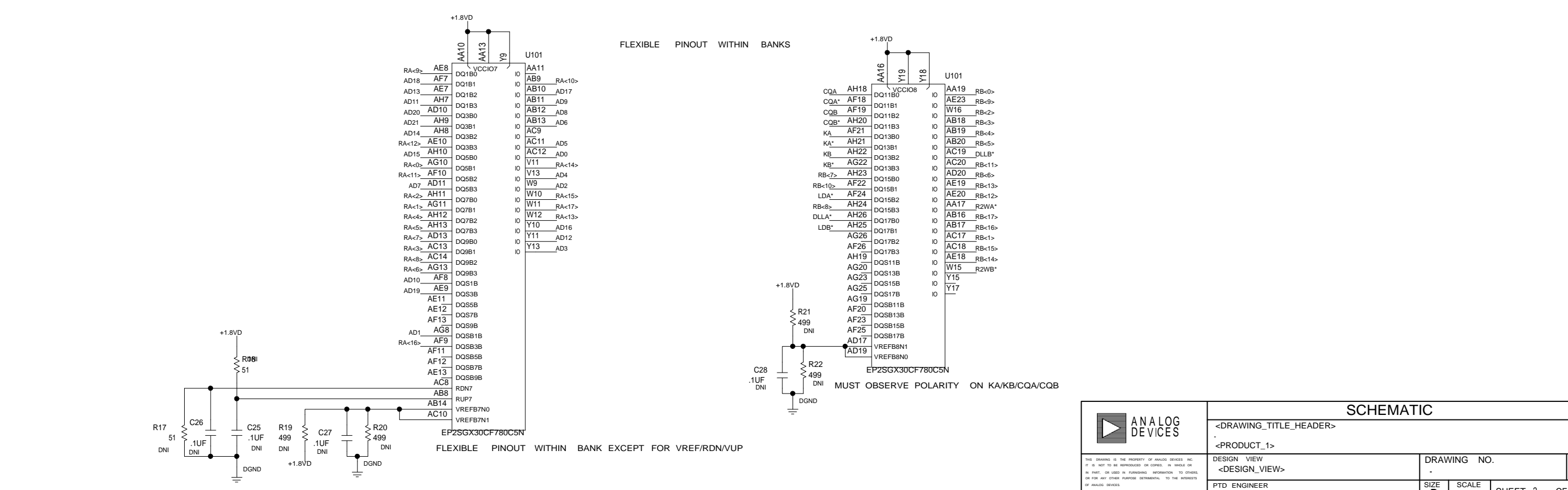
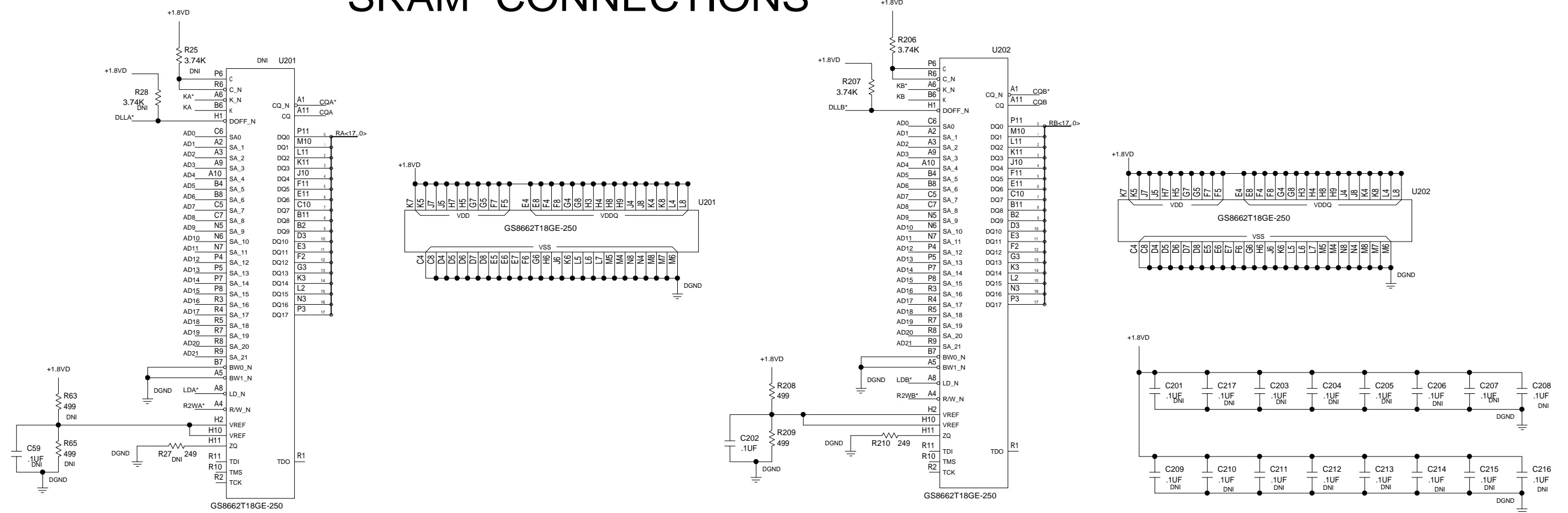


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SRAM CONNECTIONS



FLEXIBLE PINOUT WITHIN BANKS

FLEXIBLE PINOUT WITHIN BANK EXCEPT FOR VREF/RDN/VUP

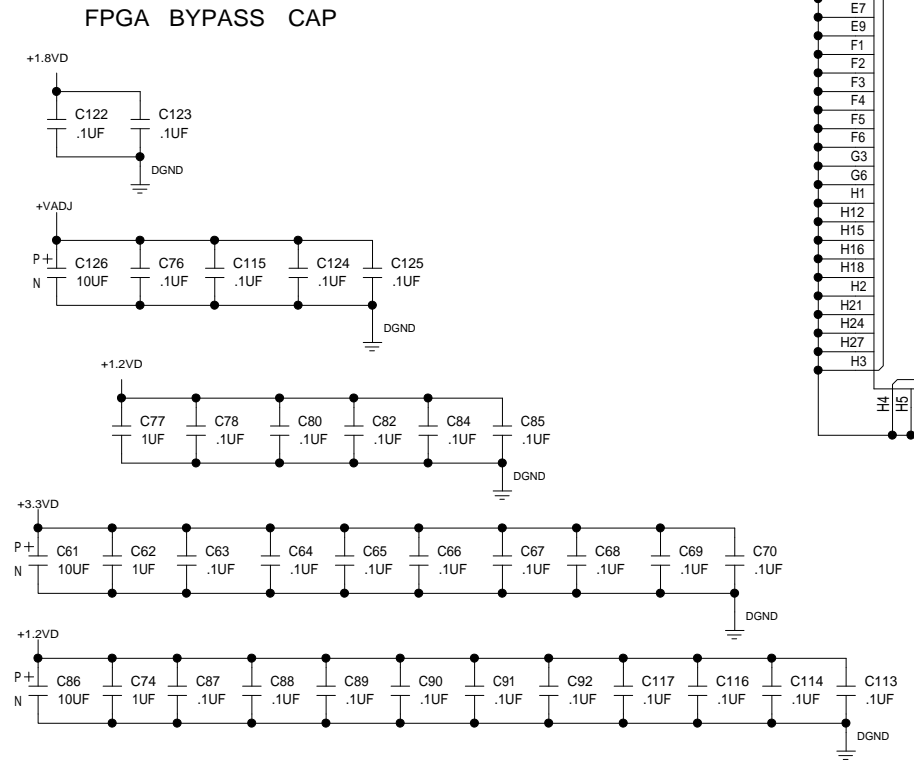
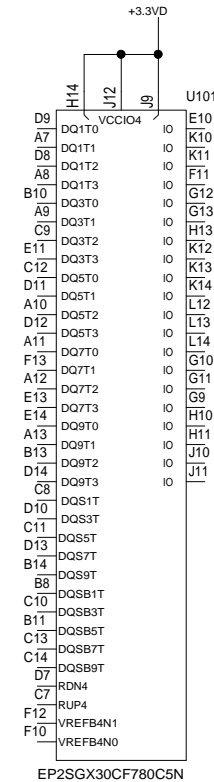
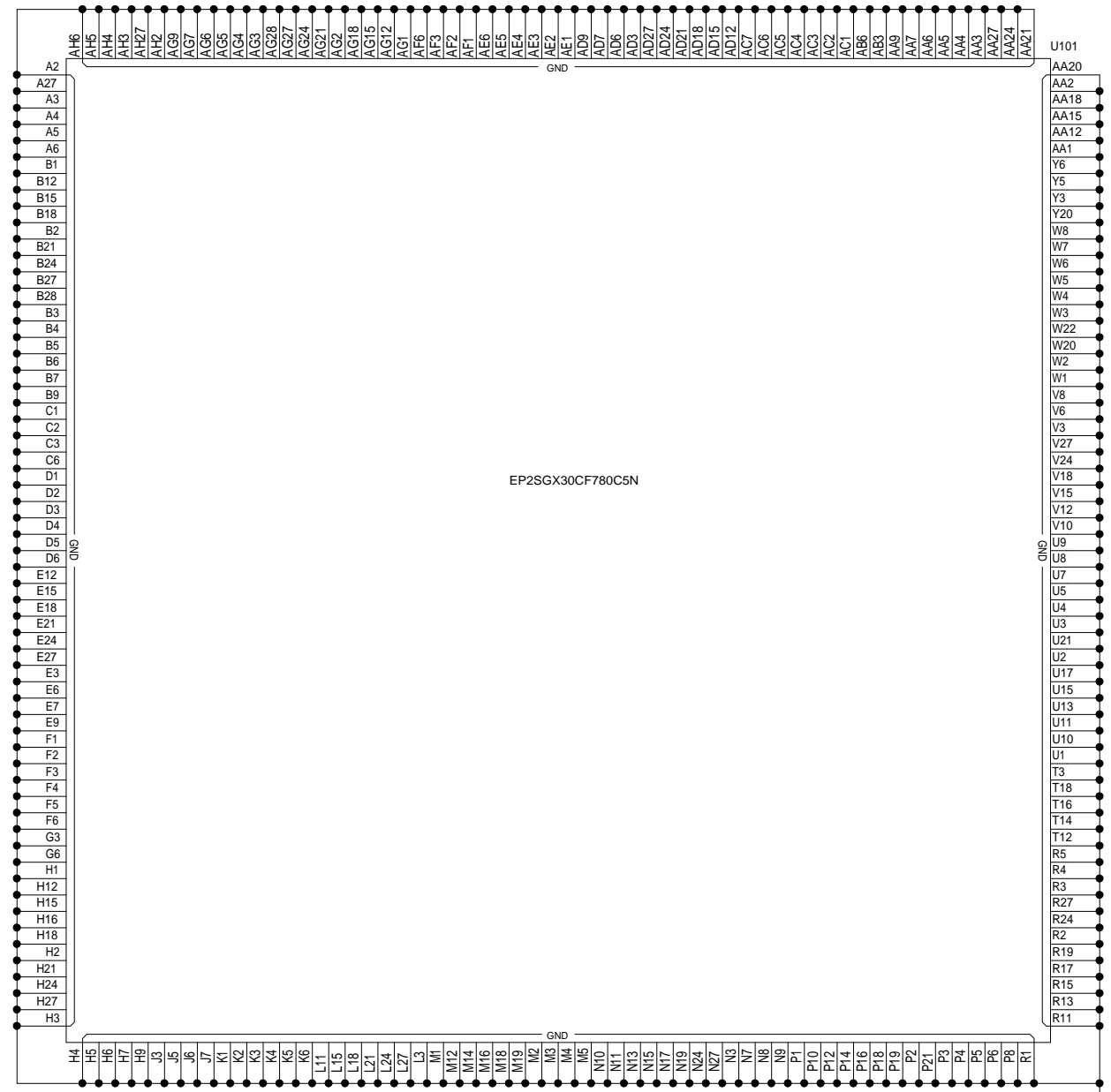
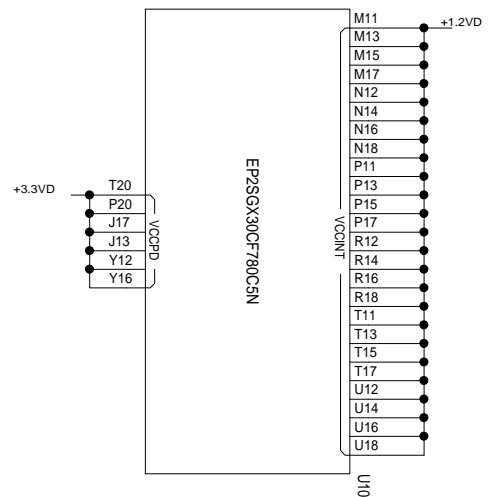
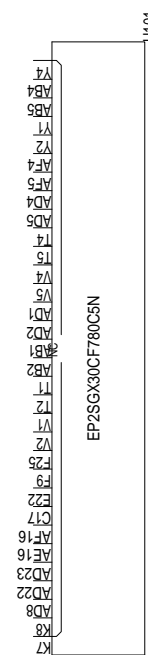
MUST OBSERVE POLARITY ON KA/KB/CQA/CQB

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FPGA POWER AND DECOUPLING

COPY DUT FOOTPRINT FROM ALTERA EVAL BOARD

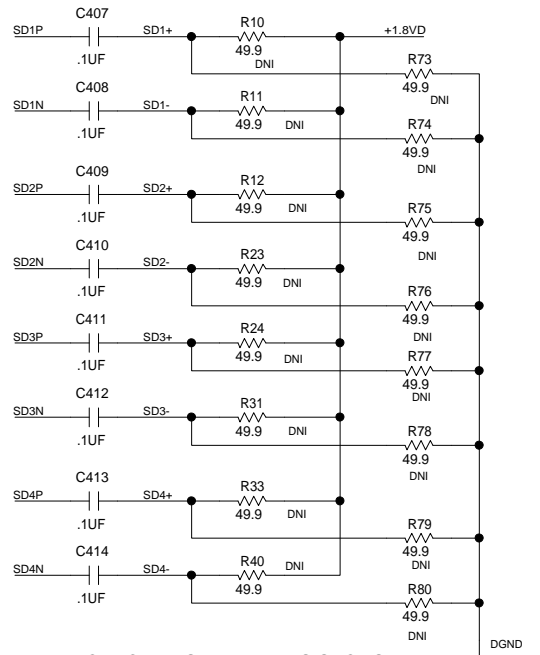
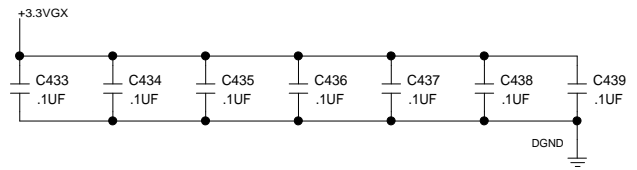
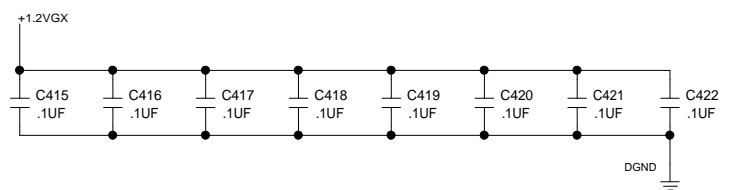
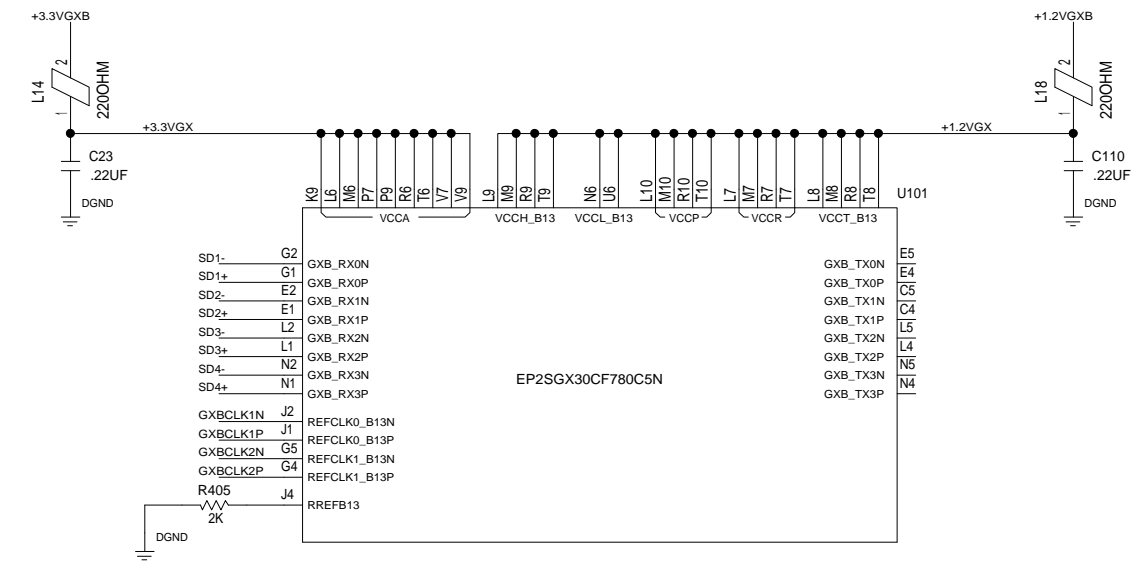
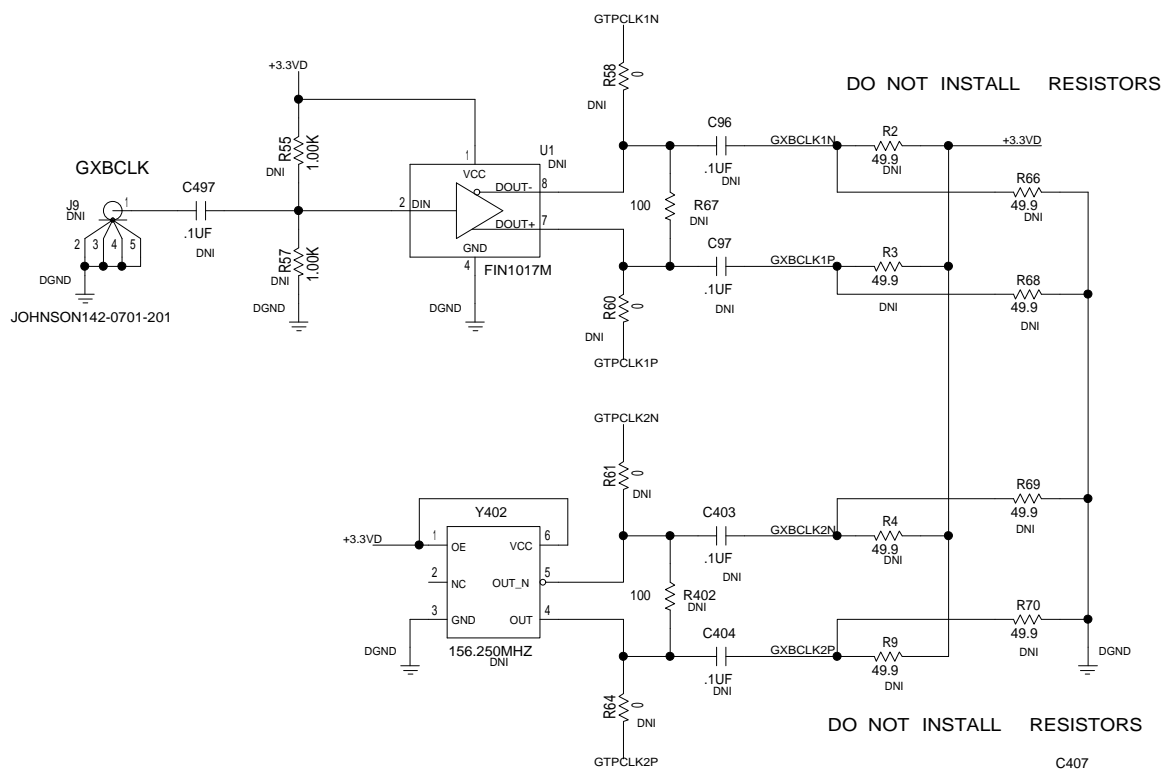
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REV	DESCRIPTION	DATE	APPROVED

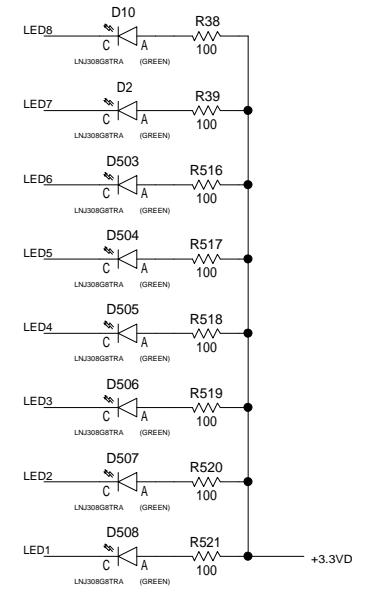
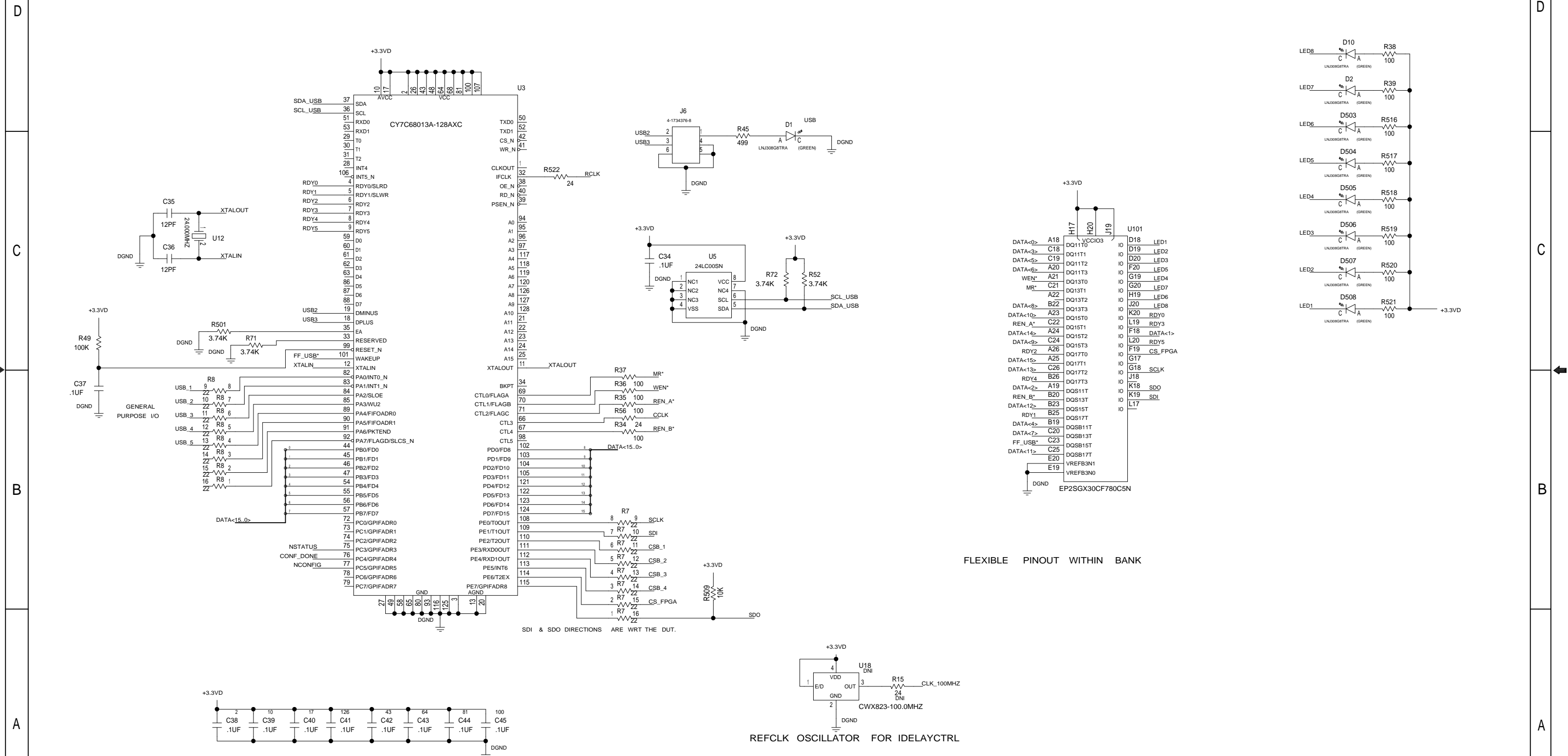
GXB CONNECTIONS



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REVISIONS			
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USB CONNECTIONS

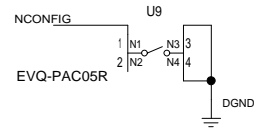
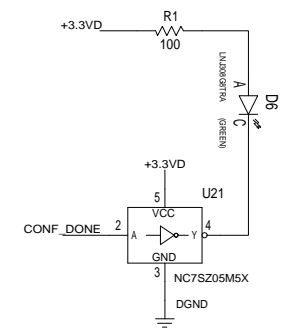
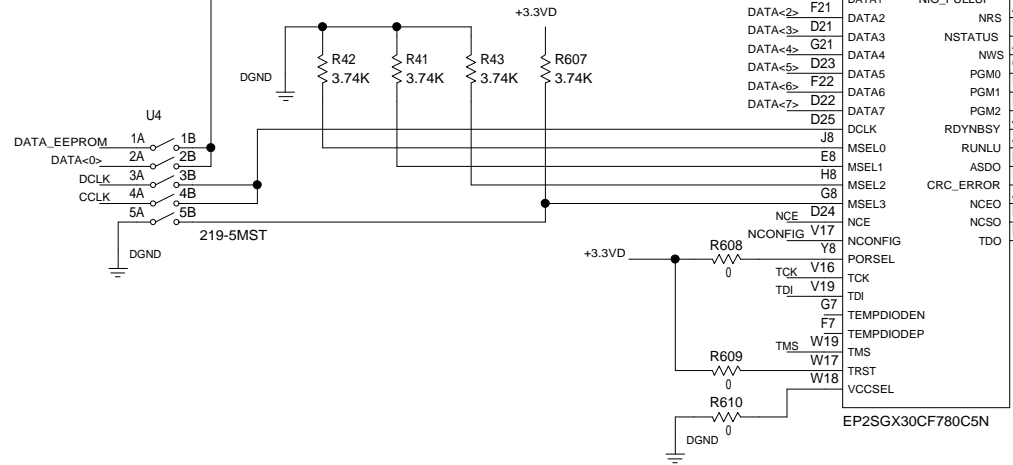
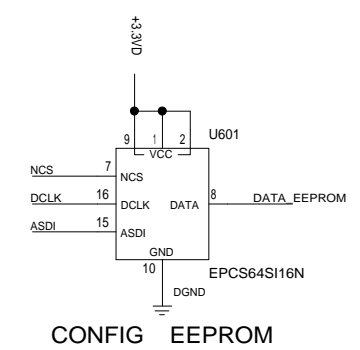
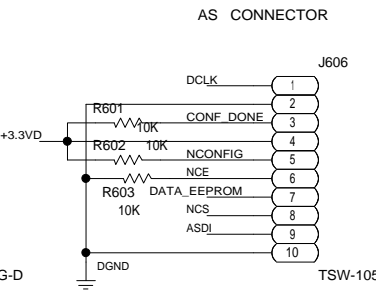
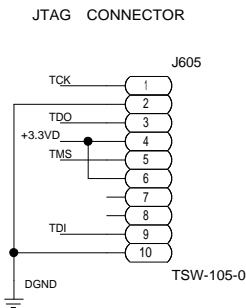
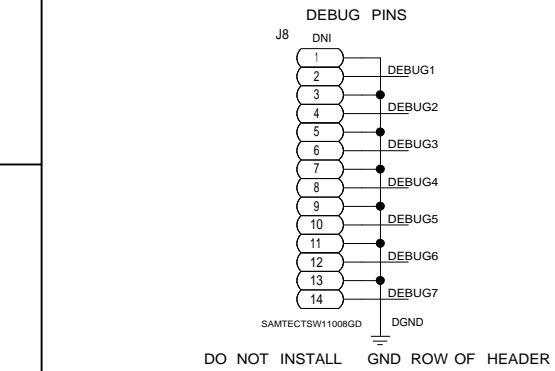
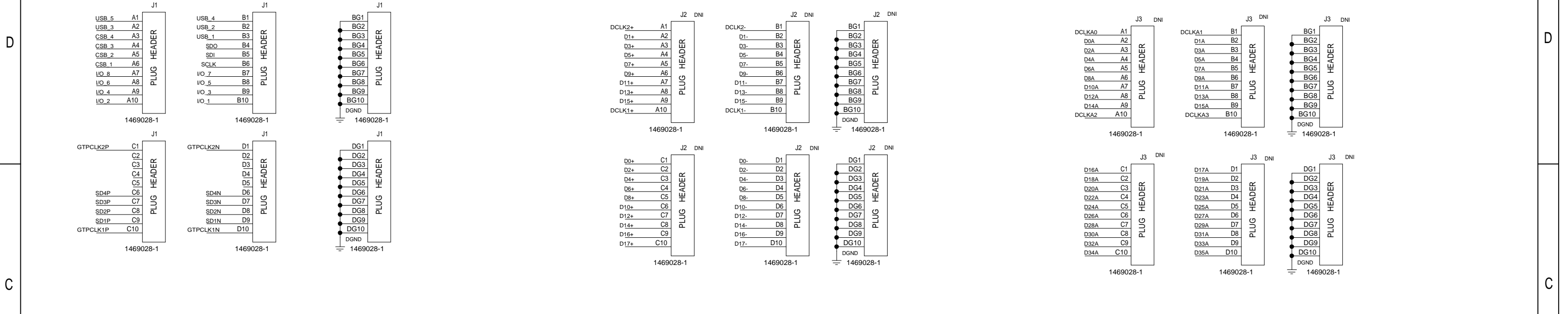


IC Pin	Signal	IC Pin	Signal
A18	DATA<0>	DQ11T0	D18 LED1
C18	DATA<3>	DQ11T1	D19 LED2
C19	DATA<5>	DQ11T2	D20 LED3
A20	DATA<6>	DQ11T3	F20 LED5
A21	WEN*	DQ13T0	G19 LED4
C21	MR*	DQ13T1	G20 LED7
A22	DATA<8>	DQ13T2	H19 LED6
B22	DATA<10>	DQ13T3	J20 LED8
A23	DATA<14>	DQ15T0	K20 RDY3
A24	DATA<14>	DQ15T1	F18 DATA<1>
C24	DATA<9>	DQ15T2	L20 RDY5
A26	RDY2	DQ15T3	F19 CS_FPGA
A25	DATA<15>	DQ17T0	G17
C26	DATA<13>	DQ17T1	G18 SCLK
B26	RDY4	DQ17T2	J18
A19	DATA<2>	DQ17T3	K18 SDO
A19	DATA<2>	DQS11T	K19 SDI
B20	REN_B*	DQS13T	L17
B23	DATA<12>	DQS15T	
B25	RDY1	DQS17T	
B19	DATA<4>	DQS17T	
C20	DATA<7>	DQS11T	
C23	FF_USB*	DQS13T	
C25	DATA<11>	DQS15T	
E20		DQS17T	
E19		VREFB3N0	

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TYCO AND MISC FPGA CONNECTIONS

REVISIONS			
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