
















**Job: 6 Layer (Analog Devices)**  
**Revision: 1**  
**Engr: mthiel**

**Laminate Type** Isola 370HR  
**Minimum Tg** 0  
**Min Td** 0  
**MOT** 0  
**PLC Code** 0  
**T260 Min** 0  
**T288 Min** 0  
**Slash Sheet**  
**Laminate Color** Natural

**Customer: Multicircuits**  
**Part No.:**  
**Part Rev:**

Layer	Thickness (Inch)	Stackup Picture	Family	Description	Type
compmask	0.0010		SM-Std	SM-Std	
compside	0.0019		Cu-Std	.5 + Std	comp - Cu-Std
	0.0056		FR4	1080	
			FR4	1080	
layer2	0.0012		Cu-Std	1	plane_t
	0.0050		FR4	.005	
layer3	0.0012		Cu-Std	1	plane_b
	0.0086		FR4	2113	
			FR4	2116	
	0.0140		FR4	.014	
	0.0086		FR4	2116	
			FR4	2113	
layer4	0.0012		Cu-Std	1	plane_t
	0.0050		FR4	.005	
layer5	0.0012		Cu-Std	1	plane_b
	0.0056		FR4	1080	
			FR4	1080	
solderside	0.0019		Cu-Std	.5 + Std	solder - Cu-Std
soldermask	0.0010		SM-Std	SM-Std	

**0.0630 Total Expected Thickness**

**0.0590 After Lamination +0.0059 -0.0059**

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### Requirements Information in Inch

Top Layer	Bottom Layer	Required Thickness	Tol +	Tol -	Calculated Thickness
Incl.Plating		0.0620	0.0062	0.0062	0.0612
After Lamination		0.0590	0.0059	0.0059	0.0586

### Comments

### Concise Impedance Constraint Information Line Widths inInch

#	Impedance Type Name	Picture	Aff Layer	Designed Width	Plotted Width	Cntr to Cntr	Ref Planes	Target ohms	Predicted ohms
1	Surface MS		compside None	0.0085	0.0085		None layer2	50 +/- 5.0	50.28
2	EC Microstrip		compside None	0.005	0.005	0.01	None layer2	100 +/- 10.0	99.84
3	Surface MS		solderside None	0.0085	0.0085		None layer5	50 +/- 5.0	50.28
4	EC Microstrip		solderside None	0.005	0.005	0.01	None layer5	100 +/- 10.0	99.84