ANALOG DEVICES

Evaluation Board for the
High Performance 10-Bit Display Interface
AD9981/PCB

FEATURES

Two analog input connectors for RGB or YPbPr input

**Separate, low-noise regulators for each AD9981 power
domain (VD, VDD, and PVD)**

**100-pin interface connector provides 5 V input and
AD9981 outputs (syncs, clock, and data)**

APPLICATIONS

**For evaluation of AD9981 as part of the
AD9981 evaluation kit**

**Can also be adapted to end-user evaluation platform
using the 100-pin interface connector**

PACKAGE CONTENTS

AD9981 evaluation board
10-bit display interface board (AD998xEB)
DEPL evaluation software including preset files
DEPL evaluation board documentation
5 V power supply
USB and parallel port cables

PRODUCT DESCRIPTION

The purpose of the AD9981 evaluation board is both to
demonstrate the performance of the AD9981 and to serve as an
implementation example for design and layout. To aid in real-
world evaluation, it was designed so that it could be connected
as easily as possible into another PC board, such as a graphics
controller board.

This board is for IC device evaluation purposes only. Analog
Devices does not recommend using this hardware outside of
this stated usage. Further, Analog Devices provides no warran-
ties for use of this equipment beyond the scope of IC device
evaluation purposes.

REQUIREMENTS

The requirements to use the AD9981 evaluation board are a 5 V
power supply, graphics signals (through either of the 15-pin VGA
connectors), and a means to program the internal chip registers.
Hardware and software for programming the internal chip reg-
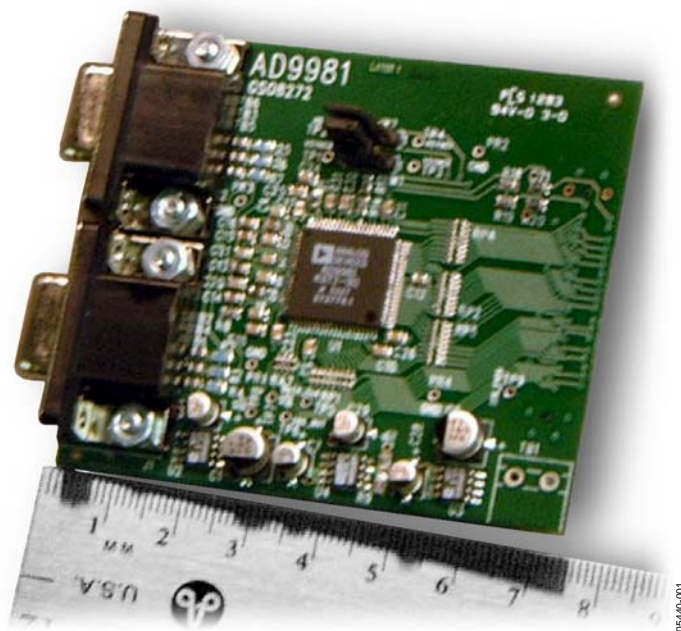ister are provided.

ANALOG FLAT PANEL INTERFACE BOARD

Figure 1. Board Shown in Centimeters

Rev. 0

AD9981/PCB

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REVISION HISTORY

3/05—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

TYPICAL CONFIGURATION

In most cases, this evaluation board is used to digitize analog RGB graphics signals and pass the data to another board. To do this, connect the graphics signals to the 15-pin VGA connector, supply 5 V to the board, and program the internal serial register. The digitized data, generated clock signals, and control signals are passed off the board through the right-side connector.

POWER

The AD9981 evaluation board contains two 3.3 V voltage regulators and an adjustable regulator set for 1.8 V. These regulators supply power to the AD9981. The three regulators provide power to the three power supplies on the AD9981 (refer to the AD9981 data sheet). The best performance can be obtained from the AD9981 when the analog supply (V_D) and the PLL (PV_D) supply have their own regulators separate from the primary 3.3 V supply (V_{DD}). The three regulators work nominally when supplied with 5 V, but work with a range of voltages. Power is applied to the board through the right-side connector (Pins 1–4 of J3). Typically, power is supplied from another board. In the AD9981 evaluation kit, 5 V is supplied by the 10-bit display interface board.

PROGRAMMING THE INTERNAL CHIP REGISTERS

Hardware and software for programming the AD9981 internal registers are provided. The hardware consists of a standard printer cable and a receiver chip located on the panel driver board. The programming signals come onto the AD9981 evaluation board through Pins 7 and 9 on Connector J3. The software is included on the installation CD and is described in the Evaluation Board Software section.

EVALUATION BOARD SOFTWARE

SETTTING UP THE SOFTWARE

The display electronics product line (DEPL) evaluation software is a Visual Basic® program requiring Windows® 95, or later. It is on a self-installing CD package included with the evaluation board. When performing the software install, always use the most recent Windows files (DLL or OCX, for example) if prompted by the install software (these files may already be on your system). The AD9882 register setup screen (similar to the DEPL Evaluation Software – AD9981 register setup window in Figure 2) should be displayed at program execution after a successful installation. The DEPL evaluation software can control any of the DEPL AD988x or AD998x devices. It can also read and write to the 10-bit display interface board and includes useful tools such as a PLL Divisor calculator.
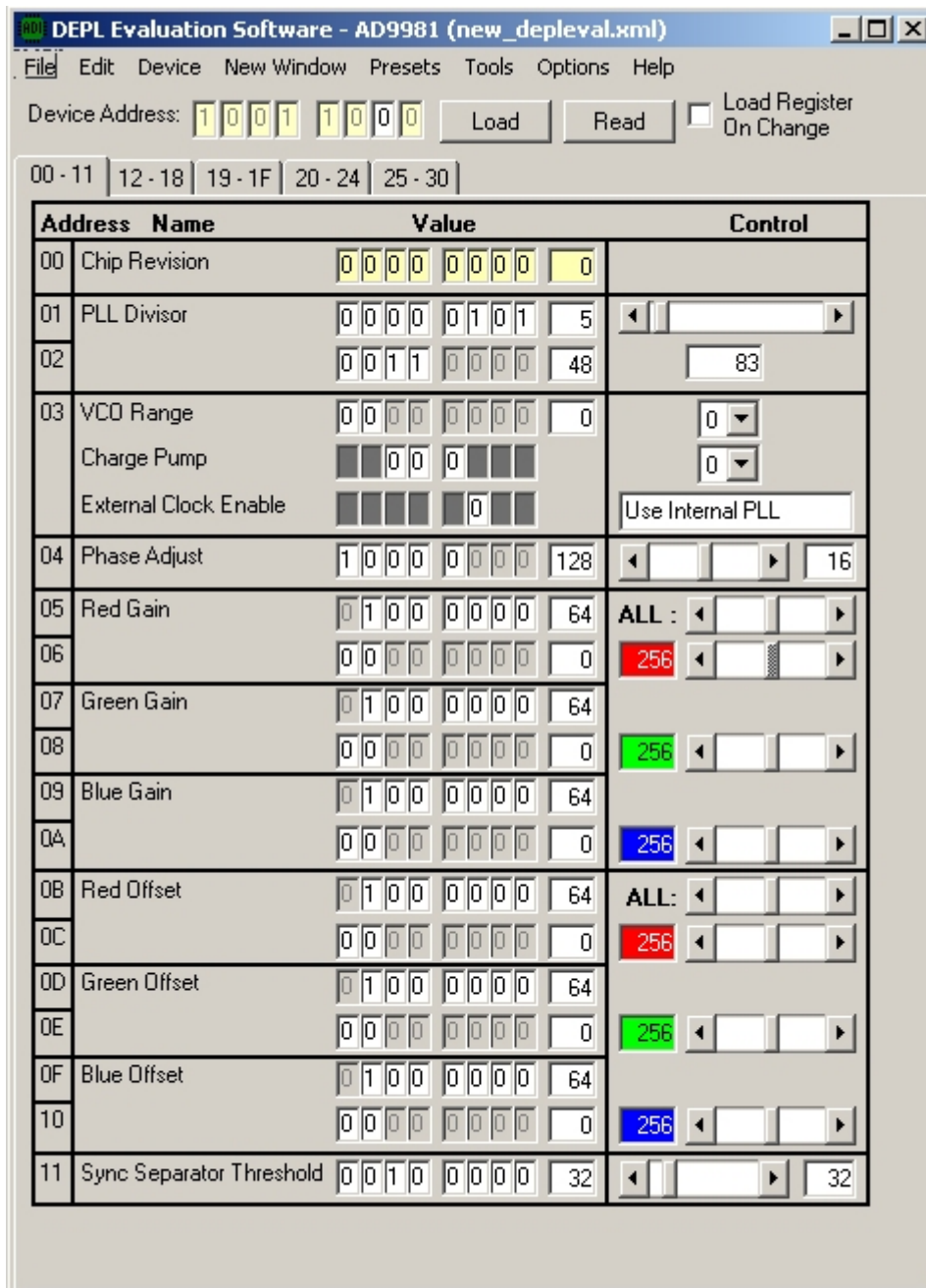
Figure 2. DEPL Evaluation Software—AD9981 Register Setup Window

AD9981 SOFTWARE CONTROL

To select the AD9981 as the target device for the DEPL evaluation software, select **Device** > **AD9981**. This displays the **DEPL Evaluation Software – AD9981** register setup window, as shown in Figure 2. From this window you can control every bit within the AD9981. A detailed, bit-by-bit functional description is provided in the AD9981 data sheet.

To update the registers in the AD9981, click **Load** at the top of the window. This is true unless **Load Register On Change** is checked. In this case, the appropriate register is updated as soon as any change is made in the window. The five tabs in this control window enable you to display groups of registers. The selections are 00-011, 12-18, 19-24, or 25-30. Click the appropriate tab to view/control the register desired.

PLL Settings

The PLL settings are in Registers 0x01 to 0x04. The PLL Divisor setting (12 bits) can be set bit-by-bit (the value toggles when clicking on the bit) by setting a value for Registers 0x01 and 0x02 (decimal value), by setting the 12-bit value (decimal value), or by moving the control bar left (to decrease) or right (to increase). When changing the value using one of these methods, the change is reflected in the other three. The values are not written to the AD9981 until you click **Load**.

The VCO Range and Charge Pump settings in Register 0x03 can be set by individual bit, by register, or by pull-down menu selection.

The 5-bit Phase Adjust in Register 0x04 can be altered in the some manner as the PLL Divisor.

Table 1 contains example PLL register settings for various video modes. For PLL settings not included here, an Excel spreadsheet for calculating PLL settings can be accessed under the Design Tools section of the Analog Devices Display Electronics web site at www.analog.com/flatpanel.

Gain and Offset Settings

The 9-bit gain control for the red, green, and blue video channels are contained in Registers 0x05 to 0x0A and can be changed bit-by-bit, by setting a value for the registers (decimal value), or by moving the control bar left (to decrease) or right (to increase). The 9-bit offset control for the red, green, and blue channels are contained in Registers 0x0B to 0x10. These can be set in the same manner as gain. Note that using the gain and offset control bars at the top of their respective sections changes all three channels by the same amount, regardless of their setting. In other words, if, in order to achieve color balance, your offset settings are 60, 70, and 80 for R, G, and B, respectively, the minimum settings are 0, 10, and 20. The maximum offset settings would then be 107, 117, and 127. To control the gain or offset of an individual channel, separate control bars for each color are also provided.

Sync Separator Control

Register 0x11 contains bits for setting the Sync Separator Threshold. The threshold can be changed bit-by-bit by setting a value for the register (decimal value), or by moving the control bar left (to decrease) or right (to increase). The resulting state of the register is reflected in the box to the right.

Sync Control

Registers 0x12 to 0x15 contain bits for controlling input and output Hsync and Vsync signals. You can toggle each bit by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit. The HSOUT and VSOUT (if enabled) pulse widths can also be adjusted using the control bar to the right of their respective registers.

Coast and Clamp Control

Pre-Coast, Post-Coast, various Coast and Clamp controls, and Clamp Placement and Duration are controlled via Registers 0x16 to 0x1B. You can toggle each bit by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit. The pre- and post-Coast as well as the Clamp Placement and Duration registers can also be controlled via the sliding bar to the right of their respective registers.

Auto-Offset Control

Register 0x1B contains bits for controlling the auto-offset function. You can toggle each bit by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit. For more details on this function, the application note "Implementing the Auto-Offset Function of the AD9981" can be downloaded from our web site. This information can also be found in the AD9981 data sheet.

SOG Control and Power Management

Registers 0x1D and 0x1E contain bits for controlling the SOG, Input Selection,m and Power Management functions. You can toggle each bit by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit.

Output Control

Registers 0x1 and 0x20 contain bits for controlling Output functions. You can toggle each bit by clicking on it. The resulting state of the bit is reflected in the box to the right of each bit. The Output Mode bits also have pull-down menus that can be used for output mode selection.

Sync Pulse Filter Control

Registers 0x21 to 0x23 contain the bits for controlling Sync Pulse Filter. These controls can be modified bit by bit, by changing the 8-bit (decimal) value or by using the slider bar to the right of each register.

Status Registers (Read-Only)

Registers 0x24 to 0x27 are read-only registers that provide status for Hsync, Vsync, and SOG Detection (0x24), Hsync, Vsync, Coast, and Clamp Polarity (0x25), and the Hsync per Vsync Counter (0x16 to 0x27). Performing a read (by clicking **Read**) lets you see the status of each of these bits. The status is also reflected in the text to the right of each of these bits.

SAMPLE SETTINGS FOR THE EVALUATION BOARD

Table 1. Sample Settings

Mode	Resolution	Nominal Frequency Hs (kHz)	Nominal Pixel Clock (MHz)	PLL Divider	PLL Settings		ADC Setting
					VCO Range[1] (0x03 7:6)	Charge Pump Current[1] (0x03 5:3)	Latch Select (0x2D 4:3)
VGA	640 × 480 at 60 Hz	31.469	25.175	800	00	101	01
	640 × 480 at 72 Hz	37.861	31.500	832	01	011	01
	640 × 480 at 75 Hz	37.500	31.500	840	01	011	01
	640 × 480 at 85 Hz	43.269	36.000	832	01	100	01
SVGA	800 × 600 at 56 Hz	35.156	36.000	1024	01	100	01
	800 × 600 at 60 Hz	37.879	40.000	1056	01	100	01
	800 × 600 at 72 Hz	48.077	50.000	1040	01	110	01
	800 × 600 at 75 Hz	46.875	49.500	1056	01	110	01
	800 × 600 @ at 85 Hz	53.674	56.250	1048	01	110	01
XGA	1024 × 768 at 60 Hz	48.363	65.000	1344	10	100	01
	1024 × 768 at 70 Hz	56.476	75.000	1328	10	100	01
	1024 × 768 at 75 Hz	60.023	78.750	1312	10	101	01
	1024 × 768 at 80 Hz	64.000	85.500	1336	10	101	01
	1024 × 768 at 85 Hz	68.677	94.50	1376	10	110	01
SXGA	1280 × 1024 at 60 Hz	60.020	108.000	1688	10	111	10
TV	480i	15.750	13.510	858	00	001	01
	480p	31.470	27.000	858	00	100	01
	720p	45.000	74.250	1650	10	100	01
	1080i	33.750	74.250	2200	10	100	01
	1080p @30 Hz	33.750	74.250	2200	10	100	01

[1] The VCO Range and Charge Pump Current settings are preliminary and may need slight adjustments.
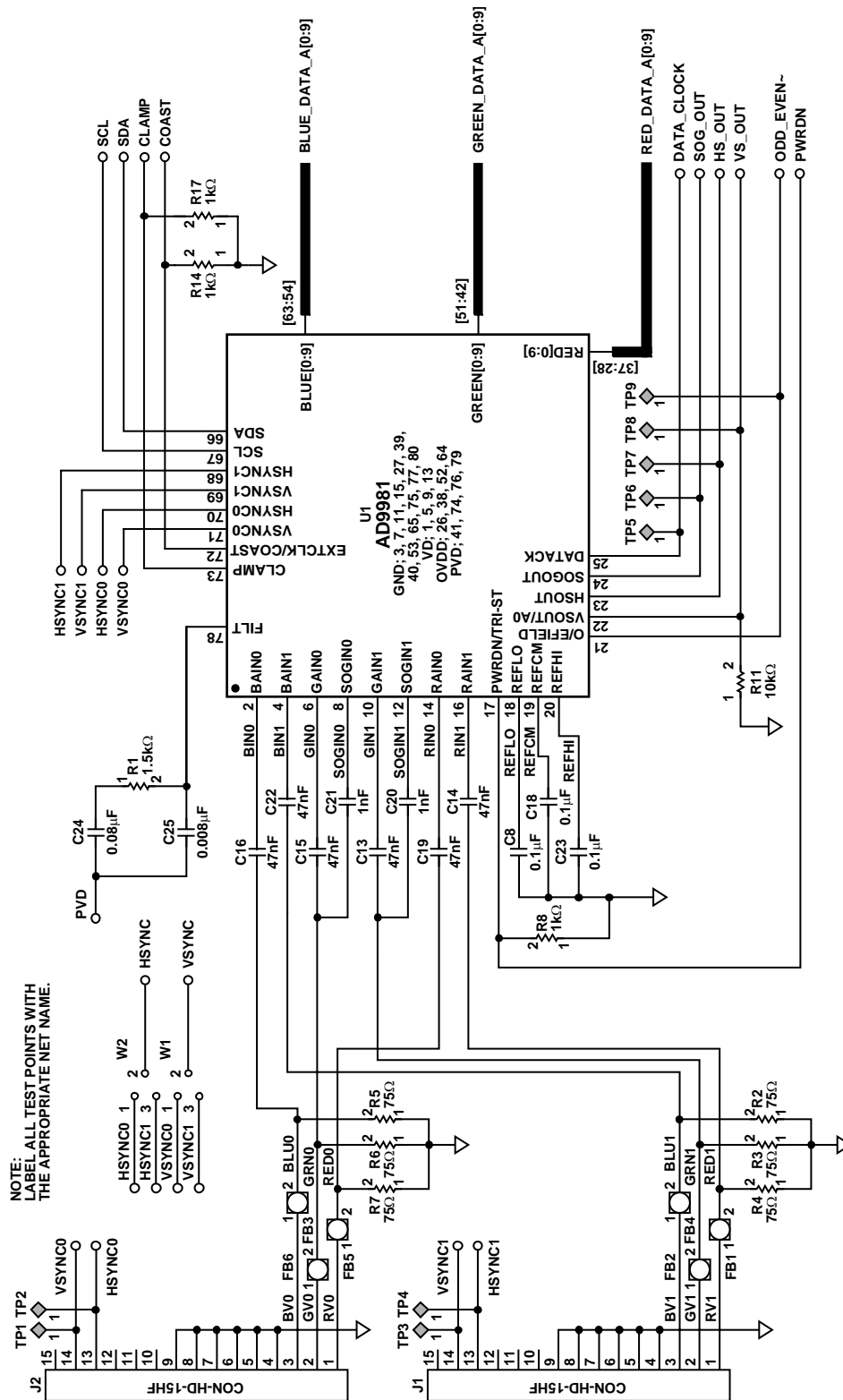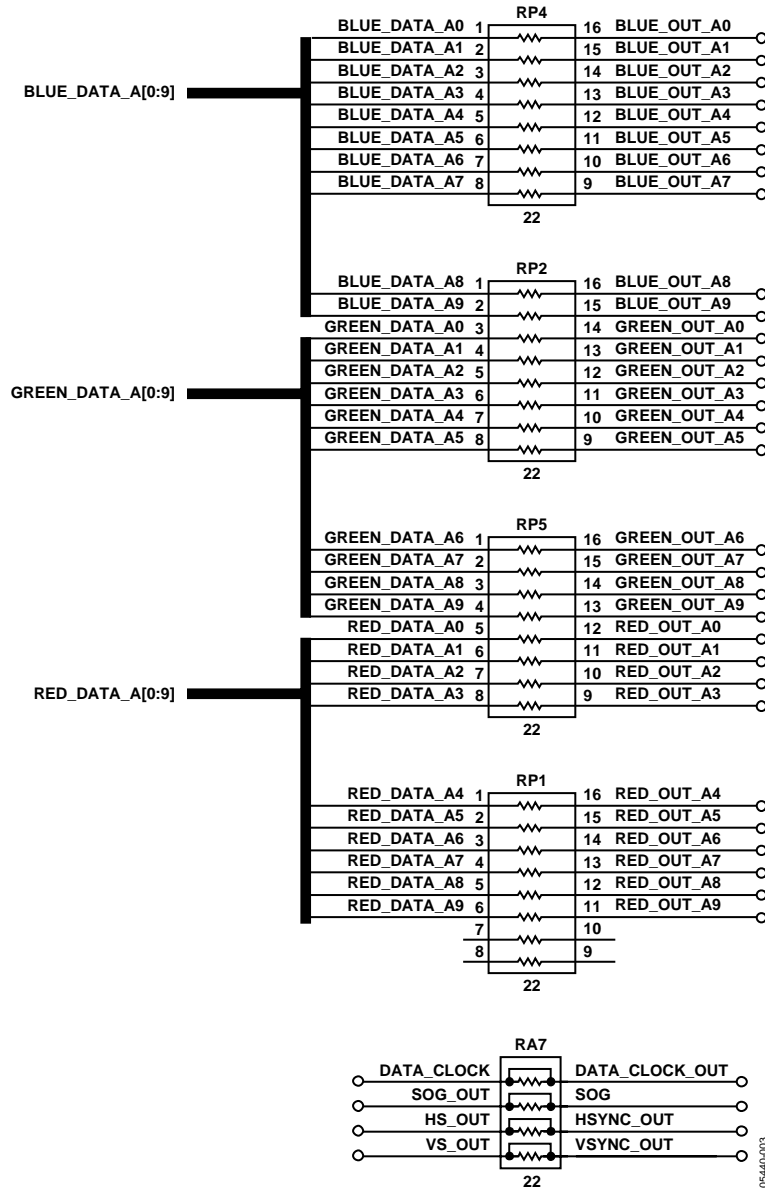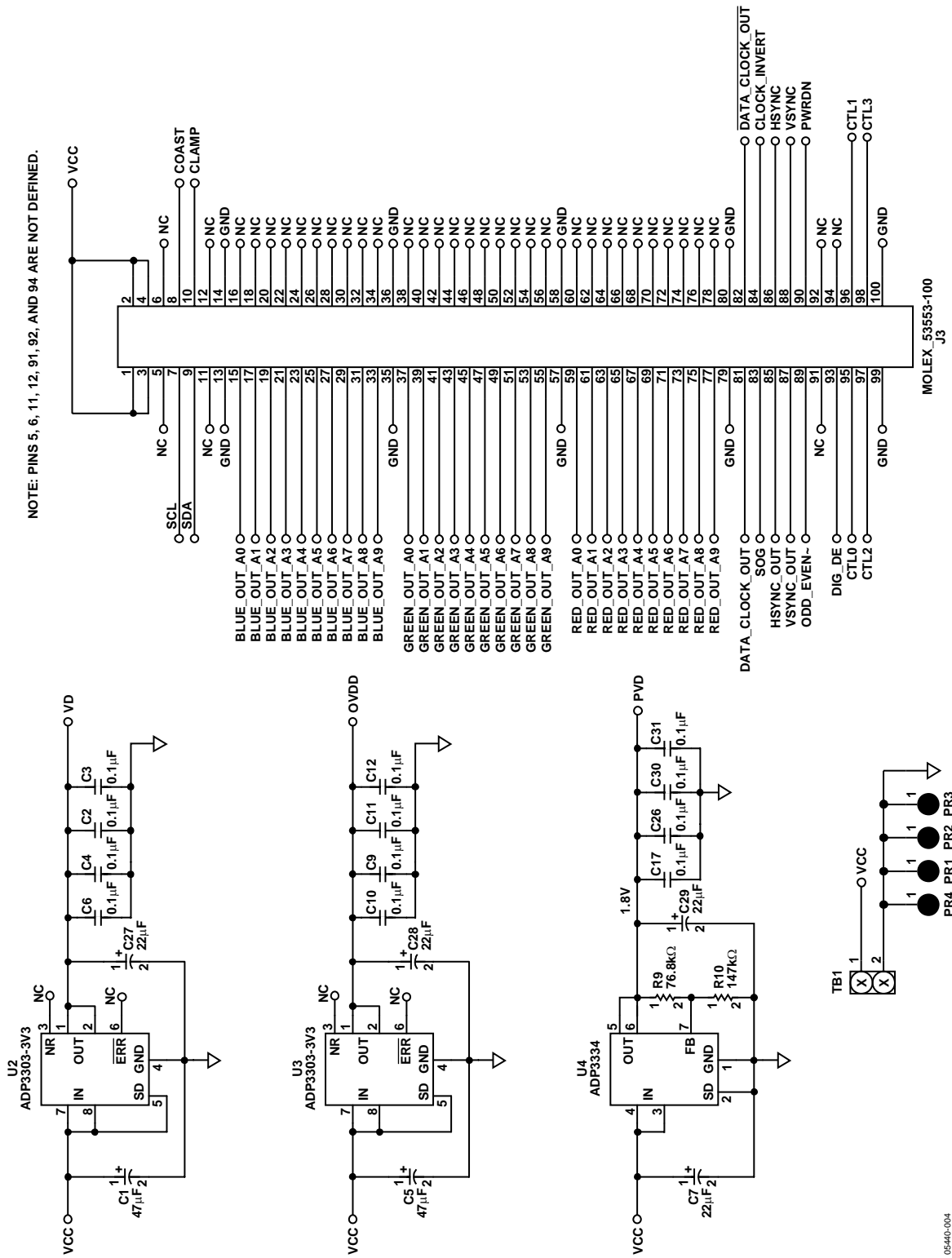
SCHEMATICS AND LAYOUT

Figure 3.

	RP4		
BLUE_DATA_A0	1	16	BLUE_OUT_A0
BLUE_DATA_A1	2	15	BLUE_OUT_A1
BLUE_DATA_A2	3	14	BLUE_OUT_A2
BLUE_DATA_A3	4	13	BLUE_OUT_A3
BLUE_DATA_A4	5	12	BLUE_OUT_A4
BLUE_DATA_A5	6	11	BLUE_OUT_A5
BLUE_DATA_A6	7	10	BLUE_OUT_A6
BLUE_DATA_A7	8	9	BLUE_OUT_A7

BLUE_DATA_A[0:9]

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	RP2		
BLUE_DATA_A8	1	16	BLUE_OUT_A8
BLUE_DATA_A9	2	15	BLUE_OUT_A9
GREEN_DATA_A0	3	14	GREEN_OUT_A0
GREEN_DATA_A1	4	13	GREEN_OUT_A1
GREEN_DATA_A2	5	12	GREEN_OUT_A2
GREEN_DATA_A3	6	11	GREEN_OUT_A3
GREEN_DATA_A4	7	10	GREEN_OUT_A4
GREEN_DATA_A5	8	9	GREEN_OUT_A5

GREEN_DATA_A[0:9]

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	RP5		
GREEN_DATA_A6	1	16	GREEN_OUT_A6
GREEN_DATA_A7	2	15	GREEN_OUT_A7
GREEN_DATA_A8	3	14	GREEN_OUT_A8
GREEN_DATA_A9	4	13	GREEN_OUT_A9
RED_DATA_A0	5	12	RED_OUT_A0
RED_DATA_A1	6	11	RED_OUT_A1
RED_DATA_A2	7	10	RED_OUT_A2
RED_DATA_A3	8	9	RED_OUT_A3

RED_DATA_A[0:9]

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	RP1		
RED_DATA_A4	1	16	RED_OUT_A4
RED_DATA_A5	2	15	RED_OUT_A5
RED_DATA_A6	3	14	RED_OUT_A6
RED_DATA_A7	4	13	RED_OUT_A7
RED_DATA_A8	5	12	RED_OUT_A8
RED_DATA_A9	6	11	RED_OUT_A9
	7	10	
	8	9	

22

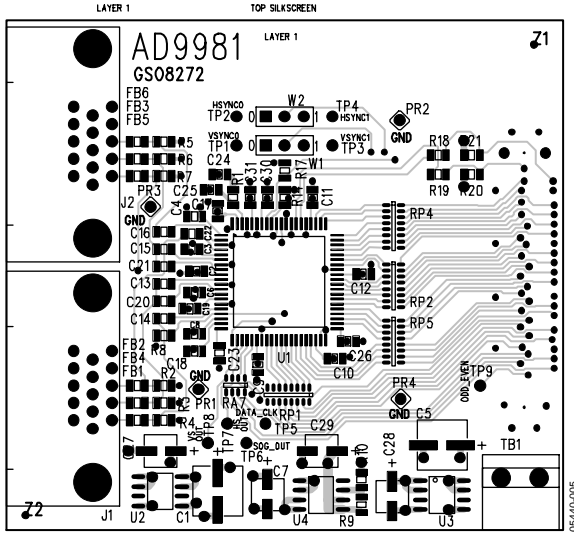|	RA7	
DATA_CLOCK		DATA_CLOCK_OUT
SOG_OUT		SOG
HS_OUT		HSYNC_OUT
VS_OUT		VSYNC_OUT

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05440-003

Figure 4.

Figure 5.

05440-004

Figure 6.

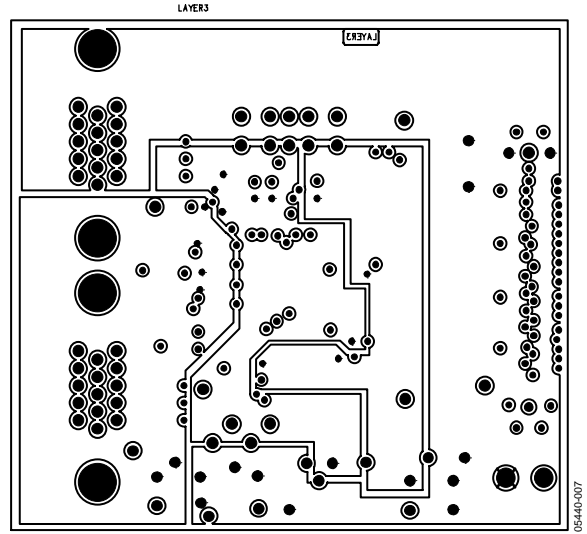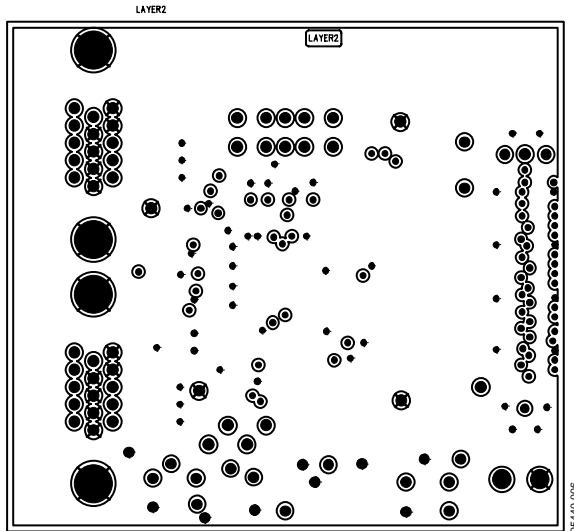

Figure 8.

Figure 7.
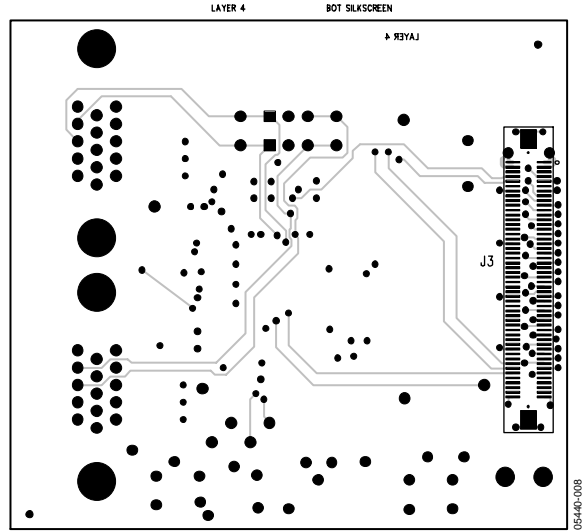
Figure 9.

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

L/I	QTY	REFDES	Description	Part No.	Mfgr.	Dist.	Dist. Part No.	Sub?
1	2	C1, C5	47 µF,16 V, ALUM, ELECTRO, 'D'	ECE-V1CA470SP	PANASONIC	DIGIKEY	PCE3164CT-ND	Y
2	15	C2–C4, C6, C8–C12, C17–C18, C23, C26, C30–C31	.1 µF, 25 V, X7R, 0805, CER	ECJ-2VB1E104K	PANASONIC	DIGIKEY	PCC1828CT-ND	Y
3	4	C7, C27–C29	22 µF, 6.3 V, ALUM, ELECTRO	ECE-V0JA220SR	PANASONIC	DIGIKEY	PCE3056CT-ND	Y
4	6	C13–C16, C19, C22	.047 µF, 50 V, X7R, 0805, CER	ECJ-2YB1H473K	PANASONIC	DIGIKEY	PCC1836CT-ND	Y
5	2	C20, C21	.001 µF, 50 V, NPO, 0805, CER	ECU-V1H102KBN	PANASONIC	DIGIKEY	PCC102BNCT-ND	Y
6	1	C24	.082 µF, 50 V, X7R, 0805, CER	ECJ-2YB1H823K	PANASONIC	DIGIKEY	PCC1839CT-ND	Y
7	1	C25	8200 pF, 50 V, X7R, 0805, CER	ECU-V1H822KBG	PANASONIC	DIGIKEY	PCC822BNCT-ND	Y
8	6	FB1–FB6	120 Ω @100 MHz BEAD, 0805	2508051217Z0	FAIR-RITE	ALLIED	589-0585	N
9	2	J1, J2	15-PIN D-SUB CONN	181-015-212-171	NORCOMP	DIGIKEY	815RF-ND	N
10	1	J3	100-PIN MATED CONNECTOR	53553-1009	MOLEX	FORCE	53553-1009	N
11	1	R1	1.50 kΩ, 1%, 1/10W 0805	ERJ-6ENF1501V	PANASONIC	DIGIKEY	P1.50KCCT-ND	Y
12	6	R2–R7	75.0 Ω, 1%, 1/10W 0805	ERJ-6ENF75R0V	PANASONIC	DIGIKEY	P75.0CCT-ND	Y
13	3	R8, R14, R17	1.00 kΩ, 1%, 1/10W 0805	ERJ-6ENF1001V	PANASONIC	DIGIKEY	P1.00KCCT-ND	Y
14	1	R9	76.8 kΩ, 1%, 1/10W 0805	ERJ-6ENF7682V	PANASONIC	DIGIKEY	P76.8KCCT-ND	Y
15	1	R10	147 kΩ, 1%, 1/10W 0805	ERJ-6ENF1472V	PANASONIC	DIGIKEY	P147KCCT-ND	Y
16	2	R18, R19	150 Ω, 1%, 1/10W 0805	ERJ-6ENF1500V	PANASONIC	DIGIKEY	P150CCT-ND	Y
17	2	R20, R21	2.00 kΩ, 1%, 1/10W 0805	ERJ-6ENF2001V	PANASONIC	DIGIKEY	P2.00KCCT-ND	Y
18	1	RA7	22 Ω RPAK, 1/16W, 5%, 4RES	742C083220J	CTS	DIGIKEY	742C083220JCT-ND	Y
19	4	RP1, RP2, RP4, RP5	22 Ω RPAK, 1/16W, 5%, 8RES	742C163220J	CTS	DIGIKEY	742C163220JCT-ND	Y
20	1	TB1	NOT POPULATED					
21	1	U1	IC,10-BIT CONVERTER	AD9981	ADI	ADI	AD9981	N
22	2	U2, U3	IC, 3.3 V REGULATOR	ADP3303AR-3.3	ADI	ADI	ADP3303AR-3.3	N
23	1	U4	IC, VAR REGULATOR	ADP3334	ADI	ADI	ADP3334	N
24	1	N/A	PC BOARD	GSO8272	ADI	PCSM	GSO8272	N
25	4	N/A	SCREW 4-40 X 3/8" FOR J1, J2		SPC	NEWARK	31G2198	Y
26	4	N/A	4-40 HEX NUT FOR J1, J2		SPC	NEWARK	31F2106	Y
27	2	W1, W2	3-PIN HEADER	2340-6111TN	3M	MOUSER	2340-6111TN	Y

ORDERING GUIDE

Model	Package Description
AD9981/PCB	Evaluation Board

CONTACT INFORMATION

Questions? Please email us directly at flatpanel_apps@analog.com, visit our web site at http://www.analog.com/flatpanel, or call the Analog Devices help line at 1-800-AnalogD.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

NOTES

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