



四通道、超低功耗、300Mbps ATE驱动器/比较器

MAX9972

概述

MAX9972为四通道、超低功耗、引脚电子测量IC，每通道包括三电平引脚驱动器、窗口比较器、无源负载和加载-感应Kelvin切换参数测量单元(PMU)。驱动器具有-2.2V至+5.2V电压范围，包含高阻和有源端接(第3级驱动)工作模式，在低电压摆幅下仍可保持高线性。窗口比较器具有500MHz等效输入带宽和可编程的输出电压。无源负载为被测器件(DUT)提供上拉和下拉电压。

提供两种精度等级：A级和B级。A级器件为驱动器和比较器提供精确的增益和失调匹配，允许多通道共用基准电压，且具有严格的负载阻抗公差；B级器件适用于每通道具有独立基准电压的系统设计。

通过3线、低压、CMOS兼容串口编程设置器件的低泄漏、高阻抗和端接特性。高速PMU切换通过专用的数字控制输入实现。

器件采用80引脚、12mm x 12mm、1.0mm引脚间距的TQFP封装，封装底部的6mm x 6mm裸焊盘提供高效散热。MAX9972工作在0°C至+70°C商业级温度范围，且具有管芯温度监测输出。

特性

- ◆ 小尺寸：在0.3in²上集成了四个通道
- ◆ 低功耗：每通道325mW (典型值)
- ◆ 高速：3V_{P-P}时，300Mbps
- ◆ -2.2V至+5.2V工作电压范围
- ◆ 有源端接(第3级驱动)
- ◆ 集成PMU开关
- ◆ 无源负载
- ◆ 低泄漏模式：20nA (最大值)
- ◆ 低增益误差、失调误差
- ◆ 提供无铅(Pb)封装

应用

NAND闪存测试器
DRAM探测器
低成本混合信号/片上系统(SoC)测试仪
有源老化系统
结构测试仪

引脚配置在数据资料的最后给出。

订购信息和选型指南

PART	ACCURACY GRADE	PIN-PACKAGE	HEAT EXTRACTION
MAX9972ACCS	A	80 TQFP-EP*	Bottom
MAX9972BCCS	B	80 TQFP-EP*	Bottom

注：所有器件工作在0°C至+70°C温度范围。

所有型号均提供含铅、无铅(Pb)封装。订购无铅(Pb)封装时请在型号的末端加“+”符号。

*EP = 裸焊盘。



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有关价格、供货及订购信息，请联络Maxim亚洲销售中心：10800 852 1249 (北中国区)，10800 152 1249 (南中国区)，或访问Maxim的中文网站：china.maxim-ic.com。

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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V to +9.4V
V _{SS} to GND	-6.25V to +0.3V
V _{DD} to V _{SS}	+15.7V
V _L to GND	-0.3V to +5V
DHV ₋ , DTV ₋ , DLV ₋ , DATA ₋ , RCV ₋ , LDV ₋ , DUT ₋ to GND	V _{SS} to V _{DD}
CHV ₋ , CLV ₋ , CMPH ₋ , CMPL ₋ , COMPHI, COMPLO to GND	V _{SS} to V _{DD}
FORCE ₋ , SENSE ₋ , PMU ₋ to GND	V _{SS} to V _{DD}
LD ₋ , DIN ₋ , SCLK ₋ , CS ₋ to GND	-0.3V to +5V
DUT ₋ , CMPH ₋ , CMPL ₋ Short-Circuit Duration	Continuous

DHV ₋ , DLV ₋ , DTV ₋ to Each Other	V _{SS} to V _{DD}
CHV ₋ , CLV ₋ to DUT ₋	V _{SS} to V _{DD}
DOUT ₋ to GND	-0.3V to +5V
TEMP Short-Circuit Duration	Continuous
FORCE ₋ Path Switch Current	50mA
SENSE ₋ Path Switch Current	1.5mA
Continuous Power Dissipation (T _A = +70°C) 80-Pin TQFP-EP (derate 35.7mW/°C above +70°C)	2857mW
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMP_{HI}} = +1V, V_{COMP_{LO}} = 0V, V_{LDV₋} = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DRIVER (all specifications apply when DUT₋ = DHV₋, DUT₋ = DTV₋, or DUT₋ = DLV₋)							
DC CHARACTERISTICS							
Voltage Range			-2.2		+5.2	V	
Gain		Measured at 0 and 3V	A grade	0.995	1	1.005	V/V
			B grade	0.95		1.05	
Gain Temperature Coefficient				50		ppm/°C	
Offset		V _{DHV₋} = 2V, V _{DLV₋} = 0V, V _{DTV₋} = 1V	A grade			±10	mV
			B grade			±100	
Offset Temperature Coefficient				±250		µV/°C	
Power-Supply Rejection Ratio	PSRR	V _{DD} , V _{SS} independently varied over full range			18	mV/V	
Maximum DC Drive Current	I _{DUT₋}		±40		±90	mA	
DC Output Resistance		I _{DUT₋} = ±10mA (Note 2)	48.5	49.5	50.5	Ω	
DC Output Resistance Variation		I _{DUT₋} = -40mA to +40mA			2.5	Ω	
DC Crosstalk		DHV ₋ to DLV ₋ and DTV ₋ : V _{DLV₋} = V _{DTV₋} = +1.5V, V _{DHV₋} = -2.2V, +5.2V			5	mV	
		DLV ₋ to DHV ₋ and DTV ₋ : V _{DHV₋} = V _{DTV₋} = +1.5V, V _{DLV₋} = -2.2V, +5.2V			5		
		DTV ₋ to DHV ₋ and DLV ₋ : V _{DHV₋} = V _{DLV₋} = +1.5V, V _{DTV₋} = -2.2V, +5.2V			5		
Linearity Error		0 to 3V (Note 3)			±5	mV	
		Full range (Note 4)			±15	mV	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +8V$, $V_{SS} = -5V$, $V_L = +3V$, $V_{COMPHI} = +1V$, $V_{COMPL0} = 0V$, $V_{LDV_} = 0V$, $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$, $T_J = +75^{\circ}C$. All temperature coefficients measured at $T_J = +50^{\circ}C$ to $+100^{\circ}C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Note 5)						
Dynamic Output Current		(Note 1)	40			mA
Drive-Mode Overshoot, Undershoot, and Preshoot		200mV to 4V _{P-P} swing (Note 6)		5% +10		mV
Term-Mode Spike		$V_{DHFV_} = V_{DTV_} = 1V$, $V_{DLV_} = 0V$		25		mV
		$V_{DLV_} = V_{DTV_} = 0V$, $V_{DHFV_} = 1V$		25		
High-Impedance-Mode Spike		$V_{DLV_} = -1V$, $V_{DHFV_} = 0V$		25		mV
		$V_{DLV_} = 0V$, $V_{DHFV_} = 1V$		25		
Prop Delay, Data to Output				2		ns
Prop-Delay Temperature Coefficient				10		ps/ $^{\circ}C$
Prop-Delay Match, t_{LH} vs. t_{HL}				30		ps
Prop-Delay Skew, Drivers Within Package				150		ps
Prop-Delay Change vs. Pulse Width		Relative to 12.5ns pulse	3V _{P-P} , 40MHz, PW = 4ns to 21ns		20	ps
			1V _{P-P} , 40MHz, PW = 2.5ns to 23.5ns		90	
Prop-Delay Change vs. Common-Mode Voltage		1V _{P-P} , $V_{DLV_} = 0$ to 3V, relative to delay at $V_{DLV_} = 1V$		80		ps
Prop Delay, Data to High Impedance		$V_{DHFV_} = +1.5V$, $V_{DLV_} = -1.5V$, both directions		1.8		ns
Prop Delay, Data to Term		$V_{DHFV_} = +1.5V$, $V_{DLV_} = -1.5V$, $V_{DTV_} = 0V$, both directions		1.6		ns
Minimum Voltage Swing		(Note 7)		25		mV
Rise/Fall Time		$V_{DHFV_} = 0.2V$, $V_{DLV_} = 0V$, 20% to 80%		0.7		ns
		$V_{DHFV_} = 1V$, $V_{DLV_} = 0V$, 20% to 80%		0.7		
		$V_{DHFV_} = 3V$, $V_{DLV_} = 0V$, 10% to 90%	1.5	2.0	2.5	
		$V_{DHFV_} = 4V$, $V_{DLV_} = 0V$, $R_L = 500\Omega$, 10% to 90%		2.6		
		$V_{DHFV_} = 5V$, $V_{DLV_} = 0V$, $R_L = 500\Omega$, 10% to 90%		3.4		
Rise/Fall-Time Matching		$V_{DHFV_} = 1V$ to 5V		± 5		%
Minimum Pulse Width (Note 8)		200mV, $V_{DHFV_} = 0.2V$, $V_{DLV_} = 0V$		1.8		ns
		1V, $V_{DHFV_} = 1V$, $V_{DLV_} = 0V$		2.4		
		3V, $V_{DHFV_} = 3V$, $V_{DLV_} = 0V$		3.3		

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($V_{DD} = +8V$, $V_{SS} = -5V$, $V_L = +3V$, $V_{COMP\ HI} = +1V$, $V_{COMP\ LO} = 0V$, $V_{LDV} = 0V$, $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$, $T_J = +75^\circ C$. All temperature coefficients measured at $T_J = +50^\circ C$ to $+100^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATOR (Note 9)						
DC CHARACTERISTICS (driver in high-impedance mode)						
Input Voltage Range			-2.2		+5.2	V
Differential Input Voltage		$V_{DUT_} - V_{CHV_}$, $V_{DUT_} - V_{CLV_}$	-7.4		+7.4	V
Hysteresis		$V_{CHV_} = V_{CLV_} = 1.5V$		8		mV
Input Offset Voltage		$V_{DUT_} = 1.5V$ ($V_{COMP\ HI} = 0.8V$, $V_{COMP\ LO} = 0.2V$)			± 10 ± 100	mV
Input Offset Temperature Coefficient				25		$\mu V/^\circ C$
Common-Mode Rejection Ratio	CMRR	$V_{DUT_} = 0$ and $3V$	60			dB
Linearity Error (Note 10)		$V_{DUT_} = 1.5V$ $V_{DUT_} = -2.2V, +5.2V$			± 5 ± 10	mV
Power-Supply Rejection Ratio	PSRR	$V_{DUT_} = 1.5V$, supplies independently varied over full range			5	mV/V
AC CHARACTERISTICS (Note 11)						
Equivalent Input Bandwidth		Terminated (Note 12)		500		MHz
		High impedance (Note 13)		300		
Propagation Delay				3.9		ns
Prop-Delay Temperature Coefficient				4		$ps/^\circ C$
Prop-Delay Match, t_{LH} to t_{HL}				120		ps
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL)		200		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 14)		0 to 4.9V		20		ps
		-1.9V to +4.9V		30		
Prop-Delay Dispersions vs. Overdrive		$V_{CHV_} = V_{CLV_} = 0.1V$ to $0.9V$, $V_{DUT_} = 1V_{P-P}$, $t_R = t_F = 500ps$, 10% to 90% relative to timing at 50% point		220		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width		± 60		ps
Prop-Delay Dispersions vs. Slew Rate		0.5V/ns to 2V/ns		50		ps

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($V_{DD} = +8V$, $V_{SS} = -5V$, $V_L = +3V$, $V_{COMP\ HI} = +1V$, $V_{COMP\ LO} = 0V$, $V_{LDV_} = 0V$, $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$, $T_J = +75^\circ C$. All temperature coefficients measured at $T_J = +50^\circ C$ to $+100^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
LOGIC OUTPUTS							
Reference Voltages COMPHI and COMPLO		(Note 15)	0		+3.6	V	
Output High Voltage Offset		$I_{OUT} = 0mA$, relative to COMPHI at $V_{COMP\ HI} = 1V$			± 50	mV	
Output Low Voltage Offset		$I_{OUT} = 0mA$, relative to COMPLO at $V_{COMP\ LO} = 0V$			± 50	mV	
Output Resistance		$I_{CHV_} = I_{CLV_} = \pm 10mA$	40	50	60	Ω	
Current Limit				25		mA	
Rise/Fall Time		20% to 80%, $V_{CHV_} = 1VP-P$, load = T-line, 50Ω , $> 1ns$		0.7		ns	
PASSIVE LOAD							
DC CHARACTERISTICS ($R_{DUT_} \geq 10M\Omega$)							
LDV_ Voltage Range			-2.2		+5.2	V	
Gain			0.99		1.01	V/V	
Gain Temperature Coefficient				0.02		$\%/^\circ C$	
Offset					± 100	mV	
Offset Temperature Coefficient				0.02		$mV/^\circ C$	
Power-Supply Rejection Ratio	PSRR			10		mV/V	
Output Resistance Tolerance—High Value		$I_{DUT_} = \pm 0.2mA$, $V_{LDV_} = 1.5V$	A grade	7.125	7.5	7.875	$k\Omega$
			B grade	4.200	6.0	7.875	
Output Resistance Tolerance—Low Value		$I_{DUT_} = \pm 0.1mA$, $V_{LDV_} = 1.5V$	A grade	1.90	2.0	2.10	$k\Omega$
			B grade	1.05	1.5	2.10	
Switch Resistance Variation		Relative to 1.5V	0 to 3V		± 10	%	
			Full range		± 30		
Maximum Output Current (Note 16)		$V_{LDV_} = -2V$, $V_{DUT_} = +5V$		± 4		mA	
		$V_{LDV_} = +5V$, $V_{DUT_} = -2V$		± 4			
Linearity Error, Full Range		Measured at -2.2V, +1.5V, and +5.2V (Note 16)			± 25	mV	
AC CHARACTERISTICS							
Settling Time, LDV_ to Output		$V_{LDV_} = -2V$ to +5V step, $R_{DUT_} = 100k\Omega$ (Note 17)		0.5		μs	
Output Transient Response		$V_{LDV_} = +1.5V$, $V_{DUT_} = -2V$ to +5V square wave at 1MHz, $R_{DUT_} = 50\Omega$		20		ns	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMP}HI = +1V, V_{COMP}LO = 0V, V_{LDV} = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMU SWITCHES (FORCE_, SENSE_, PMU_)						
Voltage Range			-2.2		+5.2	V
Force Switch Resistance		V _{FORCE_} = 1.5V, I _{PMU_} = ±10mA			40	Ω
Force Switch Compliance		V _{PMU_} = 6.2V, V _{FORCE_} set to make I _{FORCE_} = 30mA	25			mA
		V _{PMU_} = -3.2V, V _{FORCE_} set to make I _{FORCE_} = -30mA	25			
Force Switch Resistance Variation (Note 18)		0 to 3V		±10		%
		Full range		±30		
Sense Switch Resistance			700	1000	1300	Ω
Sense Switch Resistance Variation		Relative to 1.3V, full range		±30		%
PMU_ Capacitance		Force-and-sense switches open		5		pF
FORCE_ Capacitance				5		pF
SENSE_ Capacitance				0.2		pF
FORCE_ External Capacitance		Allowable external capacitance		2		nF
SENSE_ External Capacitance		Allowable external capacitance		1		nF
FORCE_ and SENSE_ Switching Speed		Connect or disconnect		10		μs
PMU_ Leakage		FORCE EN_ = SENSE EN_ = 0, V _{FORCE_} = V _{SENSE_} = -2.2V to +5.2V		±0.5	±5	nA
TOTAL FUNCTION						
DUT_						
Leakage, High-Impedance Mode		Load switches open, V _{DUT_} = +5.2V, V _{CLV_} = V _{CHV_} = -2.2V, V _{DUT_} = -2.2V, V _{CLV_} = V _{CHV_} = +5.2V, full range			2	μA
Leakage, Low-Leakage Mode		Full range		±1	±20	nA
Low-Leakage Recovery Time		(Note 19)		10		μs
Combined Capacitance		Term mode		2		pF
		High-impedance mode		5		
Load Resistance		(Note 20)		1		GΩ
Load Capacitance		(Note 20)		12		nF

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, V_{LDV} = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE INPUTS (DHV₋, DTV₋, DLV₋, DATA₋, RCV₋, CHV₋, CLV₋, LDV₋, COMPHI, COMPLO)						
Input Bias Current					±100	μA
Input Bias Current Temperature Coefficient				±200		nA/°C
Settling to Output		0.1% of full-scale step		10		μs
DIGITAL INPUTS (DATA₋, RCV₋, LD, DIN, SCLK, CS)						
Input High Voltage		(Note 21)	V _L / 2 + 0.2		+3.6	V
Input Low Voltage		(Note 21)	-0.3		V _L / 2 - 0.2	V
Input Bias Current					100	μA
SERIAL DATA OUTPUT (DOUT)						
Output High Voltage		I _{OH} = -1mA	V _L - 0.4		V _L	V
Output Low Voltage		I _{OL} = 1mA	0		+0.4	V
Output Rise and Fall Time		C _L = 10pF		1.1		ns
SCLK to DOUT Delay		C _L = 10pF	t _{DH}		t _{SCLK} - t _{DS} - 2ns	ns
SERIAL-INTERFACE TIMING (Note 22)						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	t _{CH}		10			ns
SCLK Pulse-Width Low	t _{CL}		10			ns
CS Low to SCLK High Setup	t _{CSS0}		3.5			ns
SCLK High to CS Low Hold	t _{CSH0}		0			ns
CS High to SCLK High Setup	t _{CSS1}		3.5			ns
SCLK High to CS High Hold	t _{CSH1}		15			ns
DIN to SCLK High Setup	t _{DS}		3.5			ns
DIN to SCLK High Hold	t _{DH}		1			ns
CS High to LOAD Low Setup	t _{CLL}		6			ns
LD Low Hold Time	t _{LDW}		5			ns
LD High to Any Activity			0			ns
V _L Rising to CS Low		Power-on delay		2		μs
TEMP SENSOR						
Nominal Voltage		T _J = +27°C		3.00		V
Temperature Coefficient				+10		mV/°C
Output Resistance				500		Ω

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +8V$, $V_{SS} = -5V$, $V_L = +3V$, $V_{COMPHI} = +1V$, $V_{COMPLO} = 0V$, $V_{LDV} = 0V$, $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$, $T_J = +75^\circ C$. All temperature coefficients measured at $T_J = +50^\circ C$ to $+100^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 23)	7.6	8	8.4	V
Negative Supply Voltage	V_{SS}	(Note 23)	-5.25	-5	-4.75	V
Logic Supply Voltage	V_L		2.3		3.6	V
Positive Supply Current	I_{DD}	$f_{OUT} = 0MHz$		97	120	mA
Negative Supply Current	I_{SS}	$f_{OUT} = 0MHz$		99	120	mA
Logic Supply Current	I_L			0.15	0.30	mA
Static Power Dissipation		$f_{OUT} = 0MHz$		1.3	1.5	W
Operating Power Dissipation		$f_{OUT} = 100Mbps$ (Note 24)		1.4		W

- Note 1:** All minimum and maximum specifications are 100% production tested except driver dynamic output current, which is guaranteed by design. All specifications are with DUT_ and PMU_ electrically isolated, unless otherwise noted.
- Note 2:** Nominal target value is 49.5 Ω . Contact factory for alternate trim selections within the 45 Ω to 55 Ω range.
- Note 3:** Measured at 1.5V, relative to a straight line through 0 and 3V.
- Note 4:** Measured at end points, relative to a straight line through 0 and 3V.
- Note 5:** DUT_ is terminated with 50 Ω to ground, $V_{DHV} = 3V$, $V_{DLV} = 0$, $V_{DTV} = 1.5V$, unless otherwise specified. DATA_ and RCV_ logic levels are $V_{HIGH} = 2V$, $V_{LOW} = 1V$.
- Note 6:** Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.
- Note 7:** At the minimum voltage swing, undershoot is less than 20%. DHV_ and DLV_ references are adjusted to result in the specified swing.
- Note 8:** At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.
- Note 9:** With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
- Note 10:** Relative to a straight line through 0 and 3V.
- Note 11:** Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT} = 0$ to 1V, $V_{CHV} = V_{CLV} = +0.5V$, $t_R = t_F = 500ps$, $Z_S = 50\Omega$, driver in term mode with $V_{DTV} = +0.5V$. Comparator outputs are terminated with 50 Ω to GND. Measured from V_{DUT} crossing calibrated CHV_/CLV_ threshold to midpoint of nominal comparator output swing.
- Note 12:** Terminated is defined as driver in drive mode and set to zero volts.
- Note 13:** High impedance is defined as driver in high-impedance mode.
- Note 14:** $V_{DUT} = 200mV_{P-P}$. Propagation delay is compared to a reference time at 1.5V.
- Note 15:** The comparator meets all its timing specifications with the specified output conditions when the output current is less than 15mA, $V_{COMPHI} > V_{COMPLO}$, and $V_{COMPHI} - V_{COMPLO} \leq 1V$. Higher voltage swings are valid but AC performance may degrade.
- Note 16:** $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 1$.
- Note 17:** Waveform settles to within 5% of final value into load 100k Ω .
- Note 18:** $I_{PMU} = \pm 2mA$ at $V_{FORCE} = -2.2V$, $+1.5V$, and $+5.2V$. Percent variation relative to value calculated at $V_{FORCE} = +1.5V$.
- Note 19:** Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_.
- Note 20:** Load at end of 2ns transmission line; for stability only, AC performance may be degraded.
- Note 21:** The driver meets all of its timing specifications over the specified digital input voltage range.
- Note 22:** Timing characteristics with $V_L = 3V$.
- Note 23:** Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.
- Note 24:** All channels driven at 3V $_{P-P}$, load = 2ns, 50 Ω transmission line terminated with 3pF.

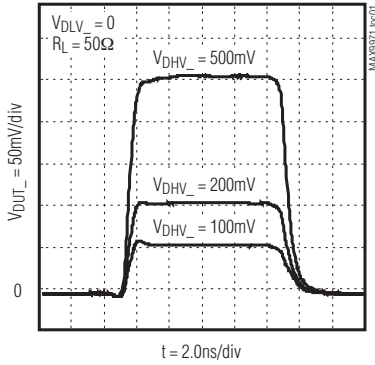
四通道、超低功耗、300Mbps ATE驱动器/比较器

典型工作特性

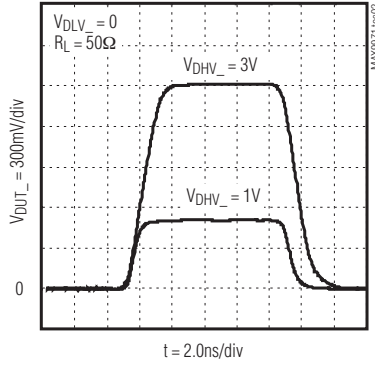
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

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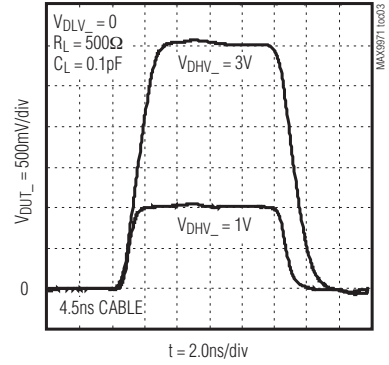
DRIVER SMALL-SIGNAL RESPONSE



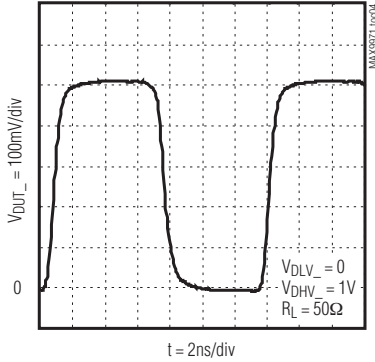
DRIVER LARGE-SIGNAL RESPONSE



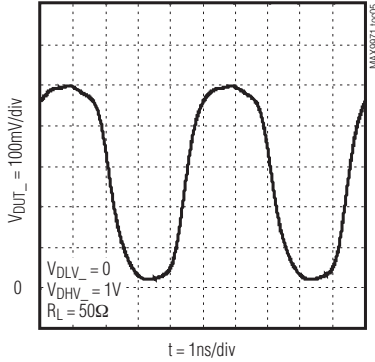
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



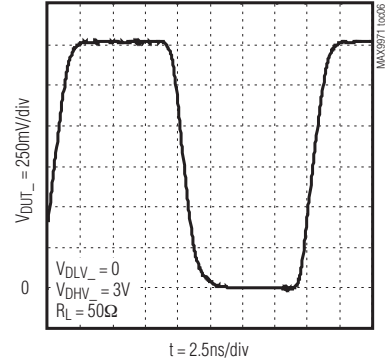
DRIVER 1Vp-p, 150Mbps SIGNAL RESPONSE



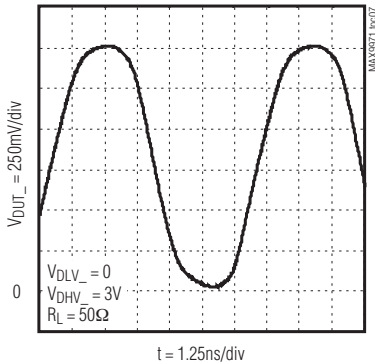
DRIVER 1Vp-p, 400Mbps SIGNAL RESPONSE



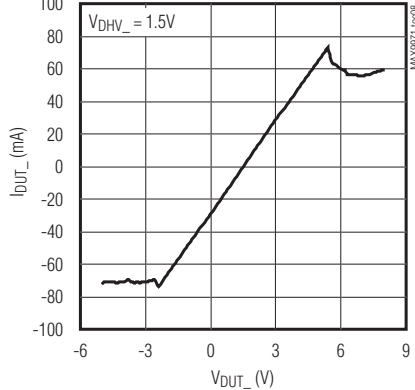
DRIVER 3Vp-p, 100Mbps SIGNAL RESPONSE



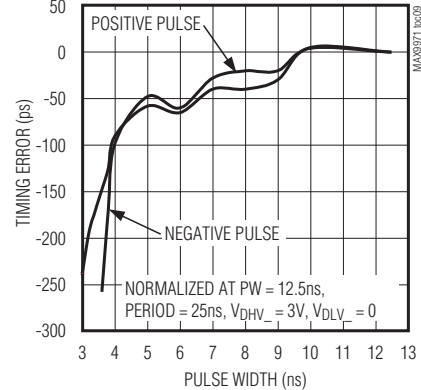
DRIVER 3Vp-p, 250Mbps SIGNAL RESPONSE



DRIVER DC CURRENT-LIMIT AND OVERVOLTAGE RESPONSE



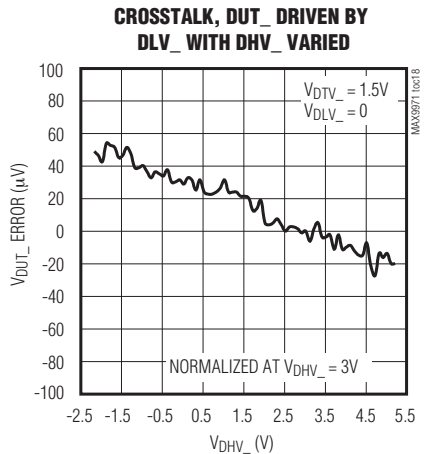
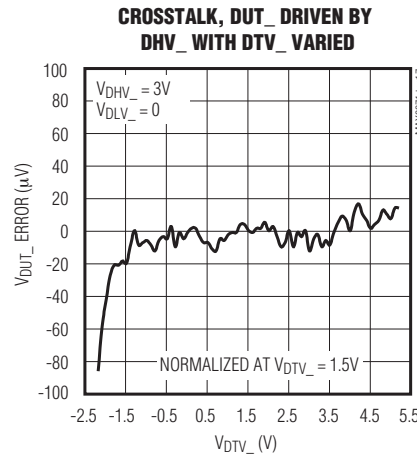
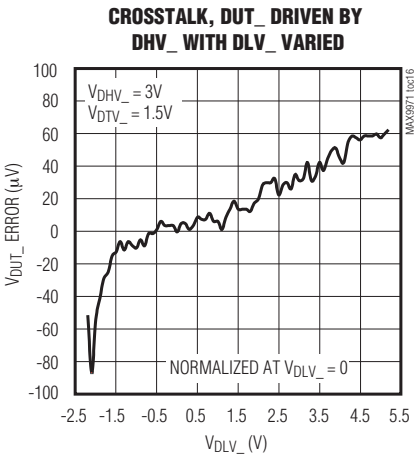
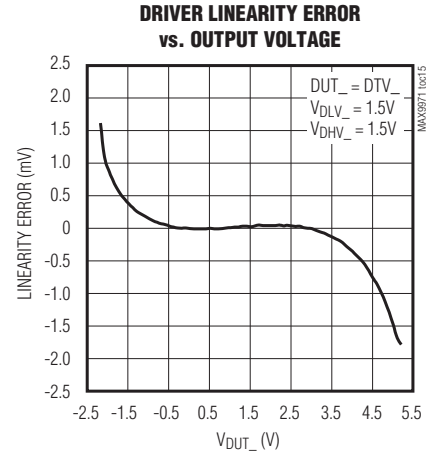
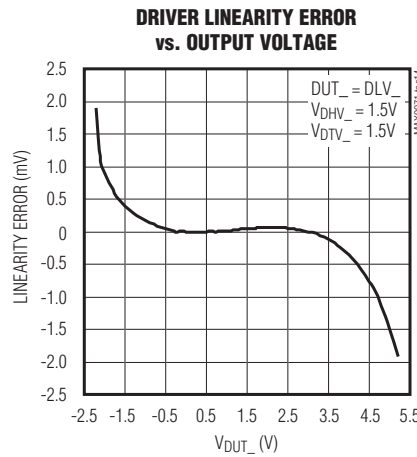
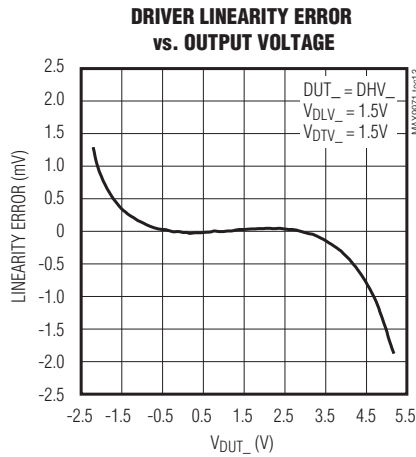
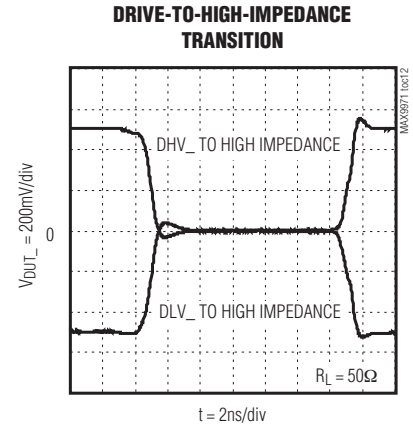
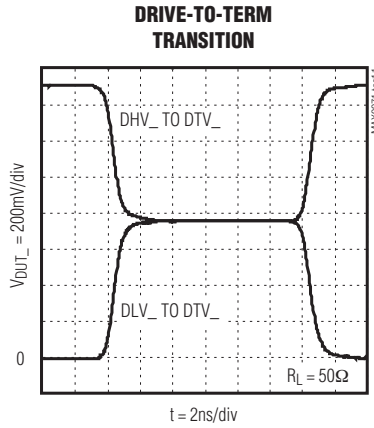
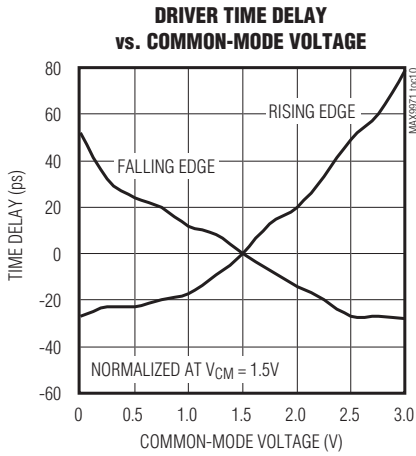
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



四通道、超低功耗、300Mbps ATE驱动器/比较器

典型工作特性(续)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

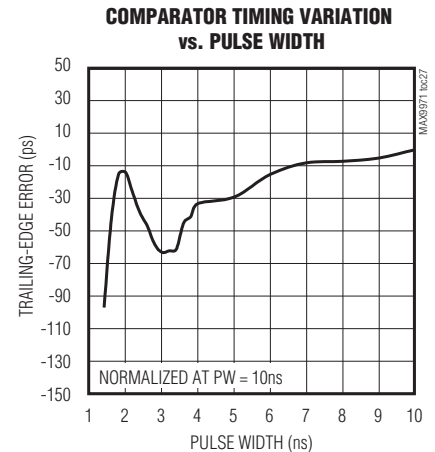
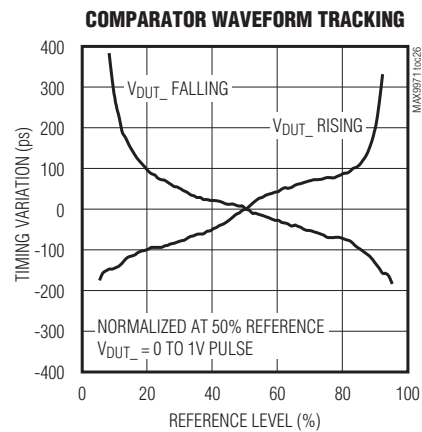
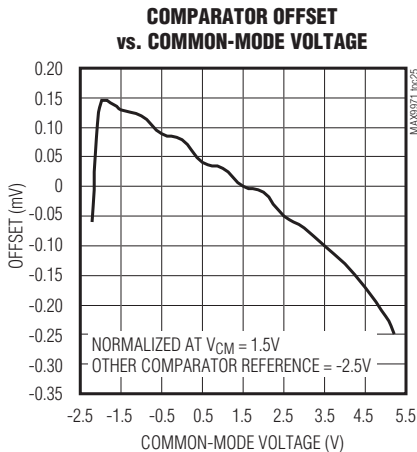
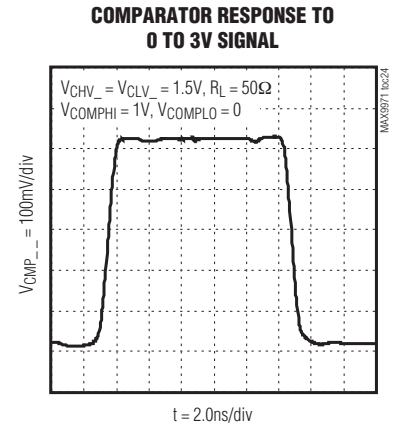
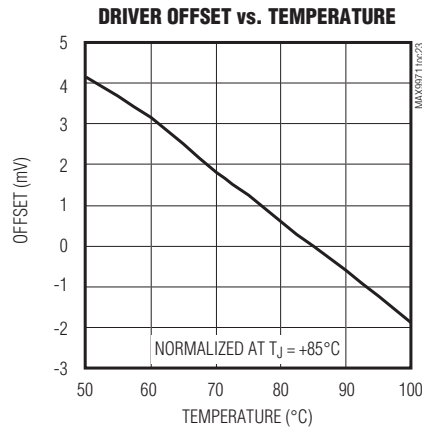
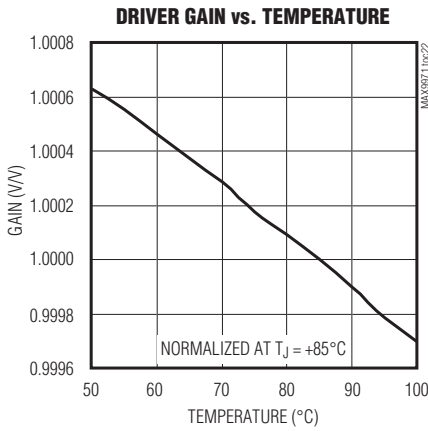
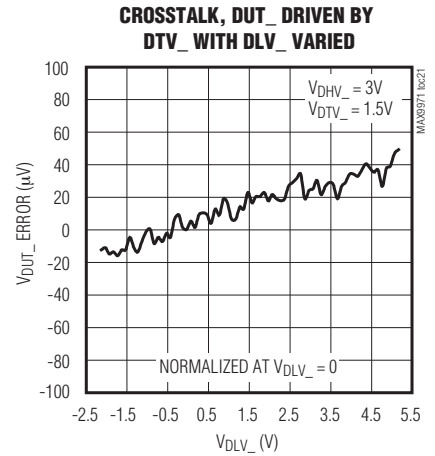
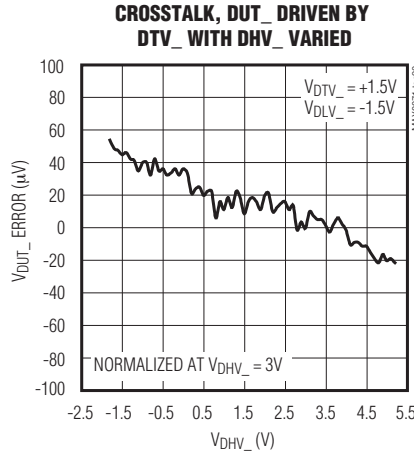
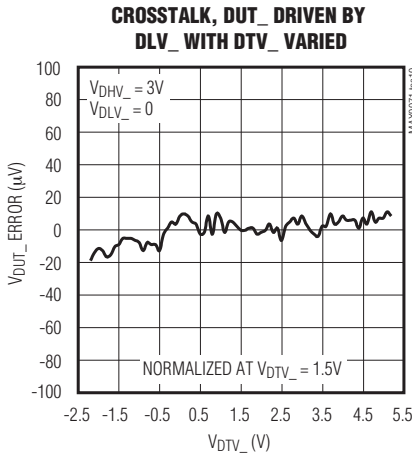


四通道、超低功耗、300Mbps ATE驱动器/比较器

典型工作特性(续)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

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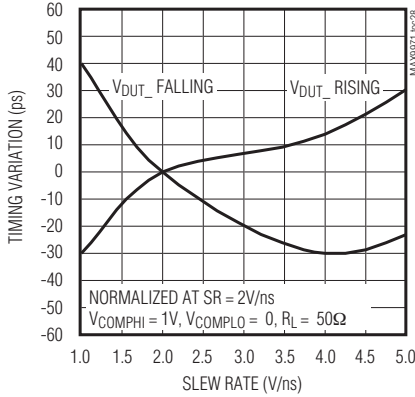


四通道、超低功耗、300Mbps ATE驱动器/比较器

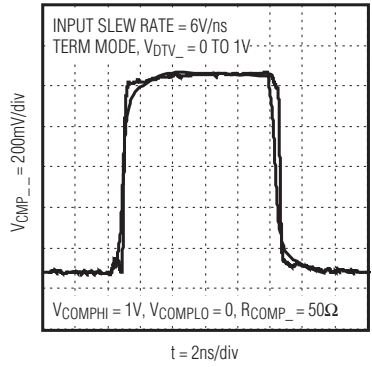
典型工作特性(续)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

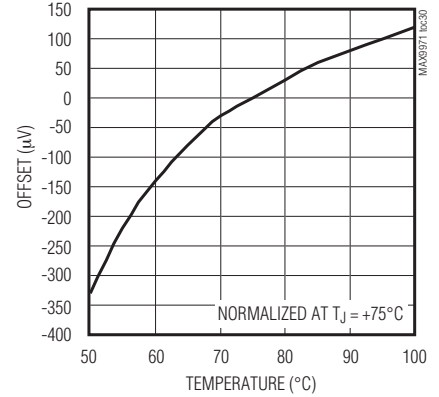
**COMPARATOR TIMING VARIATION
vs. INPUT SLEW RATE**



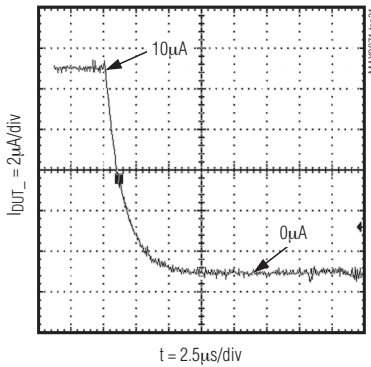
**COMPARATOR RESPONSE
vs. HIGH SLEW-RATE OVERDRIVE**



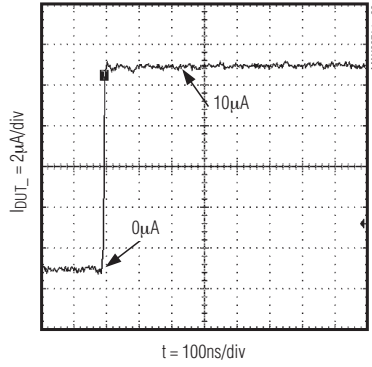
**COMPARATOR OFFSET
vs. TEMPERATURE**



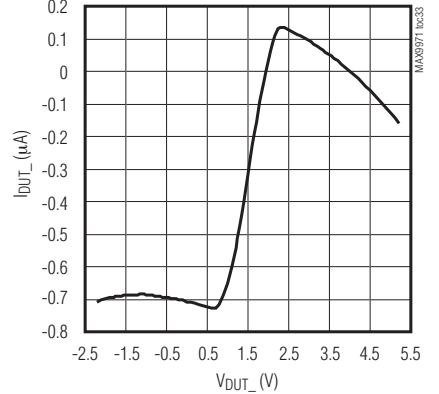
DRIVE 1V TO LOW-LEAKAGE TRANSITION



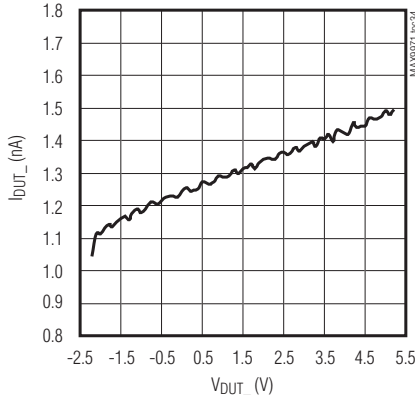
LOW LEAKAGE TO DRIVE 1V TRANSITION



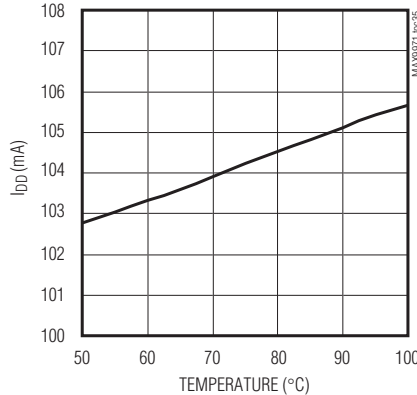
**HIGH-IMPEDANCE LEAKAGE AT DUT_
vs. DUT_ VOLTAGE**



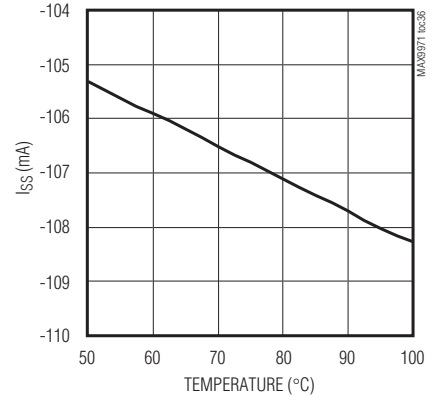
**LOW-LEAKAGE CURRENT
vs. DUT_ VOLTAGE**



**I_DD SUPPLY CURRENT
vs. TEMPERATURE**



**I_SS SUPPLY CURRENT
vs. TEMPERATURE**



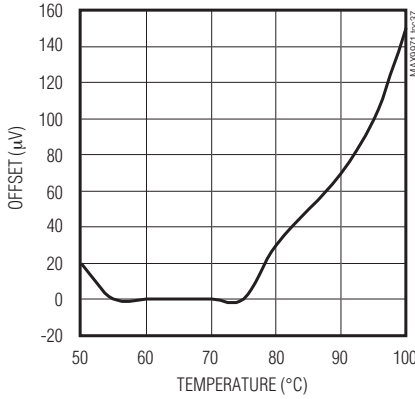
四通道、超低功耗、300Mbps ATE驱动器/比较器

典型工作特性(续)

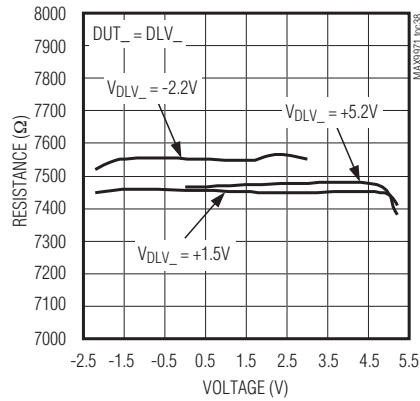
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX9972

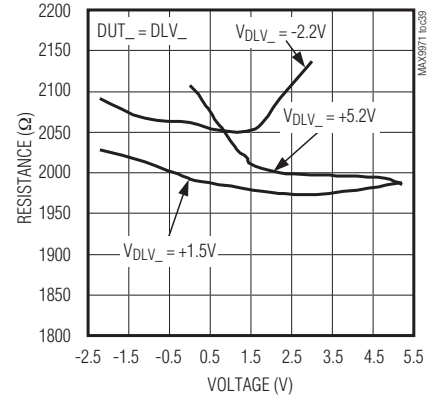
**PASSIVE LOAD OFFSET
vs. TEMPERATURE**



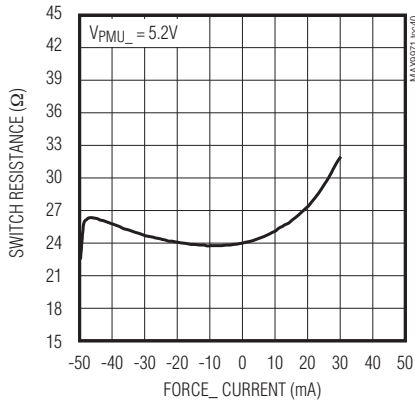
**PASSIVE LOAD HIGH RESISTOR
vs. VOLTAGE**



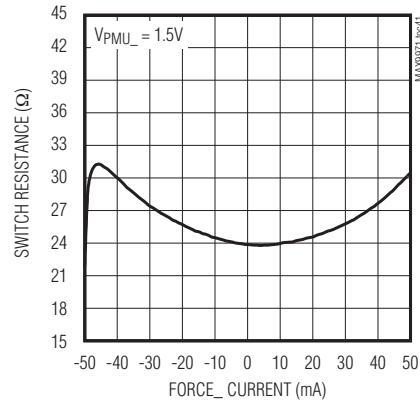
**PASSIVE LOAD LOW RESISTOR
vs. VOLTAGE**



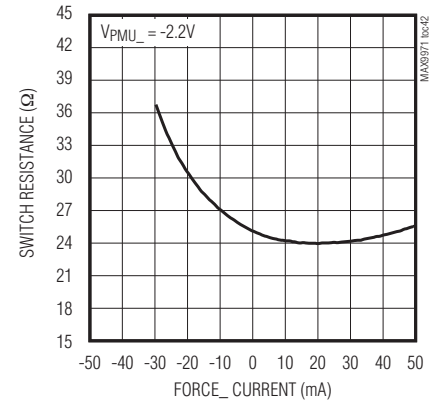
**PMU_FORCE_SWITCH RESISTANCE
vs. FORCE_CURRENT**



**PMU_FORCE_SWITCH RESISTANCE
vs. FORCE_CURRENT**



**PMU_FORCE_SWITCH RESISTANCE
vs. FORCE_CURRENT**



四通道、超低功耗、300Mbps ATE驱动器/比较器

MAX9972

引脚说明

引脚	名称	功能
1	DATA1	通道1复用器控制输入。驱动模式下，用来选择DHV1或DLV1作为驱动器1的输入，见表1和图2。
2	RCV1	通道1复用器控制输入，将通道1置为驱动或接收模式，见表1和图2。
3, 8, 13, 18, 51	GND	模拟地。
4	CMPH1	通道1高端比较器输出。
5	CMPL1	通道1低端比较器输出。
6	DATA2	通道2复用器控制输入。驱动模式下，用来选择DHV2或DLV2作为驱动器2的输入，见表1和图2。
7	RCV2	通道2复用器控制输入。将通道2置为驱动或接收模式，见表1和图2。
9	CMPH2	通道2高端比较器输出。
10	CMPL2	通道2低端比较器输出。
11	CMPL3	通道3低端比较器输出。
12	CMPH3	通道3高端比较器输出。
14	RCV3	通道3复用器控制输入。将通道3置为驱动或接收模式，见表1和图2。
15	DATA3	通道3复用器控制输入。驱动模式下，用来选择DHV3或DLV3作为驱动器3的输入，见表1和图2。
16	CMPL4	通道4低端比较器输出。
17	CMPH4	通道4高端比较器输出。
19	RCV4	通道4复用器控制输入。将通道4置为驱动或接收模式，见表1和图2。
20	DATA4	通道4复用器控制输入。驱动模式下，用来选择DHV4或DLV4作为驱动器4的输入，见表1和图2。
21	DHV4	通道4驱动器高压输入。
22	DLV4	通道4驱动器低压输入。
23	DTV4	通道4驱动器端接电压输入。
24	CHV4	通道4高端比较器门限电压输入。
25	CLV4	通道4低端比较器门限电压输入。
26	DHV3	通道3驱动器高压输入。
27	DLV3	通道3驱动器低压输入。
28	DTV3	通道3驱动器端接电压输入。
29	CHV3	通道3高端比较器门限电压输入。
30	CLV3	通道3低端比较器门限电压输入。
31	DGND	数字地。
32	DOUT	串口数据输出。
33	$\overline{\text{LD}}$	负载输入。在时钟上升沿，将串行输入寄存器的数据锁存到控制寄存器。低电平时，数据为透明传输。
34	DIN	串行接口数据输入。
35	SCLK	串行时钟。
36	$\overline{\text{CS}}$	片选。
37	SENSE4	通道4 PMU检测连接。
38	FORCE4	通道4 PMU加载连接。

四通道、超低功耗、300Mbps ATE驱动器/比较器

引脚说明(续)

MAX9972

引脚	名称	功能
39	SENSE3	通道3 PMU 检测连接。
40	FORCE3	通道3 PMU 加载连接。
41	TEMP	温度传感器输出。
42, 47, 52, 56, 60	V _{DD}	正电源输入。
43	DUT4	通道4被测设备连接, 用于通道4的驱动器、比较器和负载I/O节点。
44	PMU4	通道4参数测量连接, 用于通道4的PMU开关I/O节点。
45, 50, 53, 57	V _{SS}	负电源输入。
46	V _L	逻辑电源输入。
48	DUT3	通道3被测设备连接, 用于通道3的驱动器、比较器和负载I/O节点。
49	PMU3	通道3参数测量连接, 用于通道3的PMU开关I/O节点。
54	PMU2	通道2参数测量连接, 用于通道2的PMU开关I/O节点。
55	DUT2	通道2被测器件连接, 用于通道2的驱动器、比较器和负载I/O节点。
58	PMU1	通道1参数测量连接, 用于通道1的PMU开关I/O节点。
59	DUT1	通道1被测器件连接, 用于通道1的驱动器、比较器和负载I/O节点。
61	FORCE2	通道2 PMU 加载连接。
62	SENSE2	通道2 PMU 检测连接。
63	FORCE1	通道1 PMU 加载连接。
64	SENSE1	通道1 PMU 检测连接。
65	COMPLO	比较器输出低电平参考输入。
66	COMPHI	比较器输出高电平参考输入。
67	LDV4	通道4负载电压输入。
68	LDV3	通道3负载电压输入。
69	LDV2	通道2负载电压输入。
70	LDV1	通道1负载电压输入。
71	CLV2	通道2低端比较器门限电压输入。
72	CHV2	通道2高端比较器门限电压输入。
73	DTV2	通道2驱动器端接电压输入。
74	DLV2	通道2驱动器低压输入。
75	DHV2	通道2驱动器高压输入。
76	CLV1	通道1低端比较器门限电压输入。
77	CHV1	通道1高端比较器门限电压输入。
78	DTV1	通道1驱动器端接电压输入。
79	DLV1	通道1驱动器低压输入。
80	DHV1	通道1驱动器高压输入。
—	EP	裸焊盘, 浮空或接至V _{SS} 。

四通道、超低功耗、300Mbps ATE驱动器/比较器

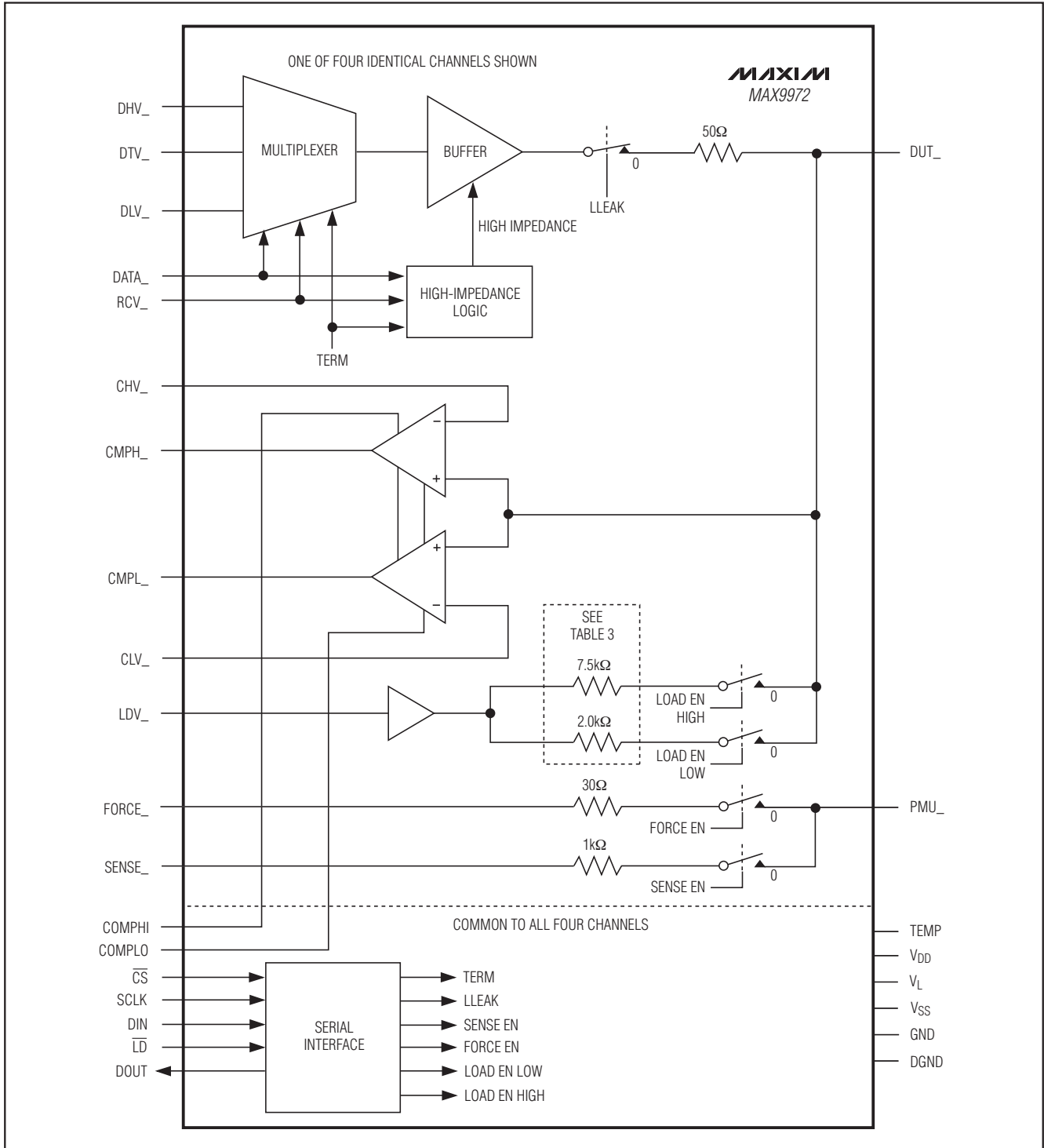


图1. 功能框图

四通道、超低功耗、300Mbps ATE驱动器/比较器

详细说明

MAX9972为四通道、引脚电子测量IC，用于自动测试设备，每通道包括三电平引脚驱动器、窗口比较器、无源负载和Kelvin仪表连接(图1)。所有电路工作在-2.2V至+5.2V电压范围，且驱动器包含高阻和有源端接(第3级驱动)工作模式。比较器具有可编程输出电压，允许针对不同的CMOS接口标准进行优化。负载具有可选的输出阻抗，允许优化DUT的加载电流。Kelvin连接可实现精确测量，提供±25mA的源出电流和吸入电流。另外，MAX9972提供低泄漏模式，可将DUT_漏电流降至20nA以下。

MAX9972提供两种精度等级。A级器件具有精确的驱动器增益和失调匹配、比较器失调匹配以及负载电阻。在对成本敏感的应用中，可以使多个通道共用基准电压。B级器件适用于每通道具有独立基准的系统设计。

4个通道中的每一通道均具有单端CMOS兼容输入：DATA_和RCV_，用于控制信号驱动通道(图2)。MAX9972通过3线、低压CMOS逻辑兼容的串口编程设置运行模式。

输出驱动器

驱动器输入级为高速多路复用器，可选择DHF_、DLV_或DTV_三个电压之一作为输入。信号切换通过高速输入DATA_、RCV_以及模式控制位TERM进行控制(表1)。DATA_和RCV_为单端输入，门限电压等于 $V_L/2$ 。每通道的门限电压独立产生，以保证串扰最小。

DUT_可在缓冲器输出和高阻模式之间高速切换，也可置为低泄漏模式(图2和表1)。通过高速输入RCV_和模式控制位TERM、LLEAK选择这些模式。高阻模式下，DUT_的偏置电流在-2.2V至+5.2V电压范围内小于 $2\mu\text{A}$ ，而且节点能够保持其高速信号跟踪能力。低泄漏模式下，DUT_的偏置电流进一步降至20nA以下，信号跟踪速度减缓。

驱动器输出阻抗标称值为 50Ω ，若需 45Ω 至 51Ω 范围内的不同阻值，请与厂商联系。

表1. 驱动器通道控制信号

EXTERNAL CONNECTIONS		INTERNAL CONTROL BITS		DRIVER OUTPUT	DRIVER MODE
RCV_	DATA_	TERM	LLEAK		
0	0	X	0	DUT_ = DLV_	Drive
0	1	X	0	DUT_ = DHV_	Drive
1	X	0	0	High Impedance	Receive
1	X	1	0	DUT_ = DTV_	Receive
X	X	X	1	Low Leak	Low Leakage

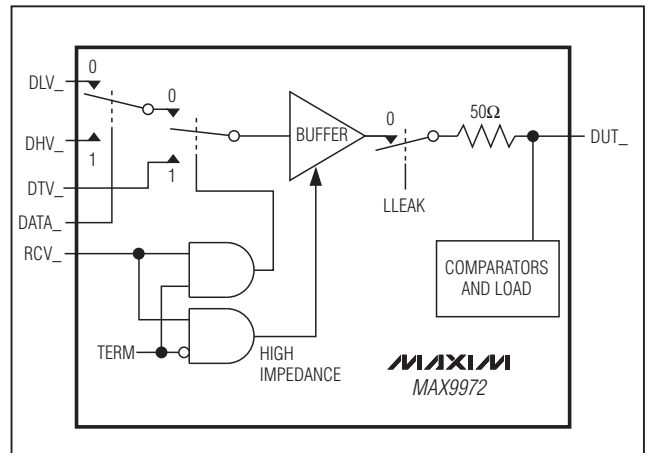


图2. 复用器和驱动器通道

四通道、超低功耗、300Mbps ATE驱动器/比较器

比较器

MAX9972为每一通道提供两个独立的高速比较器。每个比较器的一路输入由内部连接至DUT₋，另外一路连接至CHV₋或CLV₋(见图1)。如表2所示，比较器输出为输入条件的逻辑运算结果。

比较器输出电压可以很容易地与多种逻辑标准接口。利用经过缓冲的COMPHI和COMPLO设置输出高、低电平。为保证正常工作，COMPHI电压应大于或等于COMPLO电压。比较器50Ω输出阻抗提供信号源端接(图3)。

无源负载

MAX9972四个通道中的每一通道均具有无源负载，无源负载包含经过缓冲的输入电压LDV₋，该电压通过两个电阻通路连接到DUT₋(图1)。每条通路经过由串口控制的开关独立连接至DUT₋。设置选项包括悬空(未接负载)、连接任意一路或两路。电阻值的选取由器件的精度等级确定，如表3所示。该负载简化了与比较器连接时的快速开路/短路测试，以及漏极开路DUT₋输出的上拉。

参数开关

MAX9972四个通道中的每个通道可提供加载、检测路径，将PMU或其它直流源连接至被测设备(图1)。每个加载、检测开关通过串口独立控制，具有极高的应用灵活性。PMU₋和DUT₋采用独立引脚，无需参数开关，消除了PMU₋上的附加电容。还允许PMU₋直接或通过阻抗匹配网络连接至DUT₋。

低泄漏模式，LLEAK

通过串口置位LLEAK将使MAX9972进入超低泄漏模式(参考*Electrical Characteristics*)。这种模式可以方便地完成IDDQ和PMU测量，不需要输出断开继电器。对于每个通道，LLEAK控制互相独立。

如果DUT₋以高速信号驱动时LLEAK置位，泄漏电流将瞬间增大并超过正常工作的限制。*Electrical Characteristics*表中的低泄漏恢复指标给出了器件在这种条件下的运行状态。

温度监视

每个器件提供温度输出信号TEMP，管芯温度为+70°C(343K)时输出标称值为3.43V的电压。该输出电压以10mV/°C的比例随温度线性增长，温度传感器输出阻抗为500Ω(典型值)。

表2. 比较器逻辑

DUT ₋ > CHV ₋	DUT ₋ > CLV ₋	CMPH ₋	CMPL ₋
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

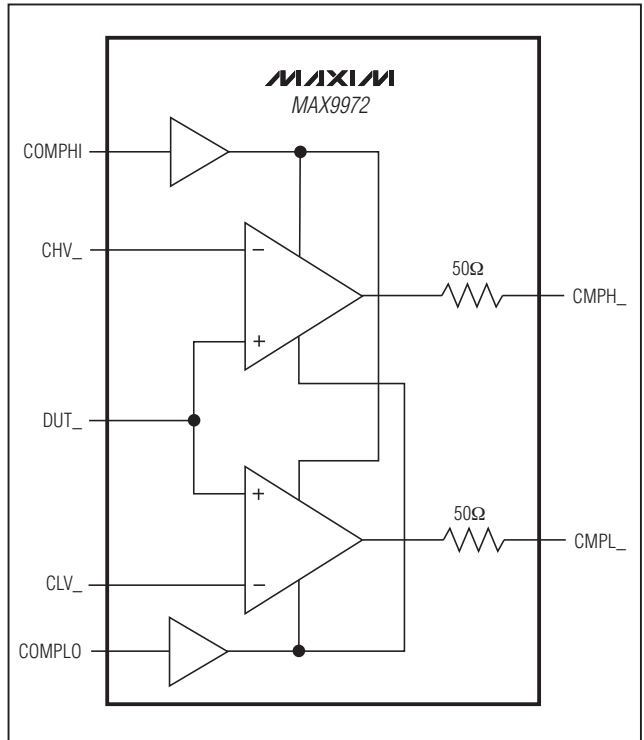


图3. 比较器50Ω互补输出

表3. 无源负载电阻值

ACCURACY GRADE	HIGH RESISTOR (kΩ)	LOW RESISTOR (kΩ)
A	7.5	2
B	6	1.5

四通道、超低功耗、300Mbps ATE驱动器/比较器

串口和器件控制

CMOS兼容的串行接口控制MAX9972的工作模式(图4)。控制数据移入一个12位移位寄存器(LSB在前),并在 \overline{CS} 变为高电平时锁存该数据。如图4、表4所示,来自移位寄存器的数据装载到其中一个或所有通道的锁存器,具体

由D8–D11位决定。锁存器为器件的每个通道提供6位模式控制位。模式位配合外部输入DATA_、RCV_管理每个通道的功能。强制 \overline{LD} 为低电平时,数据将从输入寄存器异步传送到通道寄存器。保持 \overline{LD} 为低电平,在 \overline{CS} 上升沿传输数据。

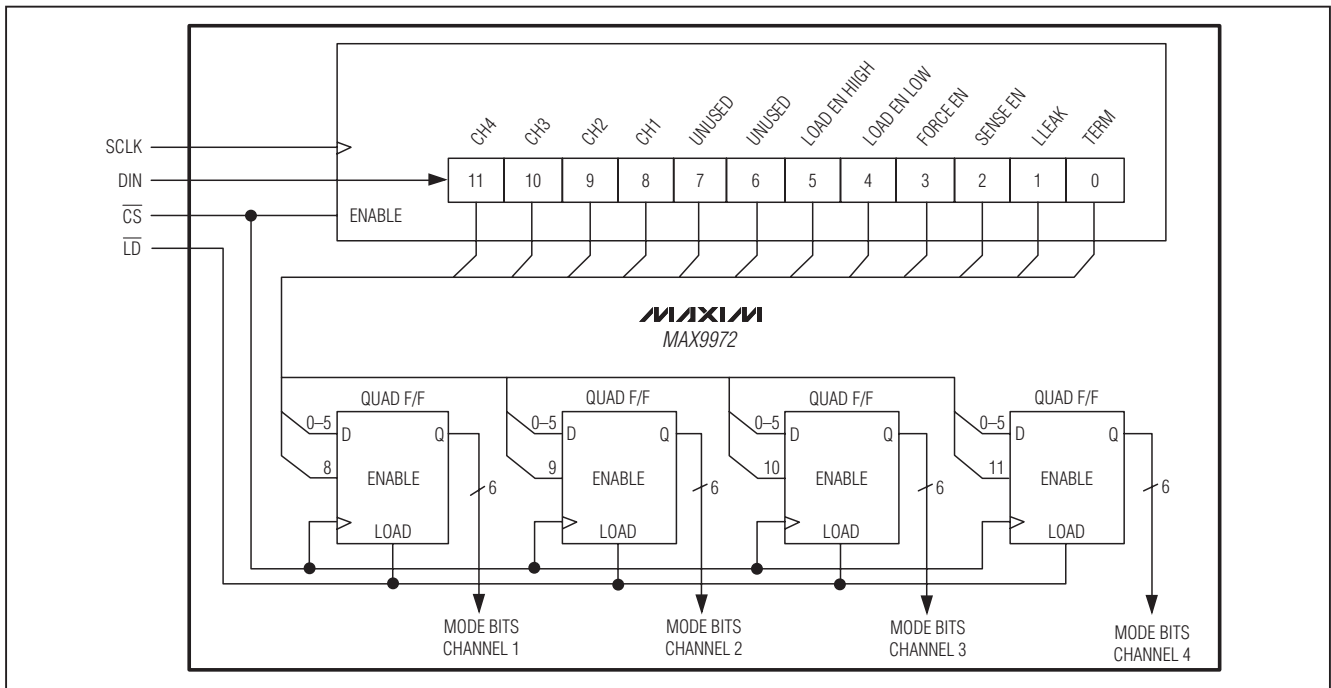


图4. 串行接口

表4. 控制寄存器位的功能

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
0	TERM	Term Mode Control	High Impedance	Term Mode	0
1	LLEAK	Assert Low-Leakage Mode	Term Mode	Low Leakage	0
2	SENSE EN	Enable Sense Switch	Disabled	Enabled	0
3	FORCE EN	Enable Force Switch	Disabled	Enabled	0
4	LOAD EN LOW	Enable Low Load Resistor	Disabled	Enabled	0
5	LOAD EN HIGH	Enable High Load Resistor	Disabled	Enabled	0
6	—	Unused	X	X	0
7	—	Unused	X	X	0
8	CH1	Update Channel 1 Control Register	Disabled	Enabled	1
9	CH2	Update Channel 2 Control Register	Disabled	Enabled	1
10	CH3	Update Channel 3 Control Register	Disabled	Enabled	1
11	CH4	Update Channel 4 Control Register	Disabled	Enabled	1

四通道、超低功耗、300Mbps ATE驱动器/比较器

MAX9972

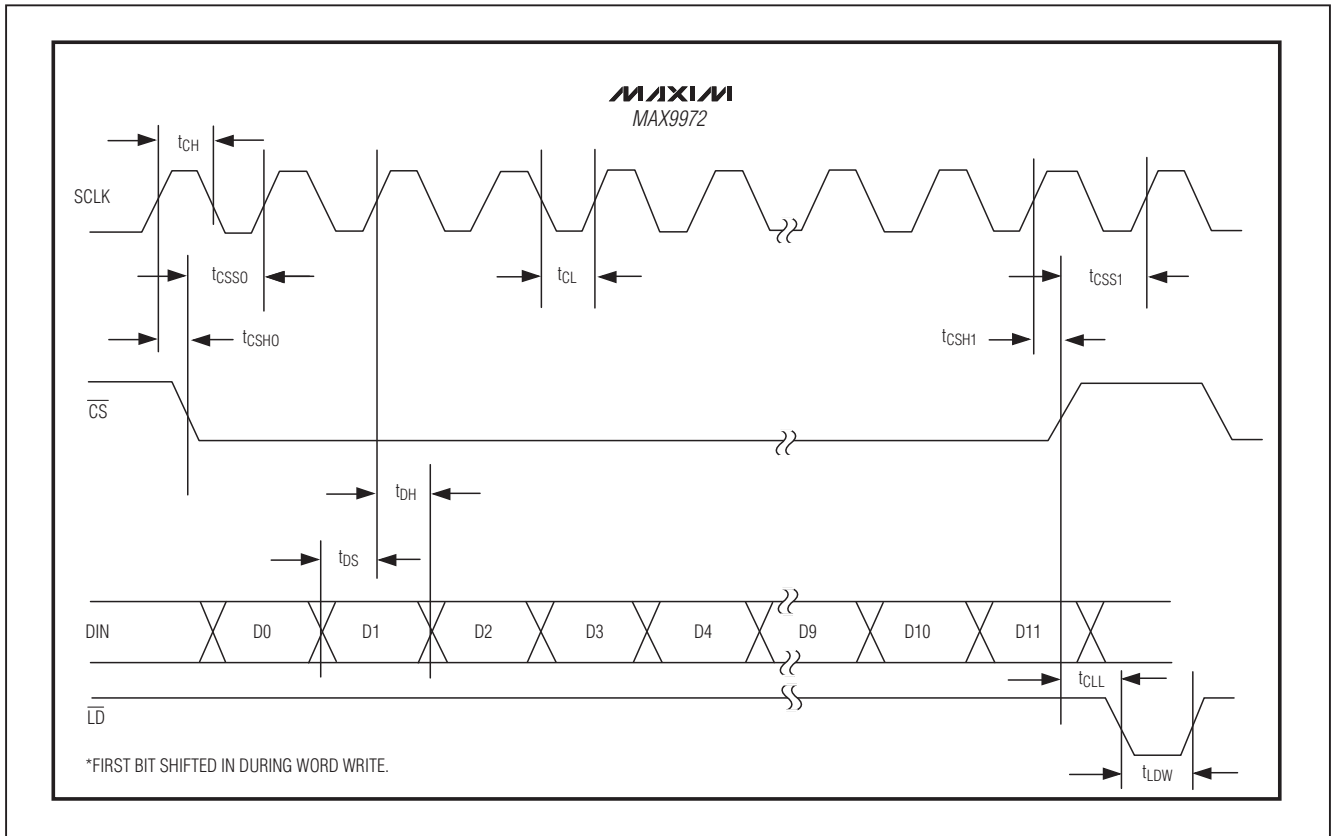


图5. 串口时序

散热

正常通风环境中，多数工作条件下器件不需要外部散热器。如果出现过热，则需要将裸焊盘焊接至电路板的覆铜层。裸焊盘必须保持浮空、隔离或连接至 V_{SS} 。

降低功耗

为降低功耗，可以只启动所需要的通道。每个通道工作在低泄漏模式时，可节省约240mW的功耗。

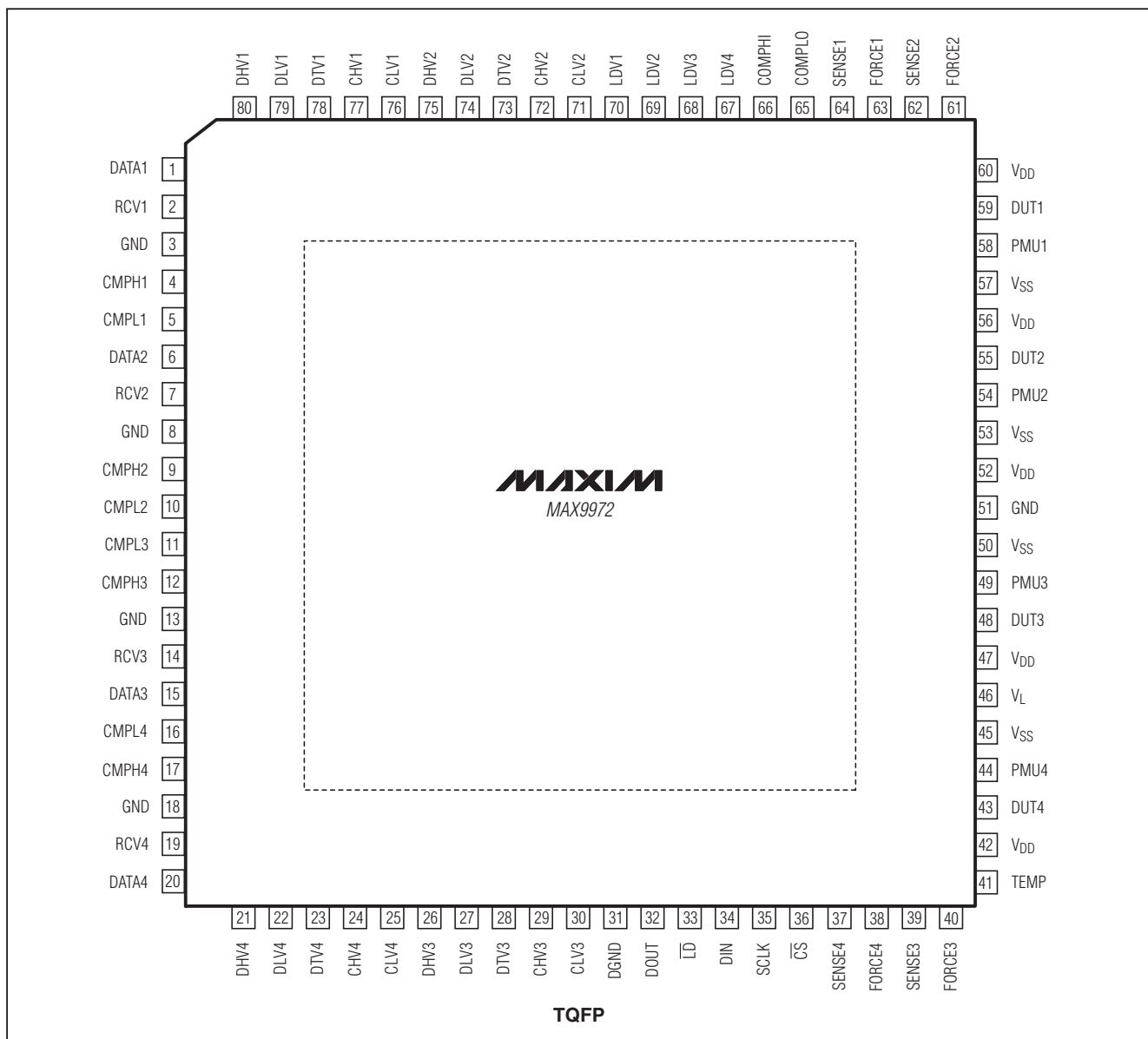
芯片信息

PROCESS: BiCMOS

四通道、超低功耗、300Mbps ATE驱动器/比较器

引脚配置

MAX9972



封装信息

如需最近的封装外形信息和焊盘布局，请查询 china.maxim-ic.com/packages。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	文档编号
80 TQFP-EP	C80E-4	21-0115

四通道、超低功耗、300Mbps ATE驱动器/比较器

修订历史

修订号	修订日期	说明	修改页
0	6/06	最初版本。	—
1	7/09	更改了 <i>Electrical Characteristics</i> 表中的驱动器失调电压最大值，并删除了MAX9971的所有相关内容。	1-22

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