ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}).....-0.5V to +4.1V
Continuous Output Current Range
(OUT+, OUT-) .....-25mA to +25mA
Input Voltage Range (IN+, IN-) .....-0.5V to (V_{CC} + 0.5V)
Logic Inputs Range (PE1, PE0,
TX_DISABLE, IN_LEV, OUT_LEV) .....-0.5V to (V_{CC} + 0.5V)
LOS Open-Collector Supply Voltage Range
(with ≥ 4.7kΩ pullup) .....-0.5V to +5.5V
Storage Ambient Temperature Range (T_{STG}) ...-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply Noise Tolerance		1MHz ≤ f < 2GHz		40		mV_{P-P}
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data	1.0	8.5	10.3	Gbps
Consecutive Identical Digits (CID)		CID (bits)			100	Bits
Input Swing (Measured differentially at data source, point A of Figure 2 and 3. Pins LOS and TX_DISABLE are floating.)		IN_LEV = high, Figure 2; 4.25Gbps < data rate ≤ 10.3Gbps	360		1200	mV_{P-P}
		IN_LEV = high, Figure 2; 1.25Gbps < data rate ≤ 4.25Gbps	360		1600	
		IN_LEV = high, Figure 2; 1.0Gbps ≤ data rate ≤ 1.25Gbps	360		2400	
		IN_LEV = low, Figure 3; 1.0Gbps < data rate ≤ 10.3Gbps	100		360	
Time to Reach 50% Mark/Space Ratio					1	µs

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	OUT_LEV = low, TX_DISABLE = low		100	124	mA
		OUT_LEV = high, TX_DISABLE = low		120	148	
Inrush Current		Beyond steady state supply current (Note 1)			10	mA
Power-On Delay		(Note 1)	1		30	ms
EQUALIZER AND DRIVE SPECIFICATIONS						
Input Return Loss	S11	100MHz to 5GHz		10		dB
Input Resistance		Measured differentially (Note 2)	85	100	115	Ω
Different Output Swing (Notes 3, 4)		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high, PE1 = PE0 = high	1000		1300	mV_{P-P}
		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = low, PE1 = PE0 = high	800		1100	
		TX_DISABLE = high, PE1 = PE0 = high			10	
Common-Mode Output (AC) (Note 4)		Measured at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high (Note 5)			25	mV_{RMS}
Output Resistance	R_{OUT}	OUT+ or OUT-, single-ended	42	50	58	Ω
Output Return Loss	S22	100MHz to 5GHz		12		dB
Output Transition Time 20% to 80%	t_r, t_f	20% to 80% (Note 6)		32	40	ps
Random Jitter (Note 4)		Measured at point D in Figure 3 (Note 7)			0.8	ps_{RMS}
Output Preemphasis		Figure 1 (Note 3) PE1 = 0, PE0 = 0		3.5		dB
		Figure 1 (Note 3) PE1 = 0, PE0 = 1		6.5		
		Figure 1 (Note 3) PE1 = 1, PE0 = 0		9.5		
		Figure 1 (Note 3) PE1 = 1, PE0 = 1		13		
Residual Output Deterministic Jitter at 1.0Gbps (Notes 4, 8, and 9)		Source to IN: 6-mil, 10in of FR-4; OUT to load: 3m, 24 AWG; PE1 = 0, PE0 = 0			0.02	UI_{P-P}
		Source to IN: 6-mil, 10in of FR-4; OUT to load: 5m, 24 AWG; PE1 = 0, PE0 = 1				
		Source to IN: 6-mil, 10in of FR-4; OUT to load: 7m, 24 AWG; PE1 = 1, PE0 = 0				
		Source to IN: 6-mil, 10in of FR-4; OUT to load: 10m, 24 AWG; PE1 = 1, PE0 = 1				

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
Residual Output Deterministic Jitter at 5.0Gbps (Notes 4, 8, and 9)		Source to IN	OUT to load	PE1	PE0				
		6-mil, 10in of FR-4	3m, 24 AWG	0	1		0.09	0.12	UI_{P-P}
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 8.5Gbps (Notes 4, 8, and 9)		Source to IN	OUT to load	PE1	PE0				
		6-mil, 10in of FR-4	3m, 24 AWG	0	1		0.15	0.20	UI_{P-P}
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 10Gbps (Notes 4, 8, and 9)		Source to IN	OUT to load	PE1	PE0				
		6-mil, 10in of FR-4	3m, 24 AWG	0	1		0.18	0.25	UI_{P-P}
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	1				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 10.0Gbps (Notes 4, 8, and 10)		10in of FR-4 at OUT±; no cable; see Figure 3		PE1	PE0		0.10		UI_{P-P}
				0	0				
Propagation Delay							230		ps
STATUS OUTPUT: LOS									
LOS Deassert		IN_LEV = high (Note 11)						300	mV_{P-P}
		IN_LEV = low (Note 11)						100	
LOS Assert		IN_LEV = high (Note 11)				80			
LOS Hysteresis (Note 4)		IN_LEV = high (Note 11)				20			mV_{P-P}
		IN_LEV = low (Note 11)					10		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOS Open-Collector Current Sink		LOS asserted	0		25	µA
		LOS asserted; $V_{OL} \le 0.4V$	1.0			mA
		(Note 12)	0		25	µA
LOS Response Time (Note 4)		Time from V_{IN} dropping below deassert level or rising above assert level to 50% point of LOS output transition			10	µs
LOS Transition Time		Rise time or fall time (10% to 90%); pullup supply = 5.5V; external pullup R ≥ 4.7kΩ		200		ns
CONTROL INPUTS: TX_DISABLE, PE0, PE1, OUT_LEV, IN_LEV						
Logic-High Voltage	V_{IH}		2.0			V
Logic-Low Voltage	V_{IL}				0.8	V
Logic-High Current	I_{IH}	Current required to maintain logic-high state at V_{IH} > +2.0V			-150	µA
Logic-Low Current	I_{IL}	Current required to maintain logic-low state at V_{IL} < +0.8V			350	µA

Note 1: Supply voltage to reach 90% of final value in less than 100µs, but not less than 10µs. Power-on delay interval measured from the 50% level of the final voltage at the filter's device side to 50% level of final current. The supply is to remain at or above 3V for at least 100ms. Only one full-scale transition is permitted during this interval. Aberrations on the transition are limited to less than 100mV.

Note 2: IN+ and IN- are single-ended, 50Ω terminations to (V_{CC} - 1.5V) ±0.2V.

Note 3: Load is 50Ω ±1% at each side and the pattern is 0000011111 or equivalent pattern at 2.5Gbps.

Note 4: Guaranteed by design and characterization.

Note 5: PE1 = PE0 = logic-high (maximum preemphasis), load is 50Ω ±1% at each side. The pattern is 11001100 (50% edge density) at 10Gbps. AC common-mode output is computed as:

$$V_{ACCM\_RMS} = RMS[(V_P + V_N) / 2) - V_{DCCM}]$$

where:
V_P = time-domain voltage measured at OUT+ with at least 10GHz bandwidth.
V_N = time-domain voltage measured at OUT- with at least 10GHz bandwidth.
AC common-mode voltage (V_{ACCM_RMS}) expressed as an RMS value.
DC common-mode voltage (V_{DCCM}) = average DC voltage of (V_P + V_N) / 2.

Note 6: Using 0000011111 or equivalent pattern at 2.5Gbps. PE0 = PE1 = logic-low for minimum preemphasis. Measured within 2in of the output pins with Rogers 4350 dielectric, or equivalent, and ≥ 10-mil line width. For transition time, the 0% reference is the steady state level after four zeros, just before the transition, and the 100% reference level is the steady state level after four consecutive logic ones.

Note 7: Pattern is 0000011111 or equivalent pattern at 10Gbps and 100mV_{P-P} differential swing. IN_LEV = logic-low and PE0 = PE1 = logic-low for minimum preemphasis. Signal transition time is controlled by the 4th-order BT filter (7.5GHz bandwidth) or equivalent. See Figure 3 for setup.

Note 8: Test pattern (464 bits): 100 zeros, 1010, PRBS7, 100 ones, 0101, PRBS7.

Note 9: Input range selection is IN_LEV = logic-high for FR-4 input equalization. Cables are unequalized, Amphenol Spectra-Strip (160-2499-997) 24 AWG or equivalent. Residual deterministic jitter is the difference between the source jitter at point A and the load jitter point D in Figure 2. The deterministic jitter (DJ) at the output of the transmission line must be from media induced loss and not from clock source modulation. DJ is measured at point D of Figure 2.

Note 10: Input range selection is IN_LEV = logic-low. Residual deterministic jitter is the difference between the source jitter at point A and the load jitter point D in Figure 3. The deterministic jitter (DJ) at the output of the transmission line must be from media induced loss and not from clock source modulation. DJ is measured at point D of Figure 3.

Note 11: Measured with 101010… pattern at 10Gbps with less than 1in of FR-4 at the input.

Note 12: True open-collector outputs. V_{CC} = 0 and the external 4.7kΩ pullup resistor is connected to +5.5V.

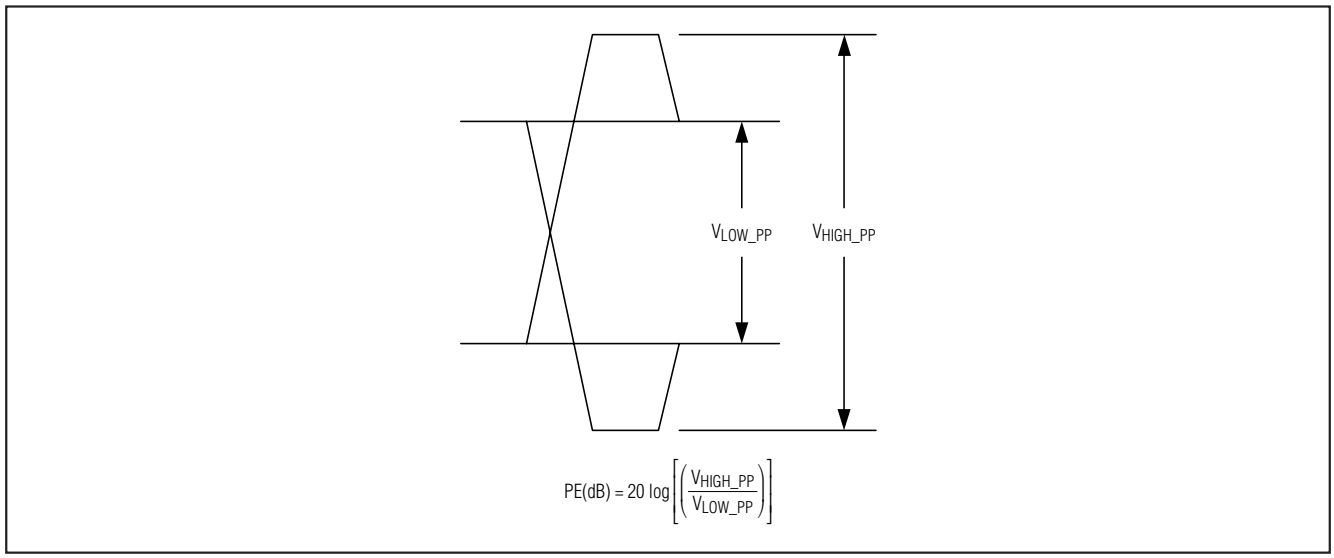


图1. 以dB表示的TX预加重

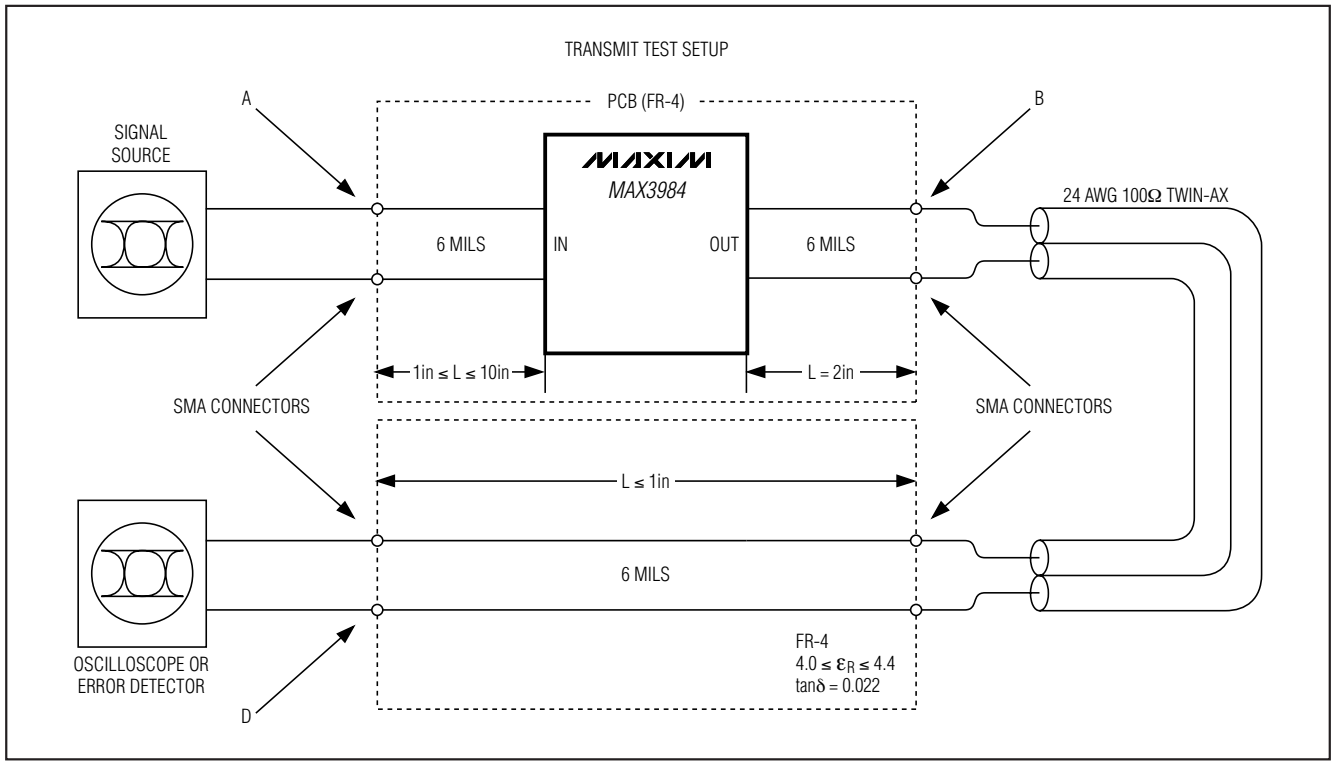


图2. 发送测试设置(标注为A、B、D的点为交流参数测试的参考点。在D点进行确定性抖动和眼图测量)。

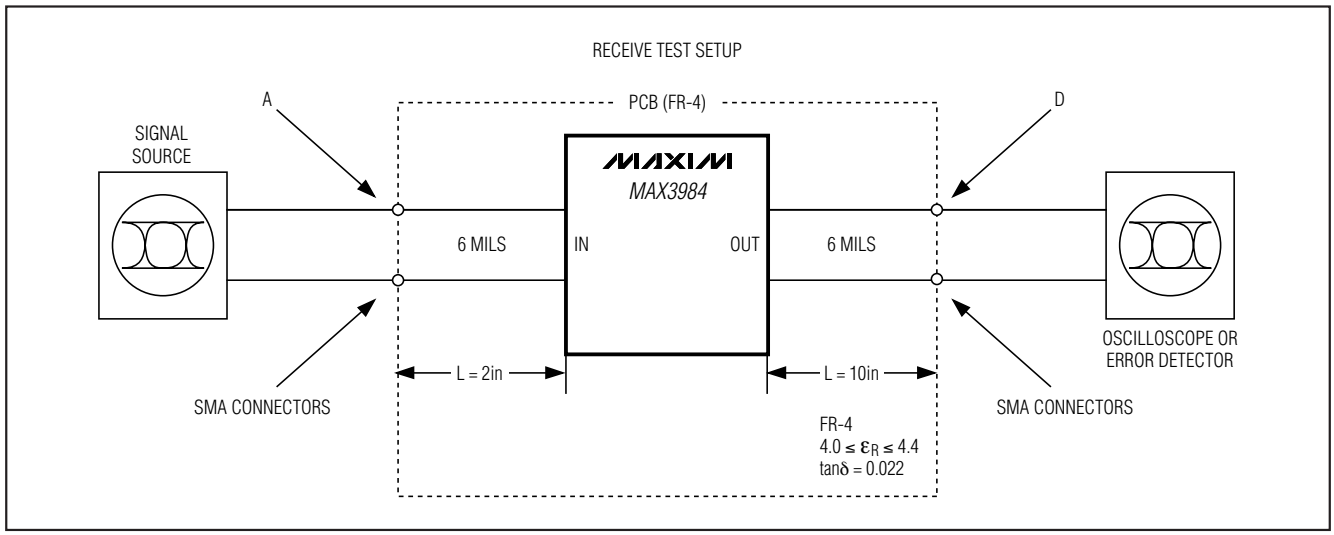
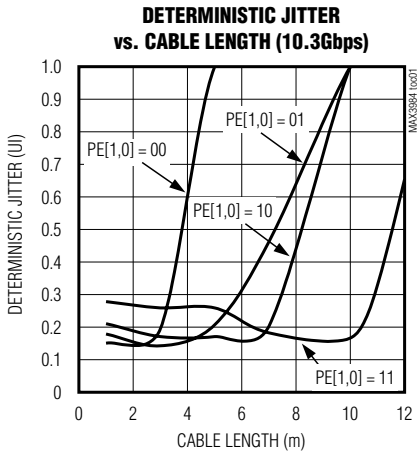
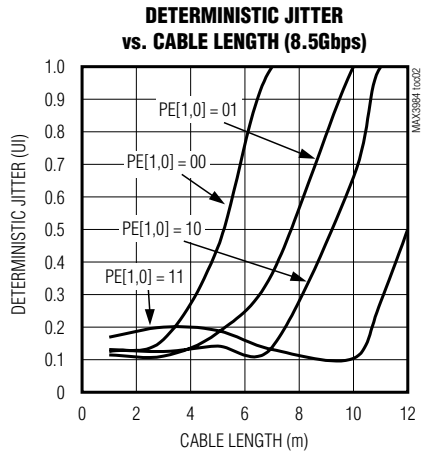


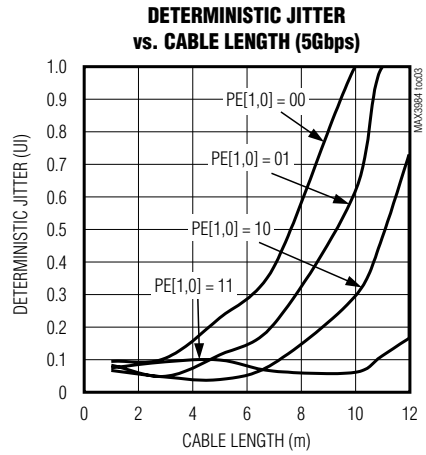
图3. 接收端测试装置(A、D为交流参数测试的参考)

典型工作特性

(V_{CC} = +3.3V, T_A = +25°C, PRBS7 + 100 CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101, OUT_LEV = high, 10in of FR-4 at the input, IN_LEV = high, 360mV_{P-P} at input of FR-4, unless otherwise noted.)



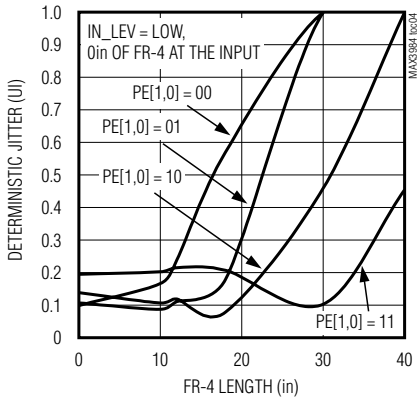




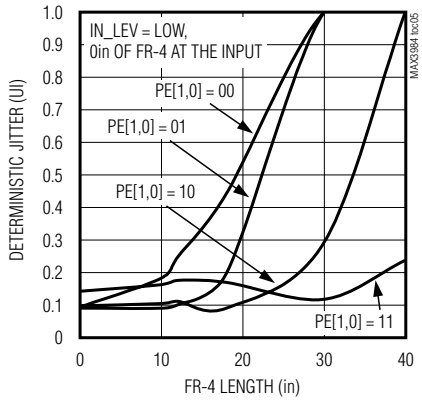
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, PRBS7 + 100 CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101, OUT_LEV = high, 10in of FR-4 at the input, IN_LEV = high, 360mV_{P-P} at input of FR-4, unless otherwise noted.)

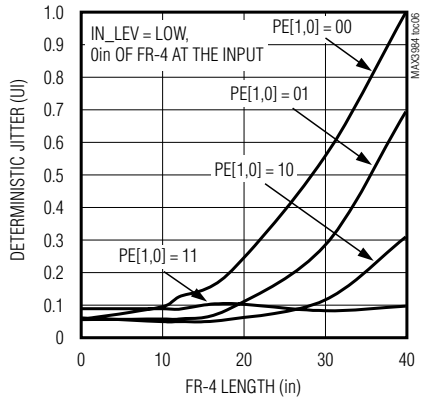
DETERMINISTIC JITTER vs. FR-4 LENGTH (10.3Gbps)



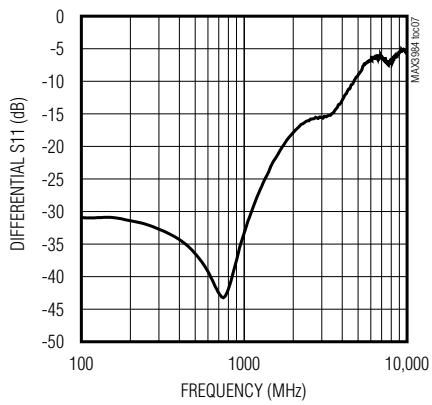
DETERMINISTIC JITTER vs. FR-4 LENGTH (8.5Gbps)



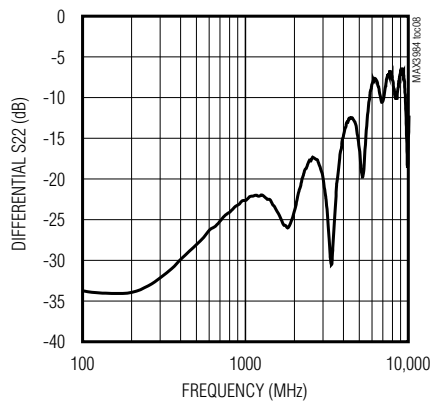
DETERMINISTIC JITTER vs. FR-4 LENGTH (5Gbps)



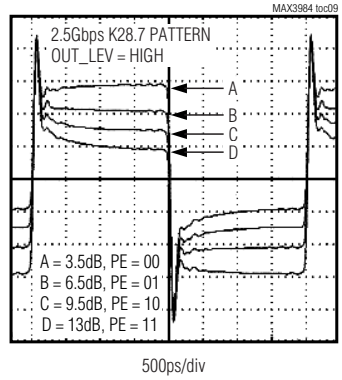
INPUT RETURN LOSS vs. FREQUENCY



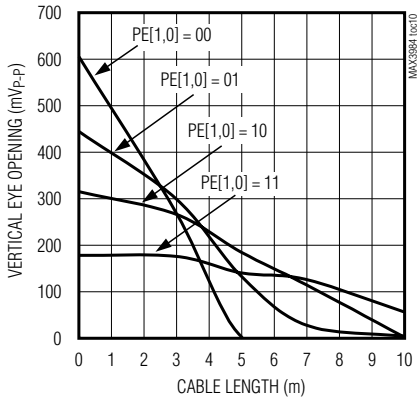
OUTPUT RETURN LOSS vs. FREQUENCY



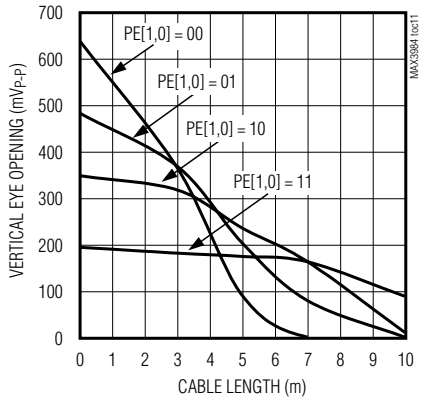
TRANSIENT RESPONSE



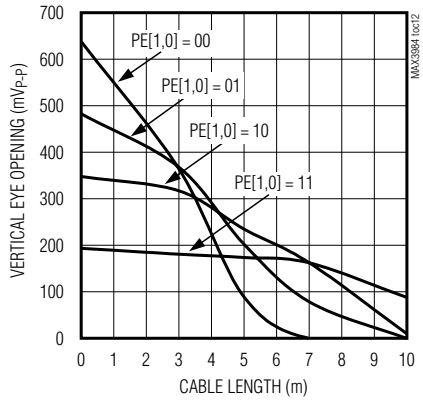
VERTICAL EYE OPENING vs. CABLE LENGTH (10.3Gbps)



VERTICAL EYE OPENING vs. CABLE LENGTH (8.5Gbps)



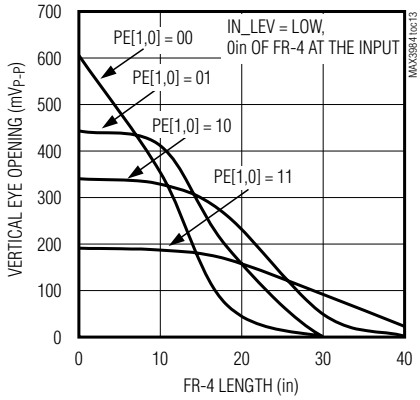
VERTICAL EYE OPENING vs. CABLE LENGTH (5Gbps)



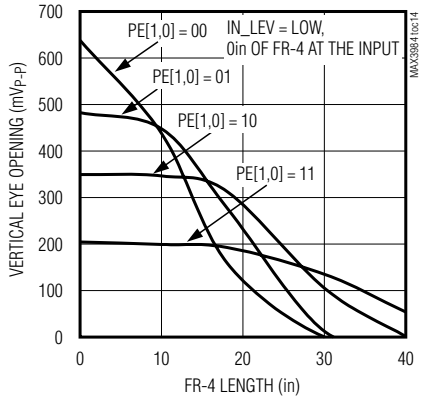
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, PRBS7 + 100 CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101, OUT_LEV = high, 10in of FR-4 at the input, IN_LEV = high, 360mV$_{P-P}$ at input of FR-4, unless otherwise noted.)

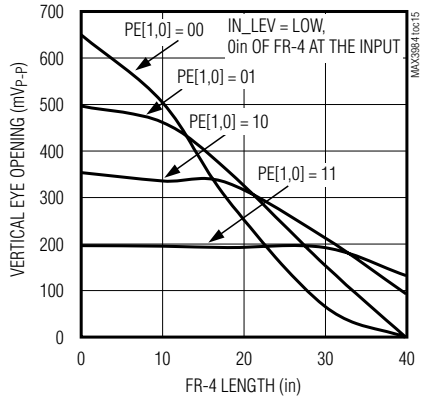
VERTICAL EYE OPENING vs. FR-4 LENGTH (10.3Gbps)



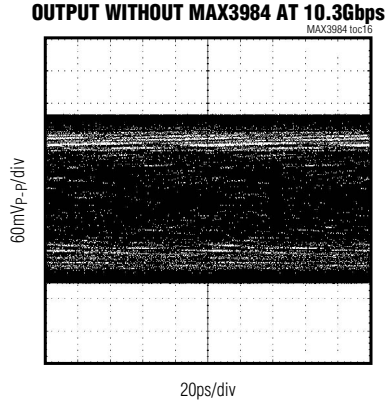
VERTICAL EYE OPENING vs. FR-4 LENGTH (8.5Gbps)



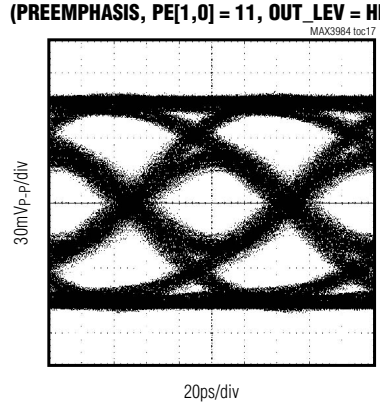
VERTICAL EYE OPENING vs. FR-4 LENGTH (5Gbps)



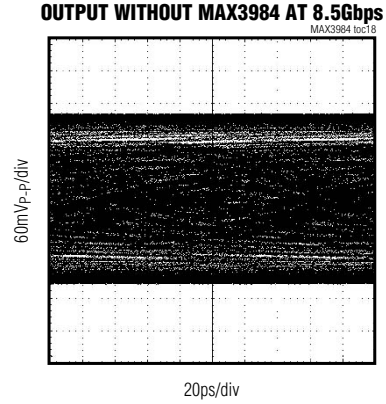
10m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3984 AT 10.3Gbps



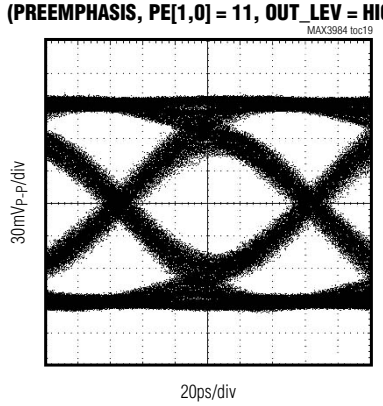
10m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3984 AT 10.3Gbps (PREEMPHASIS, PE[1,0] = 11, OUT_LEV = HIGH)



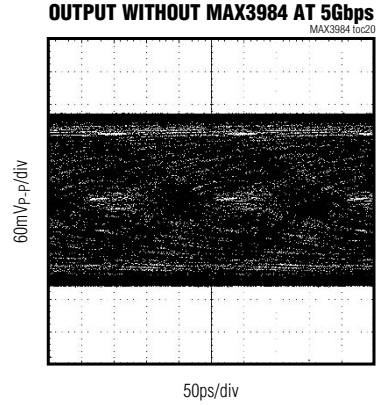
10m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3984 AT 8.5Gbps



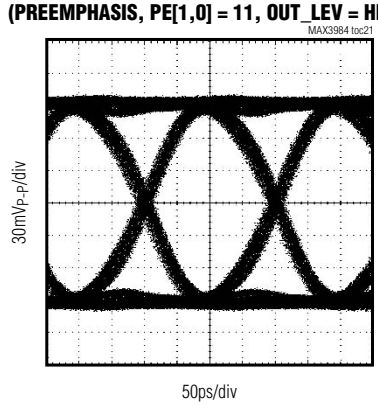
10m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3984 AT 8.5Gbps (PREEMPHASIS, PE[1,0] = 11, OUT_LEV = HIGH)



10m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3984 AT 5Gbps



10m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3984 AT 5Gbps (PREEMPHASIS, PE[1,0] = 11, OUT_LEV = HIGH)



1Gbps至10Gbps预加重驱动器，具有接收均衡器

引脚说明

引脚	名称	功能
1	V_{CC1}	电源输入端，接+3.3V。
2	IN+	数据输入正端，CML。该输入在内部以50Ω端接。
3	IN-	数据输入负端，CML。该输入在内部以50Ω端接。
4, 8, 9, 16	GND	电路地。
5	OUT_LEV	输出摆幅控制输入，具有20kΩ内部上拉的LVTTL逻辑。置为TTL高电平或浮空时，选择最大输出摆幅；置为TTL低电平时，减小输出摆幅。
6	PE1	输出预加重控制输入，具有10kΩ内部上拉的LVTTL逻辑。该引脚是2位预加重控制位的最高有效位，置为高电平或浮空时将该引脚置位。
7	PE0	输出预加重控制输入，具有10kΩ内部上拉的LVTTL逻辑。该引脚是2位预加重控制位的最低有效位，置为高电平或浮空时将该引脚置位。
10	OUT-	数据输出负端，CML。该输出以50Ω端接到V_{CC2}。
11	OUT+	数据输出正端，CML。该输出以50Ω端接到V_{CC2}。
12	V_{CC2}	输出级电源，接+3.3V。
13	TX_DISABLE	发送器禁止输入，具有10kΩ内部上拉的LVTTL逻辑。置高或浮空时，差分输出小于10mV_{P-P}；正常操作时置为低电平。
14	LOS	信号丢失检测，集电极开路TTL输出。需要一个≥ 4.7kΩ的外部上拉电阻(最高上拉电压为+5.5V)。当输入信号大于LOS解除电平时，该输出端为吸电流。如果需要禁止关闭功能，将LOS拉至地电位。
15	IN_LEV	接收均衡控制输入，具有40kΩ内部上拉的LVTTL逻辑。用于较高的LOS触发/解除检测电平、10英寸FR-4补偿时，将其置为TTL高电平或浮空；用于较低的LOS触发/解除检测电平、旁路FR-4均衡器时，则将其置为TTL低电平。
—	EP	裸焊盘，为获得最佳散热性能，该焊盘必须焊接到电路板的地层。

详细说明

MAX3984由一个接收器、一个驱动器和一个阈值可调的LOS检测器组成。接收器提供均衡功能，发送器提供可选择的预加重和可选择输出幅度控制功能，MAX3984还提供输出禁止控制功能。

接收器

数据通过一个CML输入级和可选择的均衡级馈入MAX3984，10Gbps速率下，接收器的固定均衡器可以补偿10英寸的FR-4 PCB损耗。可以把IN_LEV引脚置为逻辑低电平，旁路固定均衡器。

驱动器

驱动器含有四级预加重，可以补偿10米24 AWG、100Ω平衡电缆，或30英寸的FR-4。OUT_LEV引脚用于选择输出幅度，当OUT_LEV置低时，峰峰值为1000mV_{P-P}；当OUT_LEV置高时，峰峰值为1200mV_{P-P}。

信号丢失(LOS)

提供输入LOS检测，采用集电极开路输出，需要外部上拉电阻(≥ 4.7kΩ)。LOS通过上拉电阻连接到+3.0V至+5.5V电源。上电过程结束后，LOS输出才有效。

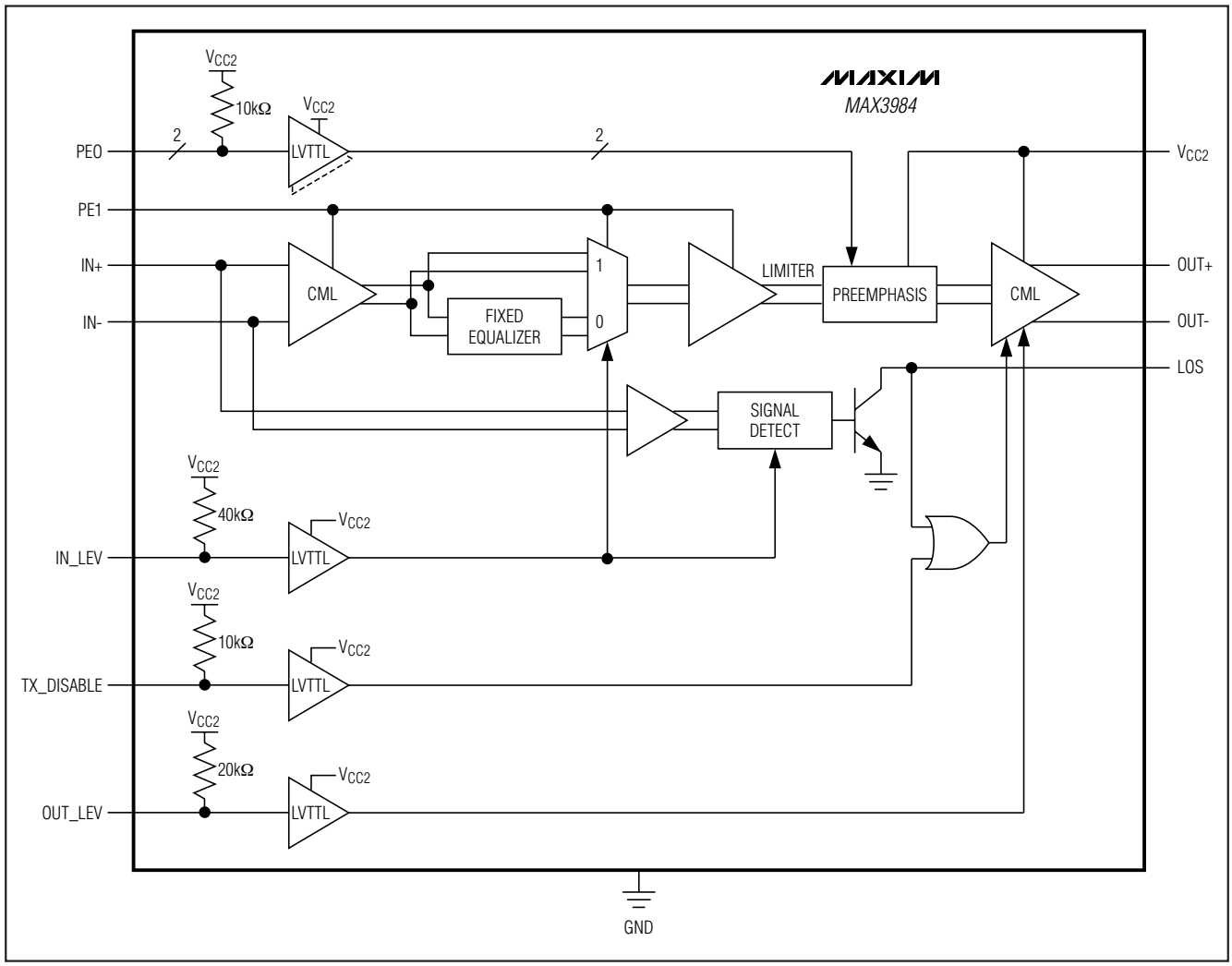


图4. 功能框图

IN_LEV引脚设置LOS触发/解除检测门限，当IN_LEV为LVTTL高电平或浮空时，LOS触发阈值为300mV$_{P-P}$；当IN_LEV为LVTTL低电平时，LOS触发阈值为100mV$_{P-P}$。

通过TX_DISABLE控制输出关断，MAX3984提供关闭功能，一旦检测到LOS条件时，关闭输出。如果需要禁止关闭控制功能，将LOS连接至地(请参考*关闭*部分)。

应用信息

关闭

MAX3984能够自动检测接收信号，使能或禁止数据输出。为使能关闭功能，LOS引脚必须通过一个上拉电阻(≥ 4.7kΩ)连接至TTL高电平或V_{CC}。TX_DISABLE和LOS在内部通过“或”逻辑门电路连接在一起，控制CML输出。如果触发LOS，则关闭输出。需要禁止关闭功能时，LOS必须拉至TTL低电平。当TX_DISABLE被置为高电平时，也可以关闭输出。

-40°C时的典型特性

MAX3984能够确保工作在0°C至+85°C，表1列出了器件在超出担保范围时的典型性能。

表1. -40°C时的典型特性

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
Different Output Swing (Note 1)		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high, PE1 = PE0 = high					1100		mV_{P-P}
		Measured differentially at point B in Figure 2; TX_DISABLE = low, OUT_LEV = low, PE1 = PE0 = high					920		
		TX_DISABLE = high, PE1 = PE0 = high					3.5		
Common-Mode Output (AC)		Measured at point B in Figure 2; TX_DISABLE = low, OUT_LEV = high (Note 2)					5		mV_{RMS}
Random Jitter		Measured at point D in Figure 3 (Note 3)					0.5		ps_{RMS}
Residual Output Deterministic Jitter at 1.0Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.02		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	0				
			5m, 24 AWG	0	1				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 5.0Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.12		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				
Residual Output Deterministic Jitter at 8.5Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.2		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	0				
			10m, 24 AWG	1	1				

表1. -40°C时的典型特性(续)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
Residual Output Deterministic Jitter at 10Gbps (Notes 4, 5)		Source to IN	OUT to load	PE1	PE0		0.25		UI_{P-P}
		6-mil, 10in of FR-4	3m, 24 AWG	0	1				
			5m, 24 AWG	1	0				
			7m, 24 AWG	1	1				
			10m, 24 AWG	1	1				

注1： 每侧负载为50Ω ±1%，0000011111模板或等效的2.5Gbps模板。

注2： PE1 = PE0 = 逻辑高电平(最大预加重)，每侧负载为50Ω ±1%，10Gbps速率下11001100模板(50%边沿密度)。按下式计算交流共模输出：

$$V_{ACCM\_RMS} = RMS[(V_P + V_N) / 2) - V_{DCCM}]$$

其中：

V_P = 在OUT+测得的时域电压，至少10GHz带宽。

V_N = 在OUT-测得的时域电压，至少10GHz带宽。

以RMS表示的交流共模电压(V_{ACCM_RMS})。

直流共模电压(V_{DCCM}) = (V_P + V_N) / 2的平均直流电压。

注3： 0000011111模板或等效的10Gbps模板，100mV_{P-P}差分摆幅。IN_LEV = 逻辑低电平，PE0 = PE1 = 最小预加重的逻辑低电平。4阶BT滤波器(7.5GHz带宽)或等效滤波器控制信号转换时间，请参考图3设置。

注4： 测试模板(464位)：100个0、1010、PRBS7、100个1、0101、PRBS7。

注5： 对于FR-4输入均衡，输入范围选择为IN_LEV = 逻辑高电平。电缆不平衡，Amphenol色谱带(160-2499-997) 24 AWG或等效电缆。残余确定性抖动是图2中A点源抖动和D点负载抖动之差。传输线输出的确定性抖动(DJ)与介质电感损耗有关，而非时钟源调制。在图2中的D点测量DJ。

1Gbps至10Gbps预加重驱动器，具有接收均衡器

布板考虑

电路板布局、设计会对MAX3984的性能产生显著影响，应尽量采用高水准高频布板技术，包括减小接地电感、对数据信号采用阻抗受控的传输线等。电源去耦电容应尽可能靠近V_{CC}引脚放置，所有V_{CC}引脚连接到一个电源层。须注意隔离输入、输出信号，以减小反馈串扰。

裸焊盘封装

带有裸焊盘的16引脚薄型QFN封装为IC提供了一个低热阻散热通道，MAX3984的裸焊盘必须焊接在电路板上，以获得良好的散热性能。有关裸焊盘封装的更多信息，请参考Maxim应用笔记*HFAN-08.1：Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

接口示意图

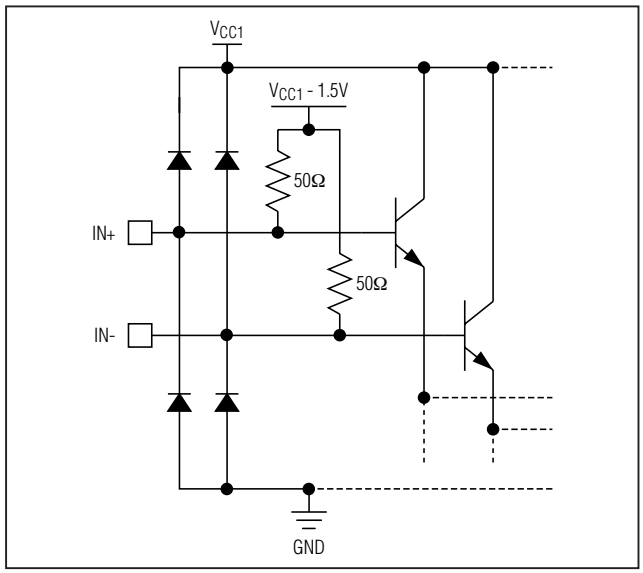


图5. IN+/IN-等效输入结构

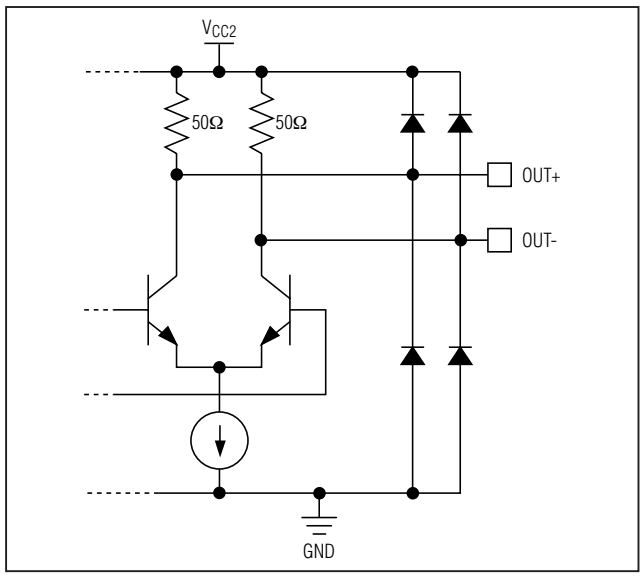
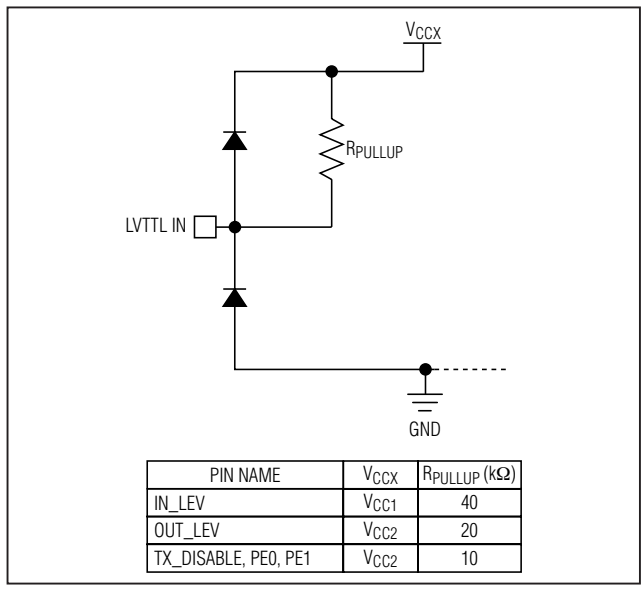


图6. OUT+/OUT-等效输出结构



PIN NAME	V_{CCX}	R_{PULLUP} (kΩ)
IN_LEV	V_{CC1}	40
OUT_LEV	V_{CC2}	20
TX_DISABLE, PE0, PE1	V_{CC2}	10

图7. LVTTL等效输入结构

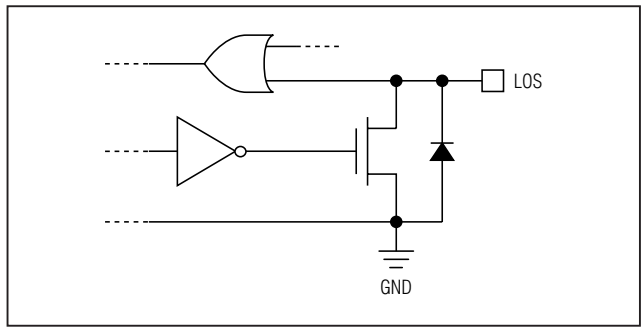
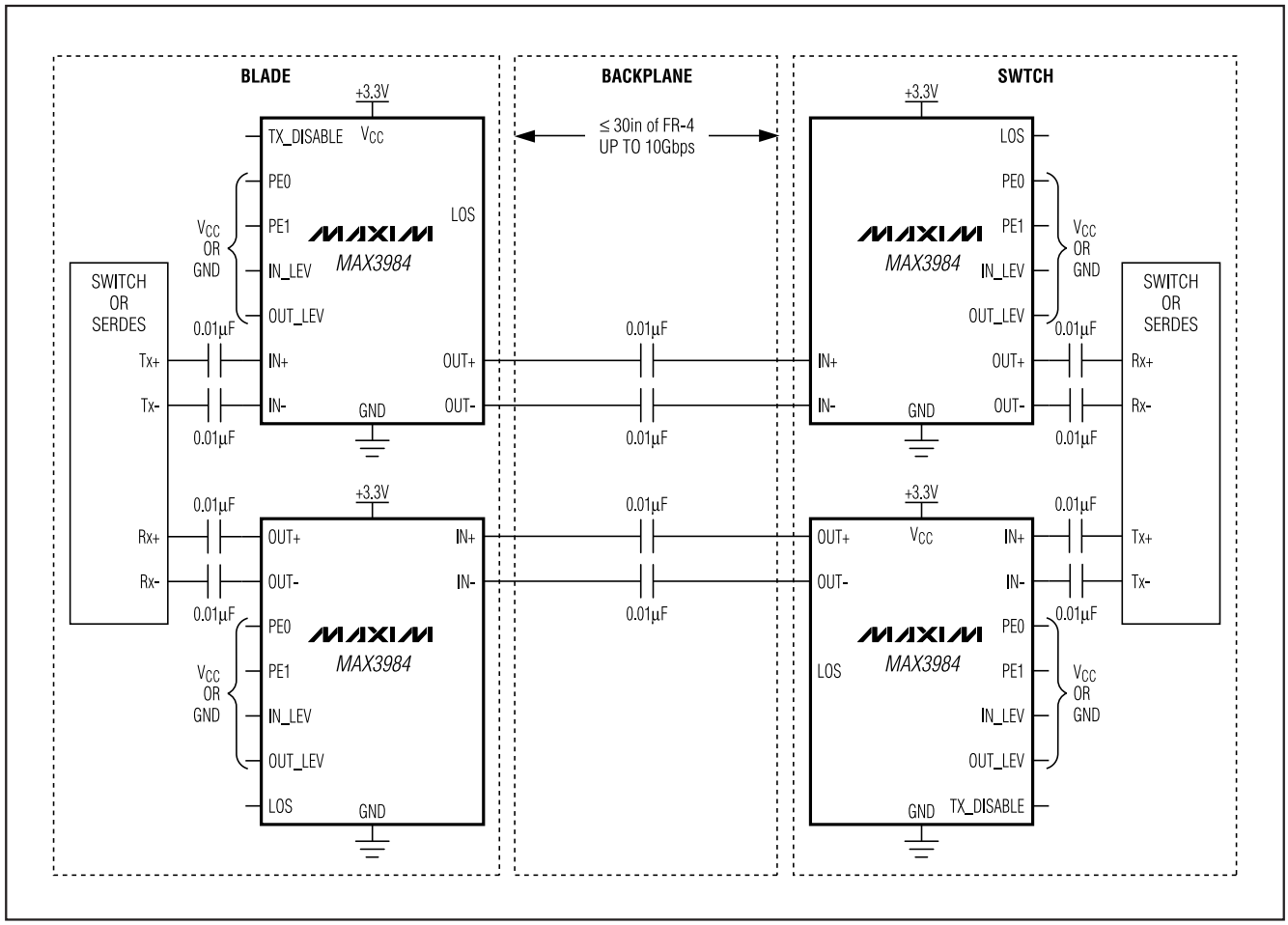
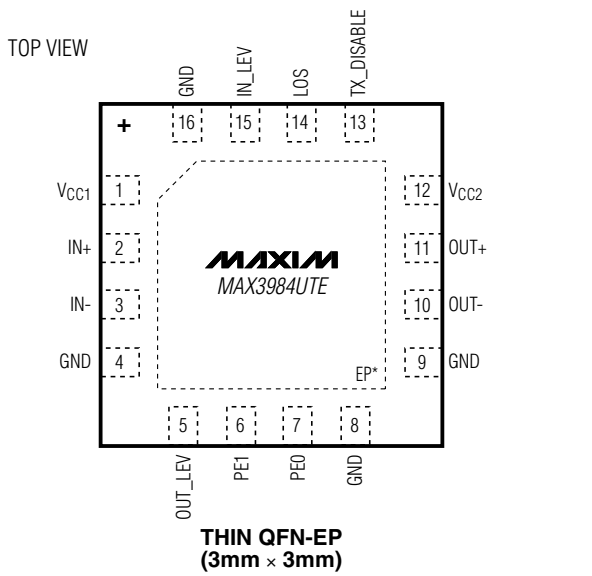


图8. 信号丢失检测等效输出结构

典型工作电路(续)


BLADE
BACKPLANE
SWTCH
≤ 30in of FR-4
UP TO 10Gbps
+3.3V
TX_DISABLE
VCC
PE0
PE1
IN_LEV
OUT_LEV
LOS
GND
IN+
IN-
OUT+
OUT-
MAX3984
VCC OR GND
SWITCH OR SERDES
Tx+
Tx-
Rx+
Rx-
0.01µF

引脚配置



THIN QFN-EP
(3mm × 3mm)

*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL OPERATION OF THE MAX3984.

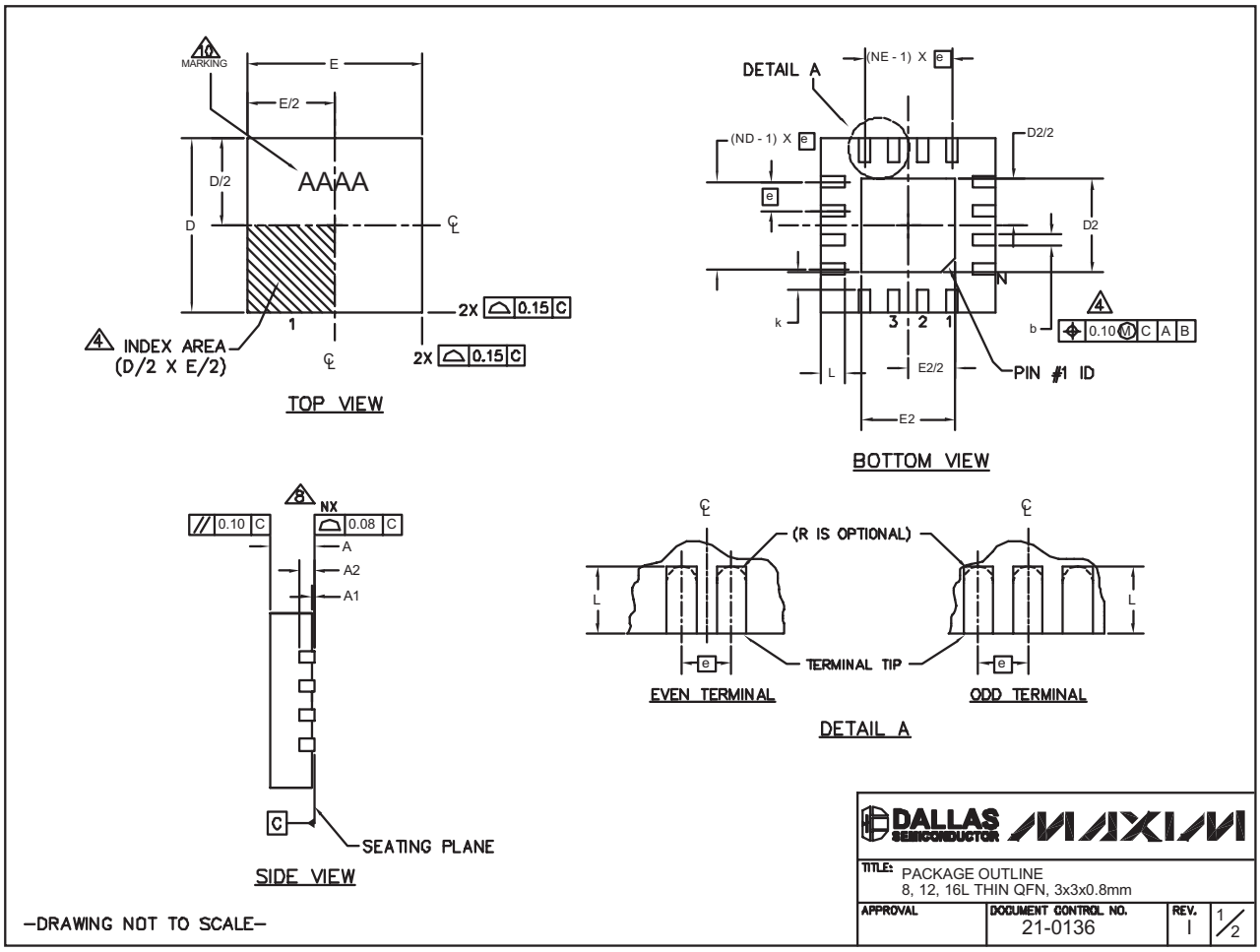
芯片信息

PROCESS: SiGe Bipolar

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

12x16L QFN THIN.EPS



封装信息(续)

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	I	2/2

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