19-4695; Rev 1; 6/10

可提供评估板

1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

MAX3799

概述

MAX3799为高度集成的限幅放大器和VCSEL驱动器，工作在高达14Gbps的数据速率，非常适合以太网和光纤通道应用。利用其可选择的数据通道噪声整形滤波器，MAX3799构建的10G光模块能够满足1000BASE-SR和10GBASE-SR的规格要求。器件采用+3.3V单电源供电，这款低功耗、集成限幅放大器和VCSEL驱动器IC为SFP MSA以及基于SFP+ MSA的光收发器建立了一个设计平台。高灵敏度限幅放大器将互阻放大器产生的差分输入信号限制在CML电平的差分输出。结构紧凑的VCSEL驱动器为VCSEL二极管提供调制电流和偏置电流。平均光功率由平均功率控制(APC)环路控制，该控制环路通过连接至VCSEL驱动器的3线数字接口控制。所有差分I/O为50Ω传输线PCB设计提供最佳的背向端接。

3线数字接口减少了引脚数量，并可实现高级Rx设置(速率选择、LOS门限、LOS禁止、LOS极性、CML输出电平、信号通道极性、去加重以及快速模式选择转换时间)和Tx设置(调制电流、偏置电流、极性以及视觉保护功能)，无需外部元件。MAX3799提供多个电流和电压DAC，允许使用低成本控制器IC。

MAX3799采用5mm x 5mm、32引脚TQFN无铅封装。

特性

- 实现单模块设计，符合1000BASE-SR和10GBASE-SR规格要求
- 1.25Gbps速率下具有-21.5dBm光灵敏度，采用10.32Gbps ROSA (-19.7dBm OMA)
- 3.3V供电时，功耗仅为320mW
- Rx/Tx通道支持14.025Gbps的典型电气特性(无重新定时，16x光纤通道方案)
- 10.32Gbps下，具有3mV$_{P-P}$接收灵敏度
- 8.5Gbps 8B/10B下接收器输出具有4ps$_{P-P}$ DJ
- 10.32Gbps 2^{31} - 1 PRBS下接收器输出具有4ps$_{P-P}$ DJ
- Rx/Tx输出具有26ps上升及下降时间
- 速率选择：1Gbps模式或10Gbps模式
- CML输出禁止
- Rx和Tx极性选择
- 可调节触发LOS报警电平
- LOS极性选择
- 能够向100Ω差分负载提供高达12mA的调制电流
- 偏置电流高达15mA
- 集成视觉保护功能
- 3线数字接口
- Tx输出具有可编程去加重

应用

1000BASE-SR/10GBASE-SR多速率SFP+光收发器

1x/2x/4x/8x/16x SFF/SFP/SFP+ MSA光纤通道(FC)光收发器

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX3799ETJ+	-40°C to +85°C	32 TQFN-EP*
MAX3799E/D	-40°C to +85°C	Dice**

+表示无铅(Pb)/符合RoHS标准的封装。

**EP = 裸焊盘。*

***在T_A = +25°C条件下进行了测试。*

典型应用电路和引脚配置在数据资料的最后给出。

ABSOLUTE MAXIMUM RATINGS

V_{CCR}, V_{CCT}, V_{CCD}.....-0.3V to +4.0V
Voltage Range at DISABLE, SDA, SCL, CSEL, RSEL, FAULT, BMON, LOS, CAZ2.....-0.3V to (V_{CC} + 0.3V)
Voltage Range at ROUT+, ROUT- .....(V_{CC} - 1V) to (V_{CC} + 0.3V)
Voltage at TIN+, TIN-.....(V_{CC} - 2.5V) to (V_{CC} - 0.5V)
Voltage Range at TOUT+, TOUT- .....(V_{CC} - 2V) to (V_{CC} + 0.3V)
Voltage at BIAS .....0V to V_{CC}
Voltage at RIN+, RIN-.....(V_{CC} - 2V) to (V_{CC} - 0.2V)
Current Range into FAULT, LOS.....-1mA to +5mA
Current Range into SDA.....-1mA to +1mA
Current into ROUT+, ROUT- 40mA
Current into TOUT+, TOUT-.....60mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5W/°C above +70°C) 2759mW
Operating Junction Temperature Range.....-55°C to +150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.85V to 3.63V, T_A = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, C_{AZ} = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, V_{CC} = 3.3V, I_{BIAS} = 6mA, I_{MOD} = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current	I_{CC}	Includes the CML output current; excludes I_{BIAS} = 6mA, I_{MOD} = 6mA, V_{DIFF_ROUT} = 400mV_{P-P} (Note 1)		97	150	mA
Power-Supply Voltage	V_{CC}		2.85		3.63	V
GENERAL						
Input Data Rate			1.0625		10.32	Gbps
Input/Output SNR			14.1			
BER					10E-12	
POWER-ON RESET						
High POR Threshold				2.55	2.75	V
Low POR Threshold		I_{BIAS} = $I_{BIASOFF}$ and I_{MOD} = I_{MODOFF}	2.3	2.45		V
Rx INPUT SPECIFICATIONS						
Differential Input Resistance RIN+/RIN-	R_{IN_DIFF}		75	100	125	Ω
Input Sensitivity (Note 2)	V_{INMIN}	RATE_SEL = 0 (1.25Gbps)		1	3	mV_{P-P}
		RATE_SEL = 1 (10.32Gbps)		3	8	
Input Overload	V_{INMAX}		1.2			V_{P-P}
Input Return Loss	SDD11	DUT is powered on, f ≤ 5GHz		14		dB
		DUT is powered on, f ≤ 16GHz		7		
Input Return Loss	SCC11	DUT is powered on, 1GHz < f ≤ 5GHz		8		dB
		DUT is powered on, 1GHz < f ≤ 16GHz		8		
Rx OUTPUT SPECIFICATIONS						
Differential Output Resistance	$R_{OUTDIFF}$		75	100	125	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, T_A = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, C_{AZ} = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, V_{CC} = 3.3V, I_{BIAS} = 6mA, I_{MOD} = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Return Loss	SDD22	DUT is powered on, f ≤ 5GHz		11		dB
		DUT is powered on, f ≤ 16GHz		5		
Output Return Loss	SCC22	DUT is powered on, 1GHz < f ≤ 5GHz		9		dB
		DUT is powered on, 1GHz < f ≤ 16GHz		7		
CML Differential Output Voltage High		$5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[162]	595	800	1005	mV_{P-P}
CML Differential Output Voltage Medium		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, SET_CML[80]	300	400	515	mV_{P-P}
CML Differential Output DAC Limit		SET_CML[7:0]			215	
Differential Output Signal When Disabled		Outputs AC-coupled, V_{INMAX} applied to input V_{DIFF_ROUT} = $800mV_{P-P}$ at 8.5Gbps (Notes 2, 3)		6	15	mV_{P-P}
Data Output Transition Time (20% to 80%) (Notes 2, 3, 4)	t_R/t_F	$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 1, V_{DIFF_ROUT} = $400mV_{P-P}$		26	35	ps
		$5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 0, V_{DIFF_ROUT} = $800mV_{P-P}$		60	100	
Rx TRANSFER CHARACTERISTICS						
Deterministic Jitter (Notes 2, 3, 5)	DJ	$60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 10.32Gbps, RATE_SEL = 1, V_{DIFF_ROUT} = $400mV_{P-P}$		4	12	ps_{P-P}
		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 8.5Gbps, RATE _SEL = 1, V_{DIFF_ROUT} = $400mV_{P-P}$		4	12	
		$5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 1.25Gbps, RATE _SEL = 0, V_{DIFF_ROUT} = $800mV_{P-P}$		20		
Random Jitter (Notes 2, 3)	RJ	Input = $60mV_{P-P}$ at 1.25Gbps, RATE_SEL = 0, V_{DIFF_ROUT} = $800mV_{P-P}$		1.8	2.5	ps_{RMS}
		Input = $60mV_{P-P}$ at 8.5Gbps, RATE _SEL = 1, V_{DIFF_ROUT} = $400mV_{P-P}$		0.32	0.48	
Low-Frequency Cutoff		C_{AZ} = 0.1µF		2		kHz
		C_{AZ} = open		500		
Rx LOS SPECIFICATIONS						
LOS Assert Sensitivity Range			14		77	mV_{P-P}
LOS Hysteresis		10 x log($V_{DEASSERT}/V_{ASSERT}$) (Note 6)	1.25	2.1		dB
LOS Assert/Deassert Time		(Note 7)	2.3		80	µs
Low Assert Level		SET_LOS[7] (Notes 2, 6)	8	11	14	mV_{P-P}
Low Deassert Level		SET_LOS[7] (Notes 2, 6)	14	18	21	mV_{P-P}
Medium Assert Level		SET_LOS[32] (Notes 2, 6)	39	48	58	mV_{P-P}
Medium Deassert Level		SET_LOS[32] (Notes 2, 6)	65	81	95	mV_{P-P}
High Assert Level		SET_LOS[63] (Notes 2, 6)	77	94	112	mV_{P-P}
High Deassert Level		SET_LOS[63] (Notes 2, 6)	127	158	182	mV_{P-P}

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, T_A = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, C_{AZ} = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, V_{CC} = 3.3V, I_{BIAS} = 6mA, I_{MOD} = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tx INPUT SPECIFICATIONS						
Differential Input Voltage	V_{IN}	Data rate = 1.0625Gbps	0.2		2.4	V_{P-P}
		Data rate = 10.32Gbps	0.075		0.8	
Common-Mode Input Voltage	V_{INCM}			2.75		V
Differential Input Resistance	R_{IN}		75	100	125	Ω
Input Return Loss	SDD11	DUT is powered on, f ≤ 5GHz		15		dB
		DUT is powered on, f ≤ 16GHz		6		
Input Return Loss	SCC11	DUT is powered on, 1GHz < f ≤ 5GHz		9		dB
		DUT is powered on, 1GHz < f ≤ 16GHz		5		
Tx LASER MODULATOR						
Maximum Modulation-On Current into 100Ω Differential Load	I_{MODMAX}	Outputs AC-coupled, V_{CCTO} ≥ 2.95V	12			mA
Minimum Modulation-On Current into 100Ω Differential Load	I_{MODMIN}	Outputs AC-coupled			2	mA
Modulation Current DAC Stability		2mA ≤ I_{MOD} ≤ 12mA (Note 8)			4	%
Modulation Current Rise Time/ Fall Time	t_R/t_F	5mA ≤ I_{MOD} ≤ 10mA, 20% to 80%, SET_TXDE[3:0] = 10 (Notes 2, 4)		26	39	ps
Deterministic Jitter (Notes 2, 9)	DJ	5mA ≤ I_{MOD} ≤ 12mA, at 10.32Gbps, 250mV_{P-P} ≤ V_{IN} ≤ 800mV_{P-P}, SET_TXDE[3:0] = 0		6	12	ps
		5mA ≤ I_{MOD} ≤ 12mA, at 10.32Gbps, 250mV_{P-P} ≤ V_{IN} ≤ 800mV_{P-P}, SET_TXDE[3:0] = 10		6	13	
		5mA ≤ I_{MOD} ≤ 12mA, at 8.5Gbps, 250mV_{P-P} ≤ V_{IN} ≤ 800mV_{P-P}, SET_TXDE[3:0] = 0		6	12	
		5mA ≤ I_{MOD} ≤ 12mA, at 8.5Gbps, 250mV_{P-P} ≤ V_{IN} ≤ 800mV_{P-P}, SET_TXDE[3:0] = 10		6	12	
		2mA ≤ I_{MOD} ≤ 12mA, at 4.25Gbps		5		
		2mA ≤ I_{MOD} ≤ 12mA, at 1.0625Gbps		5		
Random Jitter		5mA ≤ I_{MOD} ≤ 12mA, 250mV_{P-P} ≤ V_{IN} ≤ 800mV_{P-P}		0.17	0.5	ps_{RMS}
Output Return Loss	SDD22	DUT is powered on, f ≤ 5GHz		12		dB
		DUT is powered on, f ≤ 16GHz		5		
Tx BIAS GENERATOR						
Maximum Bias-On Current	$I_{BIASMAX}$	Current into BIAS pin	15			mA
Minimum Bias-On Current	$I_{BIASMIN}$	Current into BIAS pin			2	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, T_A = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, C_{AZ} = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, V_{CC} = 3.3V, I_{BIAS} = 6mA, I_{MOD} = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS Current DAC Stability		2mA ≤ I_{BIAS} ≤ 15mA (Notes 2, 10)			4	%
Compliance Voltage at BIAS	V_{BIAS}		0.9		2.1	V
BIAS Current Monitor Current Gain	I_{BMON}	External resistor to GND defines the voltage gain		16		mA/A
Compliance Voltage at BMON	V_{BMON}		0		1.8	V
BIAS Current Monitor Current Gain Stability	I_{BMON}	2mA ≤ I_{BIAS} ≤ 15mA (Note 10)			5	%
Tx SAFETY FEATURES						
Excessive Voltage at BMON	V_{BMON}	Average voltage, FAULT warning always occurs for V_{BMON} ≥ V_{CC} - 0.55V, FAULT warning never occurs for V_{BMON} ≤ V_{CC} - 0.65V	V_{CC} - 0.65V	V_{CC} - 0.6V	V_{CC} - 0.55V	V
Excessive Voltage at BIAS	V_{BIAS}	Average voltage, FAULT always occurs for V_{BIAS} ≤ 0.44V, FAULT never occurs for V_{BIAS} ≥ 0.65V	0.44	0.48	0.65	V
Maximum VCSEL Current in Off State	I_{OFF}	FAULT or DISABLE, V_{BIAS} = V_{CC}			25	µA
SFP TIMING REQUIREMENTS						
DISABLE Assert Time	$t_{\_OFF}$	Time from rising edge of DISABLE input signal to I_{BIAS} = $I_{BIASOFF}$ and I_{MOD} = I_{MODOFF}			1	µs
DISABLE Negate Time	$t_{\_ON}$	Time from falling edge of DISABLE to I_{BIAS} and I_{MOD} at 90% of steady state when FAULT = 0 before reset			500	µs
FAULT Reset Time of Power-On Time	$t_{\_INIT}$	Time from power-on or negation of FAULT using DISABLE			100	ms
FAULT Reset Time	$t_{\_FAULT}$	Time from fault to FAULT on, C_{FAULT} ≤ 20pF, R_{FAULT} = 4.7kΩ			10	µs
DISABLE to Reset		Time DISABLE must be held high to reset FAULT	5			µs
OUTPUT_LEVEL VOLTAGE DAC (SET_CML)						
Full-Scale Voltage	V_{FS}	100Ω differential resistive load		1200		mV_{P-P}
Resolution				5		mV_{P-P}
Integral Nonlinearity	INL	5mA ≤ I_{CML_LEVEL} ≤ 20mA		±0.9		LSB
LOS THRESHOLD VOLTAGE DAC (SET_LOS)						
Full-Scale Voltage	V_{FS}			94		mV_{P-P}
Resolution				1.5		mV_{P-P}
Integral Nonlinearity	INL	11mV_{P-P} ≤ V_{TH_LOS} ≤ 94mV_{P-P}		±0.7		LSB
BIAS CURRENT DAC (SET_IBIAS)						
Full-Scale Current	I_{FS}			21		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, T_A = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, C_{AZ} = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, V_{CC} = 3.3V, I_{BIAS} = 6mA, I_{MOD} = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution				40		µA
Integral Nonlinearity	INL	1mA ≤ I_{BIAS} ≤ 15mA		±1		LSB
Differential Nonlinearity	DNL	1mA ≤ I_{BIAS} ≤ 15mA, guaranteed monotonic at 8-bit resolution (SET_IBIAS[8:1])		±1		LSB
MODULATION CURRENT DAC (SET_IMOD)						
Full-Scale Current	I_{FS}			21		mA
Resolution				40		µA
Integral Nonlinearity	INL	2mA ≤ I_{MOD} ≤ 12mA		±1		LSB
Differential Nonlinearity	DNL	2mA ≤ I_{MOD} ≤ 12mA, guaranteed monotonic at 8-bit resolution (SET_IMOD[8:1])		±1		LSB
CONTROL I/O SPECIFICATIONS						
RSEL Input Current	I_{IH}, I_{IL}				150	µA
RSEL Input High Voltage	V_{IH}		1.8		V_{CC}	V
RSEL Input Low Voltage	V_{IL}		0		0.8	V
RSEL Input Impedance	R_{PULL}	Internal pulldown resistor	40	75	110	kΩ
DISABLE Input Current	I_{IH}				12	µA
	I_{IL}	Dependency on pullup resistance		420	800	
DISABLE Input High Voltage	V_{IH}		1.8		V_{CC}	V
DISABLE Input Low Voltage	V_{IL}		0		0.8	V
DISABLE Input Impedance	R_{PULL}	Internal pullup resistor	4.7	8	10	kΩ
LOS, FAULT Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ - 10kΩ to V_{CC}, R_{FAULT} = 4.7kΩ - 10kΩ to V_{CC}	V_{CC} - 0.5		V_{CC}	V
LOS, FAULT Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ - 10kΩ to V_{CC}, R_{FAULT} = 4.7kΩ - 10kΩ to V_{CC}	0		0.4	V
3-WIRE DIGITAL I/O SPECIFICATIONS (SDA, CSEL, SCL)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			0.082		V
Input Leakage Current	I_{IL}, I_{IH}	V_{IN} = 0V or V_{CC}; internal pullup or pulldown (75kΩ typ)			150	µA
Output High Voltage	V_{OH}	External pullup of 4.7kΩ to V_{CC}	V_{CC} - 0.5			V
Output Low Voltage	V_{OL}	External pullup of 4.7kΩ to V_{CC}			0.4	V
3-WIRE DIGITAL INTERFACE TIMING CHARACTERISTICS (See Figure 4)						
SCL Clock Frequency	f_{SCL}			400	1000	kHz
SCL Pulse-Width High	t_{CH}		0.5			µs
SCL Pulse-Width Low	t_{CL}		0.5			µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, T_A = -40°C to +85°C, CML receiver output load is AC-coupled to differential 100Ω, C_{AZ} = 1nF, transmitter output load is AC-coupled to differential 100Ω (see Figure 1), typical values are at +25°C, V_{CC} = 3.3V, I_{BIAS} = 6mA, I_{MOD} = 6mA, unless otherwise specified. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL External Load	C_B	Total bus capacitance on one line with 4.7kΩ pullup to V_{CC}			20	pF

Note 1: Supply current is measured with unterminated receiver CML output or with AC-coupled Rx output termination. The Tx output and the bias current output must be connected to a separate supply to remove the modulation/bias current portion from the supply current. BIAS must be connected to 2.0V. TOUT+/- must be connected through 50Ω load resistors to a separate supply voltage.

Note 2: Guaranteed by design and characterization, T_A = -40°C to +95°C.

Note 3: The data input transition time is controlled by a 4th-order Bessel filter with -3dB frequency = 0.75 x data rate. The deterministic jitter caused by this filter is not included in the DJ generation specifications.

Note 4: Test pattern is 00001111 at 1.25Gbps for RATE_SEL = 0. Test pattern is 00001111 at 8.5Gbps for RATE_SEL = 1.

Note 5: Receiver deterministic jitter is measured with a repeating 2^{31} - 1 PRBS equivalent pattern at 10.32Gbps. For 1.25Gbps to 8.5Gbps, a repeating K28.5 pattern [00111110101100000101] is used. Deterministic jitter is defined as the arithmetic sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ).

Note 6: Measured with a k28.5 pattern from 1.0625Gbps to 8.5Gbps. Measured with 2^{31} - 1 PRBS at 10.32Gbps.

Note 7: Measurement includes an input AC-coupling capacitor of 100nF and C_{CAZ} of 100nF. The signal at the input is switched between two amplitudes: Signal_ON and Signal_OFF.

1) Receiver operates at sensitivity level plus 1dB power penalty.
   a) Signal_OFF = 0
      Signal_ON = (+8dB) + 10log(min_assert_level)
   b) Signal_ON = (+1dB) + 10log(max_deassert_level)
      Signal_OFF = 0
2) Receiver operates at overload.
   Signal_OFF = 0
   Signal_ON = $1.2V_{P-P}$

max_deassert_level and the min_assert_level are measured for one LOS_THRESHOLD setting.

Note 8: Gain stability is defined as [(I_measured) - (I_reference)]/(I_reference) over the listed current range, temperature, and V_{CC} from +2.95V to +3.63V. Reference current measured at V_{CC} = +3.2V, T_A = +25°C.

Note 9: Transmitter deterministic jitter is measured with a repeating 2^7 - 1 PRBS, 72 0s, 2^7 - 1 PRBS, and 72 1s pattern at 10.32Gbps. For 1.0625Gbps to 8.5Gbps, a repeating K28.5 pattern [00111110101100000101] is used. Deterministic jitter is defined as the arithmetic sum of PWD and PDJ.

Note 10: Gain stability is defined as [(I_measured) - (I_reference)]/(I_reference) over the listed current range, temperature, and V_{CC} from +2.85V to +3.63V. Reference current measured at V_{CC} = +3.3V, T_A = +25°C.

1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

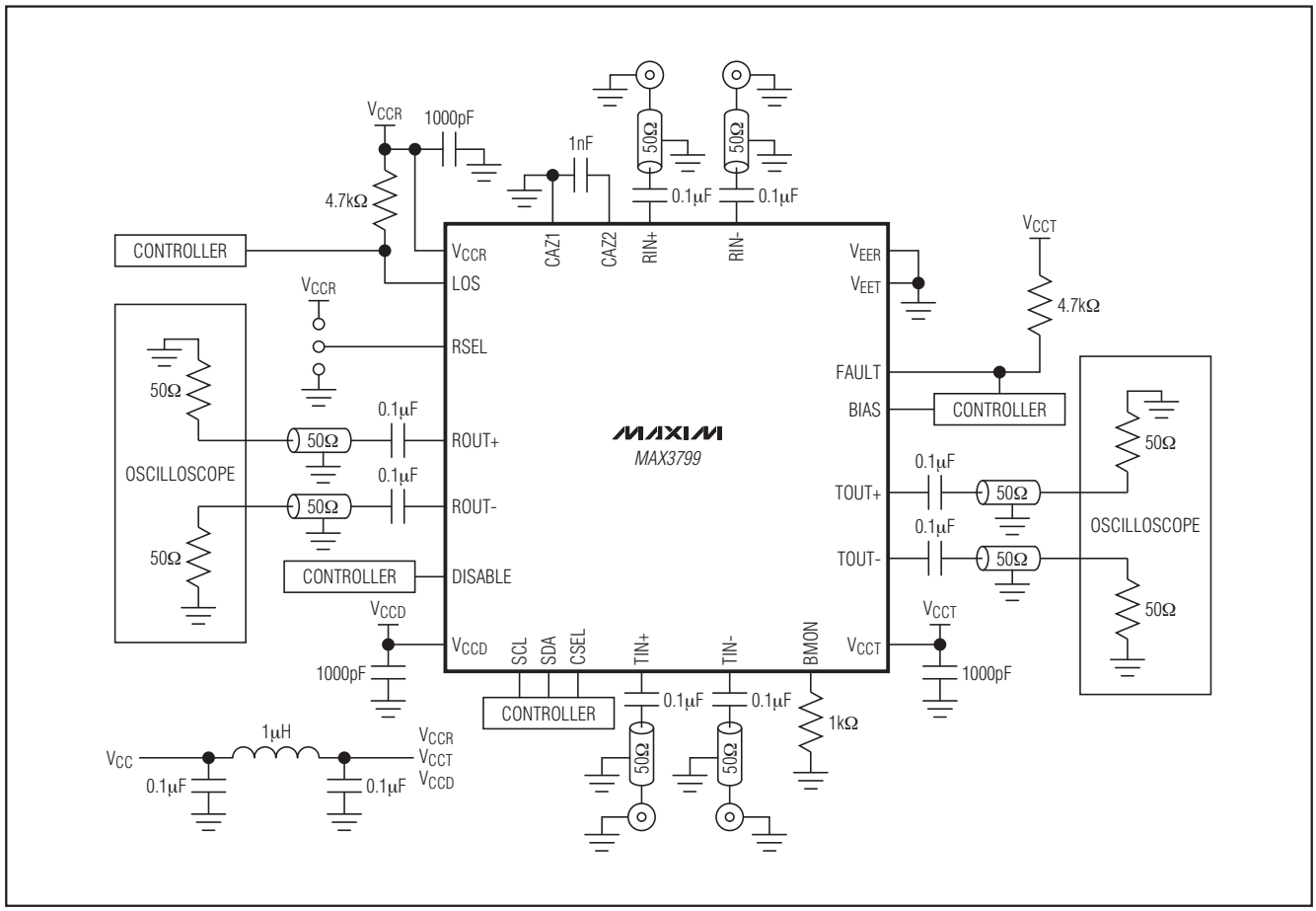
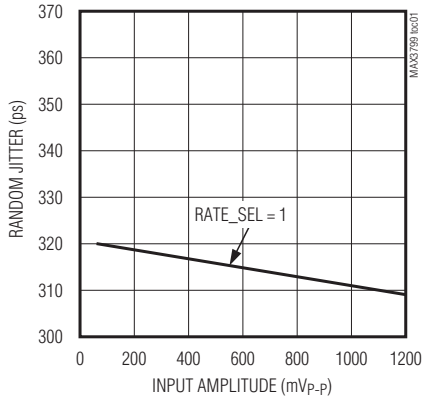


图1. VCSEL驱动器特性测试电路

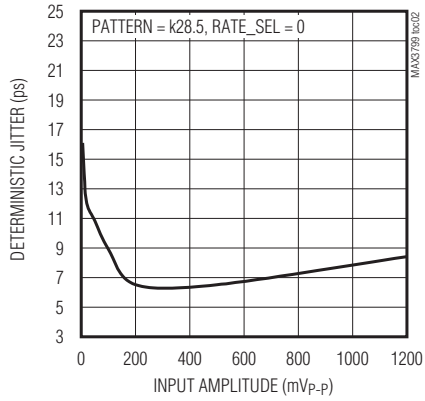
典型工作特性—限幅放大器

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

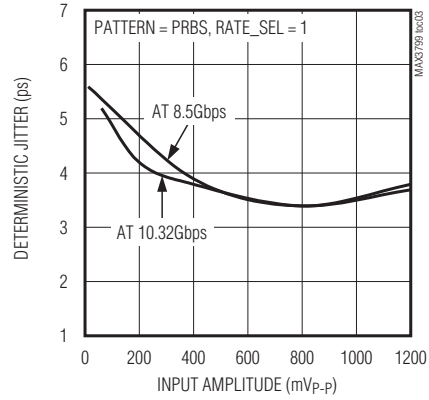
RANDOM JITTER vs. INPUT AMPLITUDE



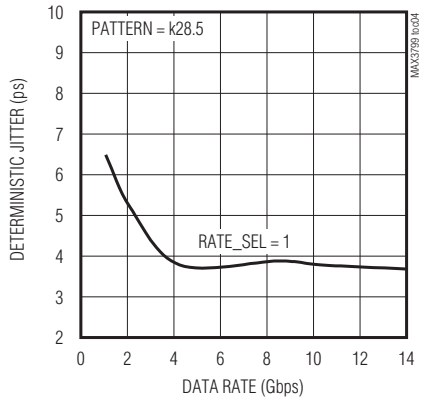
DETERMINISTIC JITTER vs. INPUT AMPLITUDE AT 1.25Gbps



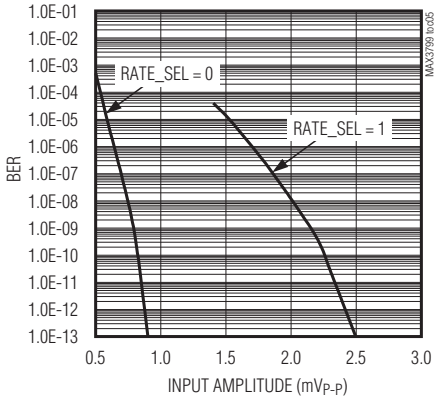
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



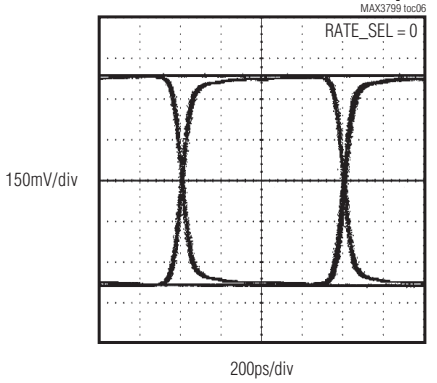
DETERMINISTIC JITTER vs. DATA RATE



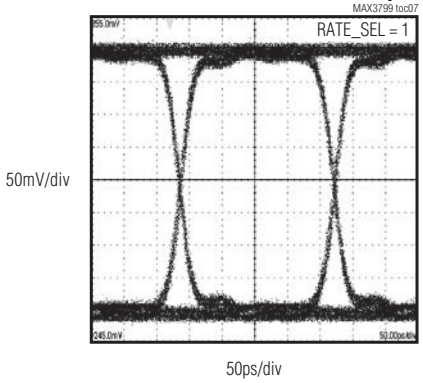
BER vs. INPUT AMPLITUDE



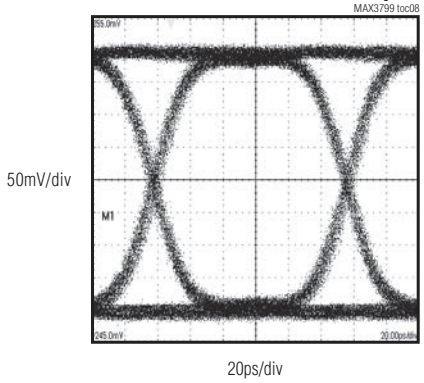
OUTPUT EYE DIAGRAM AT 1.25Gbps



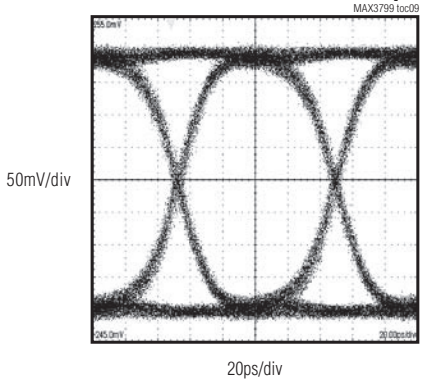
OUTPUT EYE DIAGRAM AT 4.25Gbps



OUTPUT EYE DIAGRAM AT 8.5Gbps



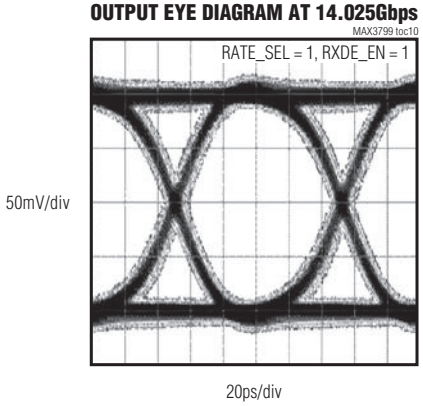
OUTPUT EYE DIAGRAM AT 10.32Gbps



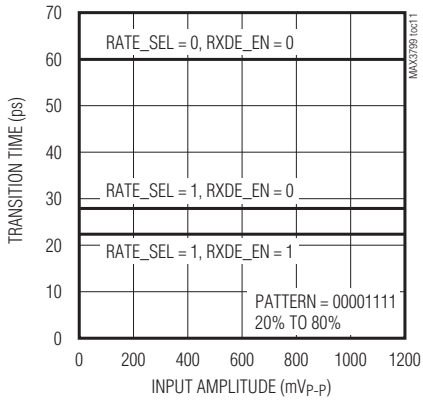
典型工作特性—限幅放大器(续)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

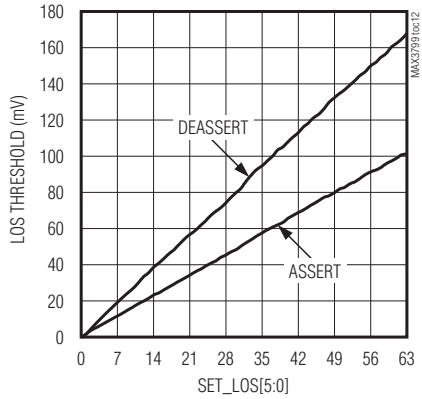
OUTPUT EYE DIAGRAM AT 14.025Gbps



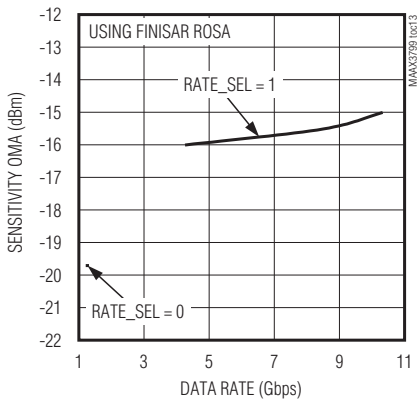
TRANSITION TIME vs. INPUT AMPLITUDE



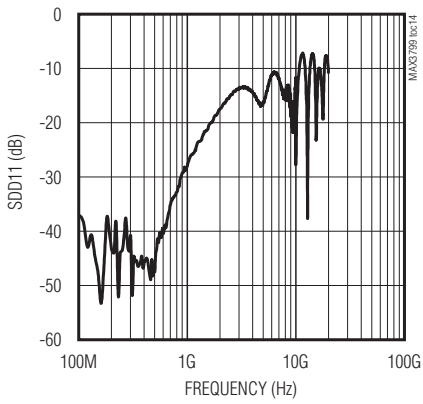
LOS THRESHOLD vs. DAC SETTING



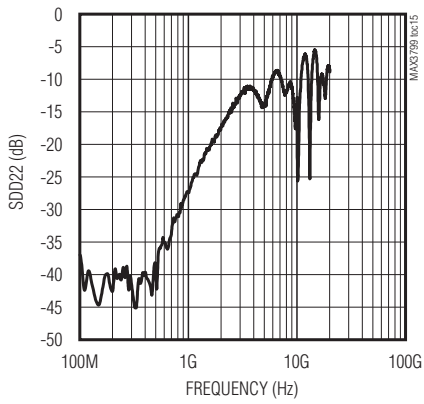
SENSITIVITY vs. DATA RATE



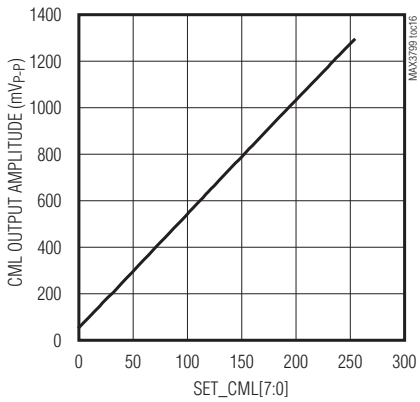
Rx INPUT RETURN LOSS



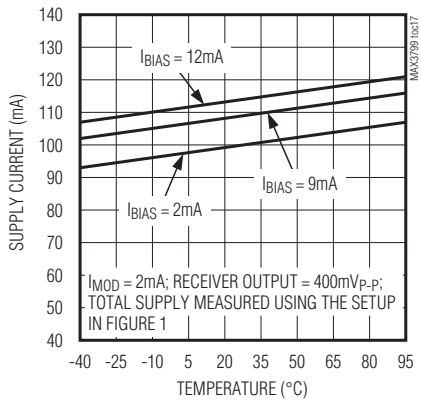
Rx OUTPUT RETURN LOSS



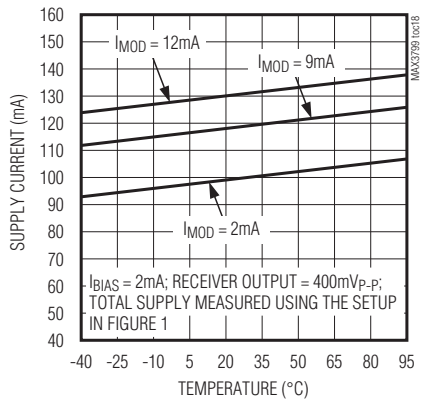
CML OUTPUT AMPLITUDE vs. DAC SETTING



TOTAL SUPPLY CURRENT vs. TEMPERATURE



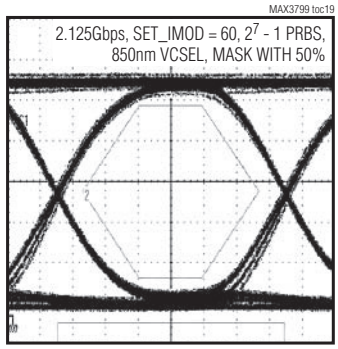
TOTAL SUPPLY CURRENT vs. TEMPERATURE



典型工作特性—VCSEL驱动器(续)

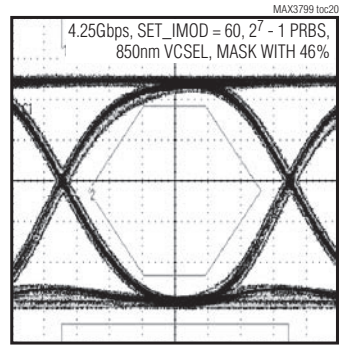
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

OPTICAL EYE DIAGRAM



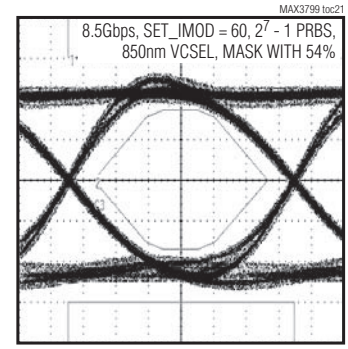
68ps/div

OPTICAL EYE DIAGRAM



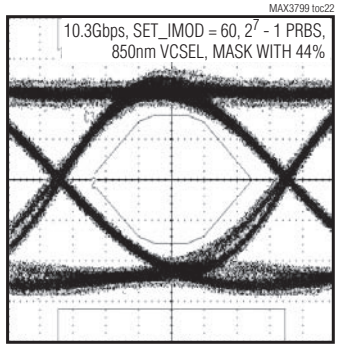
34ps/div

OPTICAL EYE DIAGRAM



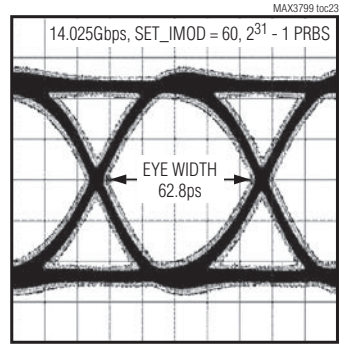
17ps/div

OPTICAL EYE DIAGRAM



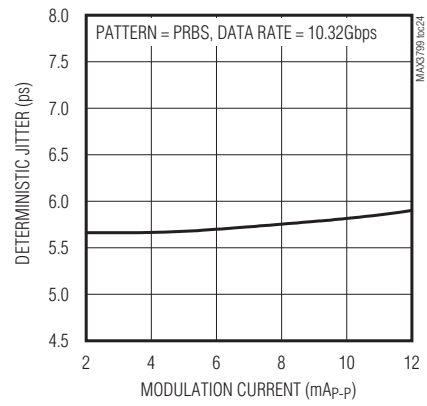
14ps/div

ELECTRICAL EYE DIAGRAM

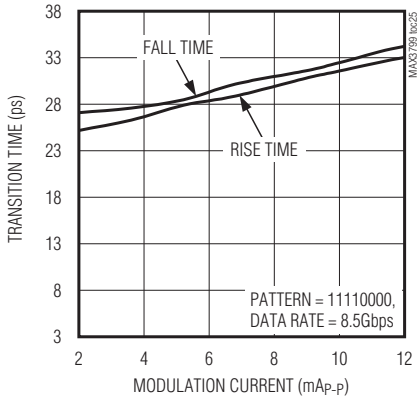


14ps/div

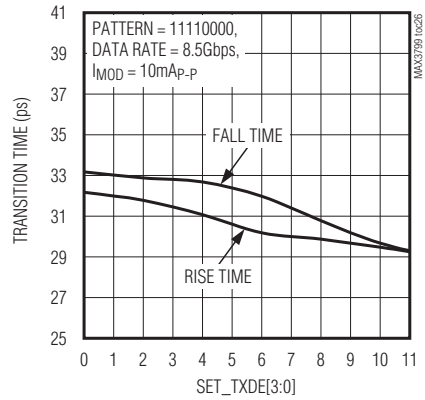
DETERMINISTIC JITTER vs. MODULATION CURRENT



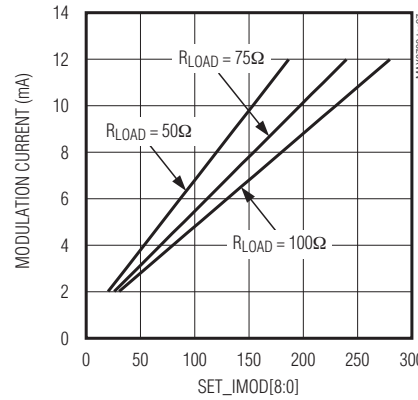
TRANSITION TIME vs. MODULATION CURRENT



TRANSITION TIME vs. DEEMPHASIS SETTING



MODULATION CURRENT vs. DAC SETTING

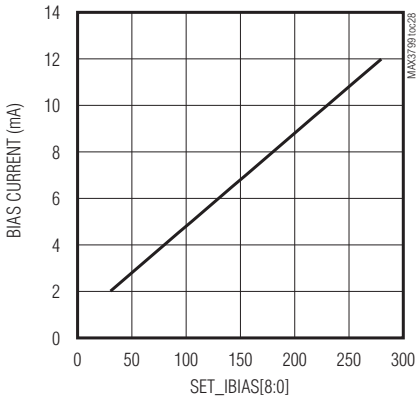


1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

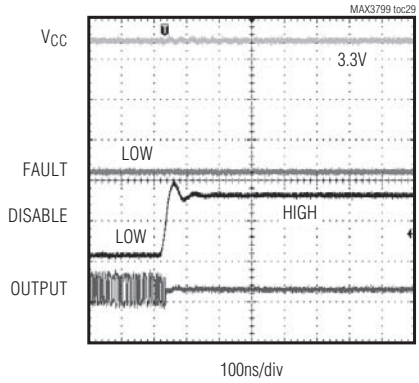
典型工作特性—VCSEL驱动器(续)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

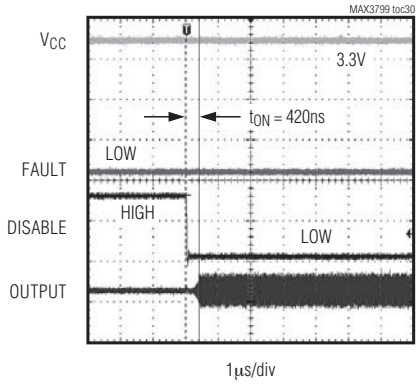
BIAS CURRENT vs. DAC SETTING



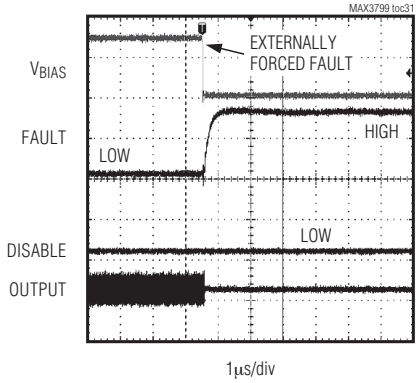
TRANSMITTER DISABLE



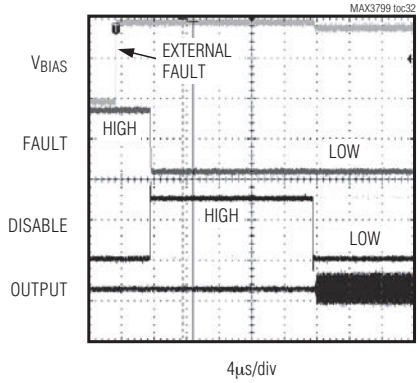
TRANSMITTER ENABLE



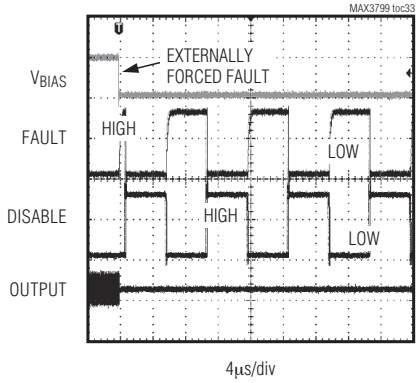
RESPONSE TO FAULT



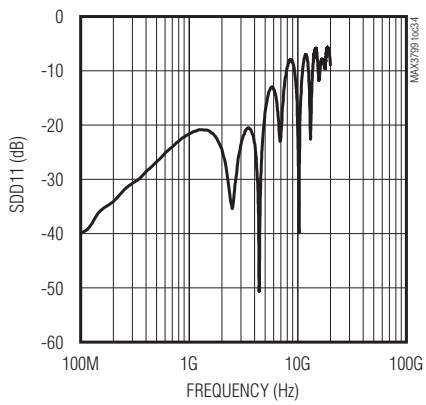
FAULT RECOVERY



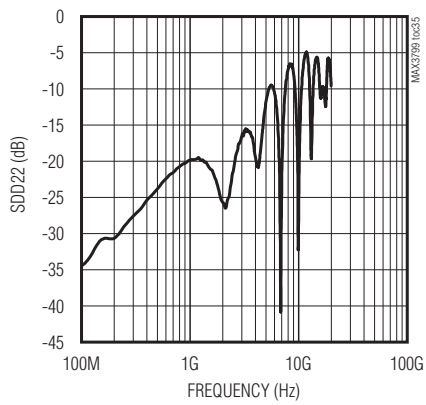
FREQUENCY ASSERTION OF DISABLE



Tx INPUT RETURN LOSS



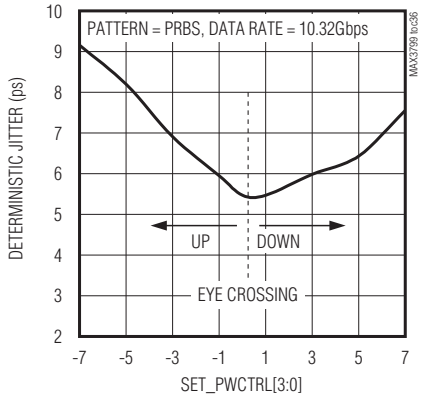
Tx OUTPUT RETURN LOSS



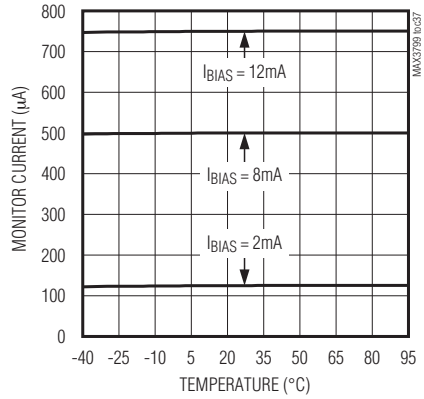
典型工作特性—VCSEL驱动器(续)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified. Figure 1 shows the typical setup used for measurements. Registers are set to default values unless otherwise noted, and the 3-wire interface is static during measurements. For testing, the RATE_SEL bit was used and the RSEL pin was left open.)

DETERMINISTIC JITTER vs. PULSE-WIDTH SETTING



BIAS MONITOR CURRENT vs. TEMPERATURE



引脚说明

引脚	名称	功能
1	LOS	信号丢失检测输出，漏极开路。当输入信号电平低于由SET_LOS DAC预设的门限时，LOS的默认极性为高电平。LOS功能的极性可通过设置LOS_POL = 0反转。通过设置LOS_EN = 0，可禁用LOS电路。
2	RSEL	模式选择输入，TTL/CMOS。将RSEL引脚或RATE_SEL位(通过3线数字接口设置)设置为逻辑高电平，即为宽带模式；将RSEL和RATE_SEL设置为逻辑低电平，即为高增益模式。RSEL引脚在内部由一个75kΩ电阻下拉至地。
3, 6, 27, 30	V_{CCR}	电源，为接收电路提供供电电压。
4	ROUT+	同相接收数据输出，CML。50Ω负载背向端接。
5	ROUT-	反相接收数据输出，CML。50Ω负载背向端接。
7	V_{CCD}	电源，为数字电路提供供电电压。
8	DISABLE	发送器禁用输入，TTL/CMOS。设置为逻辑低电平时正常工作；设置为逻辑高电平或开路时禁止产生调制和偏置电流。在内部通过一个8kΩ电阻上拉至V_{CCT}。
9	SCL	串行时钟输入，TTL/CMOS。该引脚具有一个75kΩ内部下拉电阻。
10	SDA	串行数据双向输入，TTL/CMOS，漏极开路输出。该引脚具有一个75kΩ内部上拉电阻，但需要一个4.7kΩ的外部上拉电阻，以满足3线数字时序要求(防止数据线发生冲突)。
11	CSEL	片选输入，TTL/CMOS。将CSEL设置为逻辑高电平时将启动一次工作过程；将CSEL设置为逻辑低电平时则终止工作过程，并复位控制状态机。通过内部75kΩ电阻下拉至地。
12, 15, 18, 21, 24, 25	V_{CCT}	电源，为发送电路提供供电电压。
13	TIN+	同相发送数据输入，CML。

1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

引脚说明(续)

引脚	名称	功能
14	TIN-	反相发送数据输入，CML。
16	BMON	偏置电流监测器输出。从该引脚流出的电流在一个外部电阻上产生以地为参考的电压，该电压与激光器偏置电流成正比。
17	V_{EET}	地，发送电路接地端。
19	TOUT-	反相调制电流输出，50Ω背向端接至V_{CCT}。
20	TOUT+	同相调制电流输出，50Ω背向端接至V_{CCT}。
22	BIAS	VCSEL偏置电流输出。
23	FAULT	发送器故障输出，漏极开路。逻辑高电平表示发生故障。发生故障后，即使在故障条件清除后，FAULT仍保持高电平。故障条件清除后，通过DISABLE信号清除故障锁定，使其变为低电平。
26	V_{EER}	地，接收电路接地端。
28	RIN-	反相接收数据输入，CML。
29	RIN+	同相接收数据输入，CML。
31	CAZ2	失调修正环路电容。连接在该引脚和CAZ1之间的电容用于设置失调修正环路的时间常数。通过数字接口设置控制位AZ_EN = 0，可禁用失调修正。
32	CAZ1	失调修正环路电容。与CAZ2相对应，内部连接至V_{EER}。
—	EP	裸焊盘，地。必须焊接至电路板地，以保证散热和电气性能(请参考*裸焊盘封装*部分)。

详细说明

MAX3799 SFP+收发器集成了带信号丢失检测功能的限幅放大器接收器和带故障保护功能的VCSEL激光驱动发送器。控制器通过3线接口实现MAX3799的高级Rx和Tx配置。MAX3799提供多个电流和电压DAC，允许配合使用低成本控制器IC。

限幅放大器接收器

MAX3799内部限幅放大器接收器的工作速率为1.0625Gbps至10.32Gbps。接收器包括一个双通道限幅器、失调修正电路、带去加重功能的CML输出级以及信号丢失检测电路。接收功能可通过片上3线接口控制。控制接收器功能的寄存器有RXCTRL1、RXCTRL2、RXSTAT、MODECTRL、SET_CML和SET_LOS。

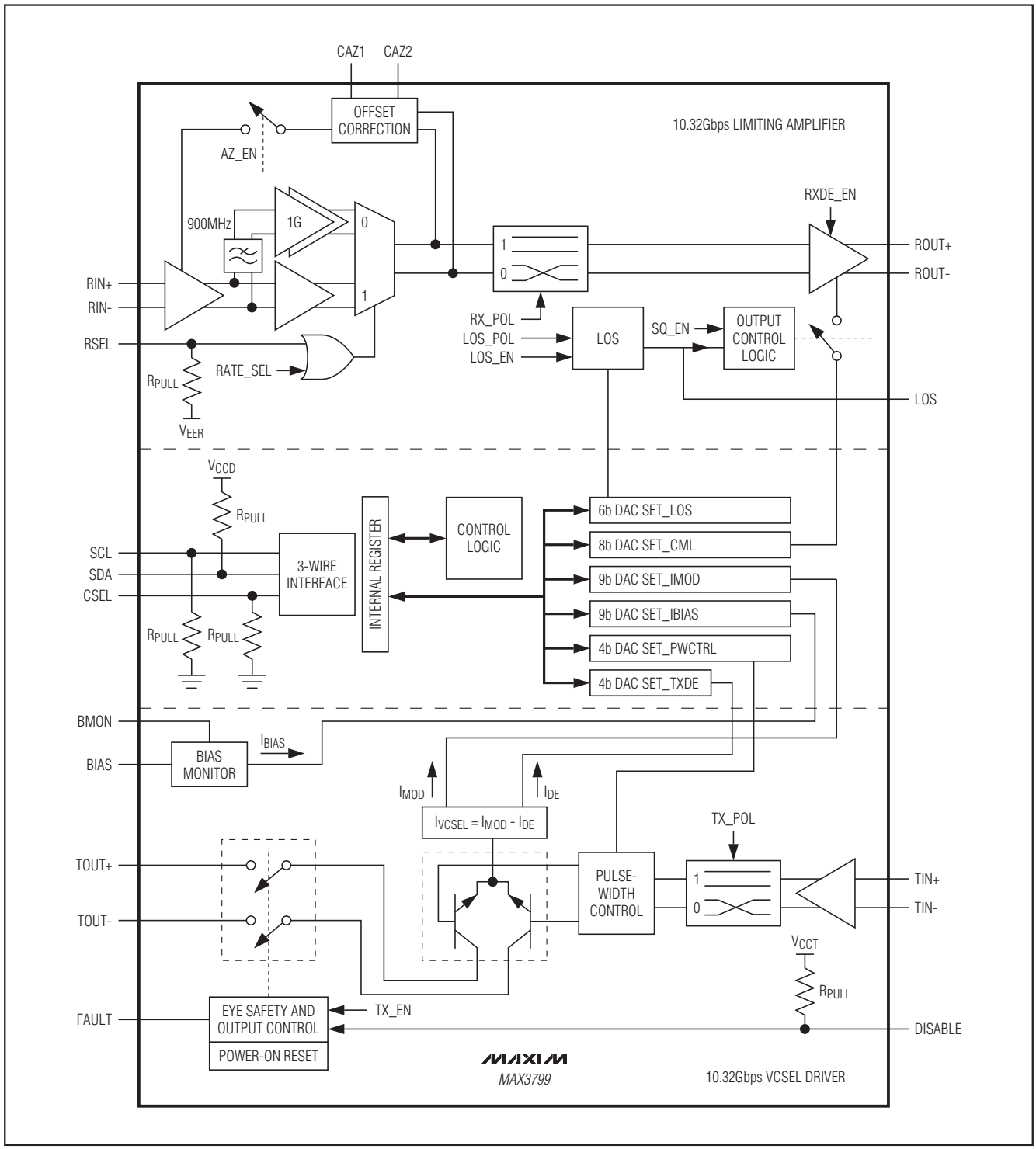

CAZ1
CAZ2
OFFSET CORRECTION
10.32Gbps LIMITING AMPLIFIER
AZ_EN
RXDE_EN
900MHz
1G
0
1
RIN+
RIN-
RSEL
RPULL
RATE_SEL
VEER
RX_POL
LOS_POL
LOS_EN
LOS
SQ_EN
OUTPUT CONTROL LOGIC
ROUT+
ROUT-
LOS
VCCD
RPULL
SCL
SDA
CSEL
3-WIRE INTERFACE
INTERNAL REGISTER
CONTROL LOGIC
6b DAC SET_LOS
8b DAC SET_CML
9b DAC SET_IMOD
9b DAC SET_IBIAS
4b DAC SET_PWCTRL
4b DAC SET_TXDE
BMON
BIAS
BIAS MONITOR
IBIAS
IMOD
IDE
IVCSEL = IMOD - IDE
TX_POL
TOUT+
TOUT-
PULSE-WIDTH CONTROL
TIN+
TIN-
VCCT
RPULL
FAULT
EYE SAFETY AND OUTPUT CONTROL
TX_EN
POWER-ON RESET
DISABLE
MAXIM
MAX3799
10.32Gbps VCSEL DRIVER

图2. 功能框图

1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

双通道限幅器

限幅放大器包括低数据速率模式(1.25Gbps)和高数据速率模式(高达10.32Gbps)，能够对整体系统进行优化处理。无论RSEL引脚还是RATE_SEL位均可用于速率选择。工作速率在1.25Gbps以下时，建议采用低数据速率模式(RATE_SEL = 0)；工作速率高达14.025Gbps时，建议采用高数据速率模式(RATE_SEL = 1)。ROUT+/ROUT-相对于RIN+/RIN-的极性通过RX_POL位设置。

失调修正电路

使能失调修正电路可消除差分放大级固有的失调电压所引起的脉宽失真，利用连接在CAZ1和CAZ2引脚之间的外部电容(C_{AZ})设置失调修正环路的截止频率。失调环路可通过AZ_EN位禁用。

带有去加重和摆率控制的CML输出级

CML输出级针对100Ω差分负载进行优化。RXDE_EN位可以控制向限幅差分输出信号加入模拟去加重补偿，以补偿SFP连接器损耗。输出级受控于RX_EN、SQ_EN位以及LOS引脚的组合，请参考表1。

CML输出级幅度受8位DAC寄存器(SET_CML)控制。差分输出幅度的范围为40mV_{P-P}至1200mV_{P-P}，分辨率为4.6mV_{P-P}(假设采用理想的100Ω差分负载)。

信号丢失(LOS)检测电路

输入数据幅度与6位DAC寄存器SET_LOS设置的门限相比较。LOS有效电平可在14mV_{P-P}至77mV_{P-P}范围内以1.5mV_{P-P}分辨率进行编程(假设采用理想的100Ω差分源)。LOS通过LOS_EN位使能，LOS极性受LOS_POL位控制。

VCSEL驱动器

MAX3799内部VCSEL驱动器的工作速率为1.0625Gbps至10.32Gbps。发送器包括具有脉宽调整功能的差分数据通路、偏置电流和调制电流DAC、带有可编程去加重的输出驱动、上电复位电路、BIAS监测器、VCSEL限流器以及视觉保护电路，通过3线数字接口控制发送器功能。控制发送器功能的寄存器有TXCTRL、TXSTAT1、TXSTAT2、SET_IBIAS、SET_IMOD、IMODMAX、IBIASMAX、MODINC、BIASINC、MODECTRL、SET_PWCTRL和SET_TXDE。

差分数据通路

CML输入缓冲器优化用于交流耦合信号，内部采用100Ω差分负载端接。差分输入数据用于补偿由SFP连接器引起的高频损耗。TXCTRL寄存器的TX_POL位用于控制TOUT+和TOUT-相对于TIN+和TIN-的极性。SET_PWCTRL寄存器控制输出眼图的交叉调节，状态指示位(TXED)监测是否存在交流输入信号。

表1. CML输出级工作模式

RX_EN	SQ_EN	LOS	OPERATION MODE DESCRIPTION
0	X	X	CML output disabled.
1	0	X	CML output enabled.
1	1	0	CML output enabled.
1	1	1	CML output disabled.

表2. CML输出级摆率控制

RATE_SEL	OPERATION MODE DESCRIPTION
0	1.25Gbps operation with reduced output edge speed.
1	Up to 10.32Gbps operation.

偏置电流DAC

MAX3799的偏置电流优化用于向50Ω至75Ω VCSEL负载提供高达15mA的偏置电流，分辨率为40µA。偏置电流由3线数字接口通过SET_IBIAS、IBIASMAX和BIASINC寄存器控制。

为了使VCSEL正常工作，IBIASMAX寄存器首先设置在所要求的最大偏置电流(最大为15mA)。流入VCSEL的偏置电流范围为0至IBIASMAX寄存器的设置值。偏置电流幅值保存在9位SET_IBIAS寄存器，只有第1位至第8位可写。SET_IBIAS的LSB (第0位)初始化为0，并通过BIASINC寄存器更新。

通过3线接口寻址BIASINC寄存器时，更新SET_IBIAS DAC寄存器值。BIASINC寄存器为8位寄存器，前5位以二进制补码格式储存递增信息。递增值范围从-8至+7 LSB。如果SET_IBIAS[8:1]的更新值超过IBIASMAX[7:0]，IBIASERR报警标识置位，而SET_IBIAS[8:0]保持不变。

调制电流DAC

MAX3799的调制电流优化用于向100Ω差分负载提供高达12mA的调制电流，分辨率为40µA。调制电流通过3线数字接口通过SET_IMOD、IMODMAX、MODINC和SET_TXDE寄存器进行控制。

为了使VCSEL正常工作，IMODMAX寄存器首先设置在所要求的最大调制电流(最大为12mA，驱动100Ω差分负载)，流入VCSEL的调制电流为0至IMODMAX寄存器的设置值。调制电流幅值保存在9位SET_IMOD寄存器，只有第1位至第8位可写。SET_IMOD的LSB (第0位)初始化为0，并通过MODINC寄存器更新。

通过3线接口寻址MODINC寄存器时，更新SET_IMOD DAC寄存器。MODINC寄存器为8位寄存器，前5位以二进制补码的格式储存递增信息，递增值范围从-8至+7 LSB。如果SET_IMOD[8:1]的更新值超过IMODMAX[7:0]，IMODERR报警标识置位，而SET_IMOD[8:0]保持不变。

输出驱动器

输出驱动器优化用于交流耦合100Ω差分负载。输出级的可编程去加重功能，将去加重幅值设置为调制电流的百分比。去加重功能通过TXDE_EN位使能。初始设置时，可使用SET_TXDE寄存器设置所要求的去加重总量。在系统工作期间，建议使用通过MODINC寄存器同时更新去加重(SET_TXDE)和调制电流DAC (SET_IMOD)的增量模式。

上电复位(POR)

上电复位确保激光器在电源电压达到规定门限(2.55V)之前处于关闭状态。上电复位后，偏置电流和调制电流缓慢爬升，以避免过冲。POR情况下，所有寄存器被复位到默认值。

偏置电流监测器

BMON引脚的输出电流典型值为I_{BIAS}的1/16。BMON端的接地电阻用于设置电压增益。如果BMON电压超过V_{CC} - 0.55V，内部比较器将锁存一次软故障。

视觉保护和输出控制电路

视觉保护和输出控制电路包括一个禁用引脚(DISABLE)和禁用位(TX_EN)，以及故障指示FAULT和故障检测器(图3)。MAX3799有两种故障：硬故障和软故障。硬故障触发FAULT引脚报警，并禁止VCSEL输出；软故障的工作方式更像一种报警，并不禁用输出。两种类型的故障储存在TXSTAT1和TXSTAT2寄存器。

FAULT引脚为锁存输出，可通过触发DISABLE引脚清除锁存状态。触发DISABLE引脚还会清零TXSTAT1和TXSTAT2寄存器。单点故障可能是对V_{CC}或GND短路，表3所示为不同单点故障下的电路响应。

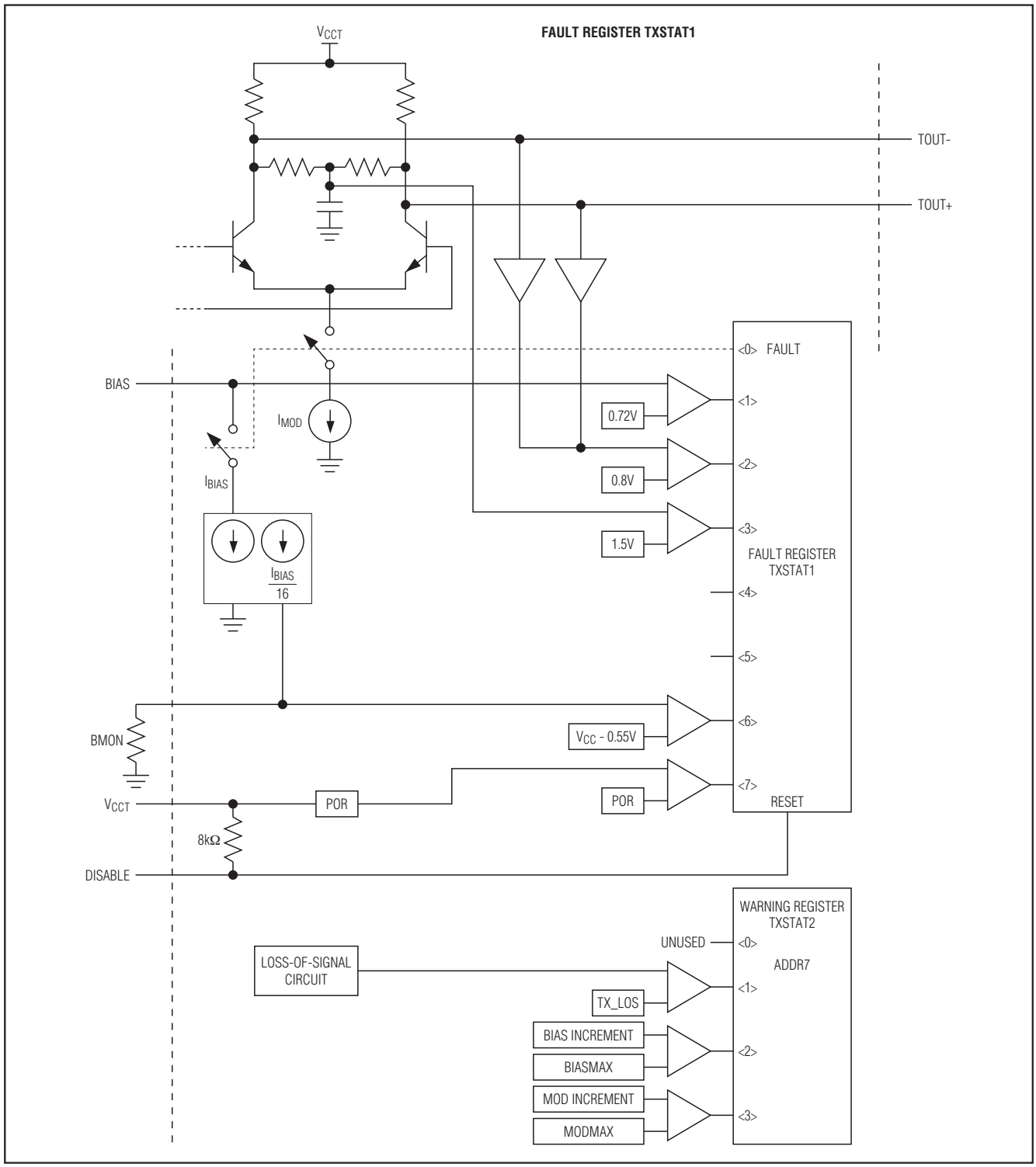

FAULT REGISTER TXSTAT1
VCCT
TOUT-
TOUT+
BIAS
IMOD
IBIAS
IBIAS
16
0.72V
0.8V
1.5V
<0> FAULT
<1>
<2>
<3>
FAULT REGISTER
TXSTAT1
<4>
<5>
<6>
<7>
RESET
VCC - 0.55V
POR
POR
BMON
VCCT
8kΩ
DISABLE
WARNING REGISTER
TXSTAT2
UNUSED
<0>
ADDR7
LOSS-OF-SIGNAL
CIRCUIT
TX_LOS
<1>
BIAS INCREMENT
BIASMAX
MOD INCREMENT
MODMAX
<2>
<3>

图3. 视觉保护电路

表3. 单点故障的电路响应

PIN	NAME	SHORT TO V_{CC}	SHORT TO GND	OPEN
1	LOS	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
2	RSEL	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
3	V_{CCR}	Normal	Disabled—HARD FAULT (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
4	ROUT+	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
5	ROUT-	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
6	V_{CCR}	Normal	Disabled—HARD FAULT (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
7	V_{CCD}	Normal	Disabled—HARD FAULT	Disabled—HARD FAULT
8	DISABLE	Disabled	Normal (Note 1). Can only be disabled with other means.	Disabled
9	SCL	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
10	SDA	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
11	CSEL	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
12	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
13	TIN+	SOFT FAULT	SOFT FAULT	Normal (Note 1)
14	TIN-	SOFT FAULT	SOFT FAULT	Normal (Note 1)
15	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
16	BMON	Disabled—HARD FAULT	Normal (Note 1)	Disabled—HARD FAULT
17	V_{EET}	Disabled—Fault (external supply shorted) (Note 2)	Normal	Disabled—HARD FAULT
18	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
19	TOUT-	I_{MOD} is reduced	Disabled—HARD FAULT	I_{MOD} is reduced
20	TOUT+	I_{MOD} is reduced	Disabled—HARD FAULT	I_{MOD} is reduced
21	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
22	BIAS	I_{BIAS} is on—No Fault	Disabled—HARD FAULT	Disabled—HARD FAULT
23	FAULT	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
24	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
25	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
26	V_{EER}	Disabled—Fault (external supply shorted) (Note 2)	Normal	Normal (Note 3)—Redundant path
27	V_{CCR}	Normal	Disabled—HARD FAULT (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
28	RIN-	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
29	RIN+	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)

表3. 单点故障的电路响应(续)

PIN	NAME	SHORT TO V_{CC}	SHORT TO GND	OPEN
30	V_{CCR}	Normal	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path
31	CAZ2	Normal (Note 1)	Normal (Note 1)	Normal (Note 1)
32	CAZ1 (V_{EER})	Disabled—Fault (external supply shorted) (Note 2)	Normal (Note 3)—Redundant path	Normal (Note 3)—Redundant path

注1：正常—不影响激光器功率。
注2：假设电源短路电流主要位于电路板上(本器件之外)，主电源由于短路损坏。
注3：功能正常，但性能会受影响。
警告：有些引脚短路至V_{CC}或对地短路会超出*Absolute Maximum Ratings*的规定值。

3线数字通信

MAX3799采用专用的3线数字接口，由外部控制器产生时钟。3线接口由SDA双向数据线、SCL时钟信号输入和CSEL片选输入(高电平有效)组成。外部主控制器通过使能CSEL引脚启动一次数据传输。主控制器在CSEL引脚置1后开始产生时钟信号，所有的数据传输均为最高有效位(MSB)在前。

协议

每次操作包括16位传输(15位地址/数据，1位RWN)。总线主控制器向SCL发出16个时钟周期，所有操作向MAX3799传输8位数据，RWN位决定是读操作还是写操作，请参考表4。

寄存器地址

MAX3799具有17个可编程寄存器，表5列出了寄存器及其地址。

写模式(RWN = 0)

主控制器在SCL上共产生16个时钟周期，主控制器在时钟下降沿向SDA线上共输出16位数据(MSB在前)。主控制器通过将CSEL置0终止传输，图4所示为接口时序。

读模式(RWN = 1)

主控制器在SCL上共产生16个时钟周期，主控制器在时钟下降沿向SDA线上共输出8位数据(MSB在前)。发送RWN位后释放SDA，从器件在时钟的上升沿输出8位数据(MSB在前)。主控制器通过将CSEL置0终止传输，图4所示为接口时序。

模式控制

常规模式下允许对MODINC和BIASINC以外的所有寄存器执行只读命令。常规模式下可以更新MODINC和BIASINC寄存器，这种操作可以通过3线接口将激光器的控制刷新速率提高2倍。常规模式为默认模式。

设置模式允许主控制器向状态寄存器(TXSTAT1、TXSTAT2和RXSTAT)以外的所有寄存器写入不受限制的数据。为了进入设置模式，MODECTRL寄存器(地址 = H0x0E)必须设置为H0x12。在MODECTRL寄存器置为H0x12后，随后的操作不再受限。在下一操作完成之后，自动退出设置模式。如果需要进行多次不受限设置，则必须重复这一过程。

表4. 数字通信字结构

BIT															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Address							RWN	Data that is written or read.							

表5. 寄存器说明和地址

ADDRESS	NAME	FUNCTION
H0x00	RXCTRL1	Receiver Control Register 1
H0x01	RXCTRL2	Receiver Control Register 2
H0x02	RXSTAT	Receiver Status Register
H0x03	SET_CML	Output CML Level Setting Register
H0x04	SET_LOS	LOS Threshold Level Setting Register
H0x05	TXCTRL	Transmitter Control Register
H0x06	TXSTAT1	Transmitter Status Register 1
H0x07	TXSTAT2	Transmitter Status Register 2
H0x08	SET_IBIAS	Bias Current Setting Register
H0x09	SET_IMOD	Modulation Current Setting Register
H0x0A	IMODMAX	Maximum Modulation Current Setting Register
H0x0B	IBIASMAX	Maximum Bias Current Setting Register
H0x0C	MODINC	Modulation Current Increment Setting Register
H0x0D	BIASINC	Bias Current Increment Setting Register
H0x0E	MODECTRL	Mode Control Register
H0x0F	SET_PWCTRL	Transmitter Pulse-Width Control Register
H0x10	SET_TXDE	Transmitter Deemphasis Control Register

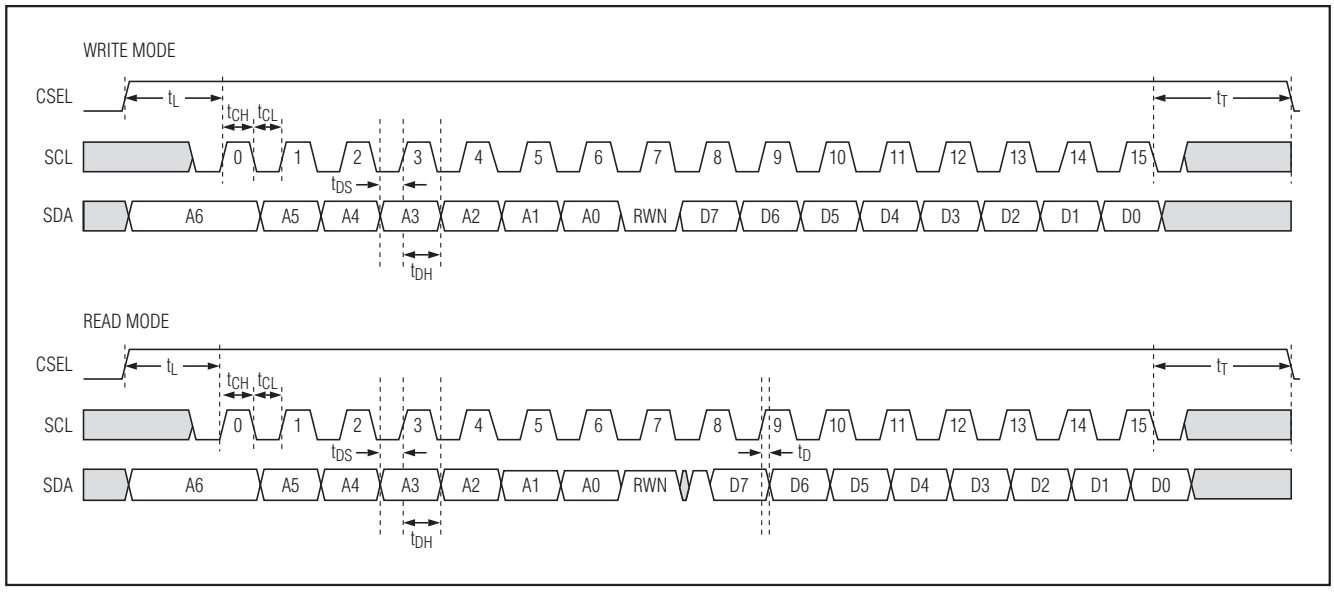


图4. 3线数字接口的时序

寄存器说明

接收器控制寄存器1 (RXCTRL1)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	X	X	X	X	RATE_SEL	X	H0x00
Default Value	X	X	X	X	X	X	0	X	

第1位：RATE_SEL。RATE_SEL与RSEL引脚通过逻辑或组合，选择低数据速率模式(1.25Gbps)或高数据速率模式(高达10.32Gbps)。

逻辑或输出0 = 1Gbps模式

逻辑或输出1 = 10Gbps模式

接收器控制寄存器2 (RXCTRL2)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	LOS_EN	LOS_POL	RX_POL	SQ_EN	RX_EN	RXDE_EN	AZ_EN	H0x01
Default Value	X	1	1	1	0	1	0	1	

第6位：LOS_EN。控制LOS电路，当RX_EN置0时，也将禁用LOS检测器。

0 = 禁用

1 = 使能

第5位：LOS_POL。控制LOS引脚的输出极性。

0 = 反相

1 = 正常

第4位：RX_POL。控制接收器信号通路的极性。

0 = 反相

1 = 正常

第3位：SQ_EN。当SQ_EN = 1时，LOS控制输出电路。

0 = 禁用

1 = 使能

第2位：RX_EN。使能或禁用接收器电路。

0 = 禁用

1 = 使能

第1位：RXDE_EN。使能或禁用接收器输出的去加重。

0 = 禁用

1 = 使能

第0位：AZ_EN。使能或禁用自动调零电路。当RX_EN置0时，也将禁用自动调零电路。

0 = 禁用

1 = 使能

接收器状态寄存器(RXSTAT)

Bit #	7	6	5	4	3	2	1	0 (STICKY)	ADDRESS
Name	X	X	X	X	X	X	X	LOS	H0x02
Default Value	X	X	X	X	X	X	X	X	

第0位：LOS。LOS输出电路的拷贝。这是一个关联位，读操作后被清零。第一次逻辑0至逻辑1变化时被锁存，直到主控制器读取该位或发生POR后清零。

输出CML电平设置寄存器(SET_CML)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_CML[7] (MSB)	SET_CML[6]	SET_CML[5]	SET_CML[4]	SET_CML[3]	SET_CML[2]	SET_CML[1]	SET_CML[0] (LSB)	H0x03
Default Value	0	1	0	1	0	0	1	1	

第7位至第0位：SET_CML[7:0]。SET_CML寄存器为8位寄存器，数值可以设置到最高255，对应于最高输出1000mV$_{P-P}$。关于典型CML输出电压和DAC编码之间的关系，请参考*典型工作特性*部分。

LOS门限电平设置寄存器(SET_LOS)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	SET_LOS[5] (MSB)	SET_LOS[4]	SET_LOS[3]	SET_LOS[2]	SET_LOS[1]	SET_LOS[0] (LSB)	H0x04
Default Value	X	X	0	0	1	1	0	0	

第5位至第0位：SET_LOS[5:0]。SET_LOS寄存器为6位寄存器，用于设置LOS门限。关于典型LOS门限电压和DAC编码之间的关系，请参考*典型工作特性*部分。

发送器控制寄存器(TXCTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	X	X	TXDE_EN	SOFTRES	TX_POL	TX_EN	H0x05
Default Value	X	X	X	X	0	0	1	1	

第3位：TXDE_EN。使能或禁止发送器输出去加重电路。

0 = 禁用

1 = 使能

第2位：SOFTRES。将所有寄存器复位到其默认值。

0 = 正常

1 = 复位

第1位：TX_POL。控制发送信号通路的极性。

0 = 反相

1 = 正常

第0位：TX_EN。使能或禁用发送电路。

0 = 禁用

1 = 使能

发送器状态寄存器1 (TXSTAT1)

Bit #	7 (STICKY)	6 (STICKY)	5 (STICKY)	4 (STICKY)	3 (STICKY)	2 (STICKY)	1 (STICKY)	0 (STICKY)	ADDRESS
Name	FST[7]	FST[6]	X	X	FST[3]	FST[2]	FST[1]	TX_FAULT	H0x06
Default Value	X	X	X	X	X	X	X	X	

第7位：FST[7]。当V_{CCT}电源电压低于2.45V时，POR电路报告故障。一旦V_{CCT}电源电压高于2.55V，POR将所有寄存器复位到其默认值，并清除故障。

第6位：FST[6]。当BMON电压高于V_{CC} - 0.55V时，报告一次软故障。

第3位：FST[3]。当$V_{TOUT+/-}$的共模电压低于1.5V时，报告一次软故障。

第2位：FST[2]。当$V_{TOUT+/-}$上的电压低于0.8V时，报告一次硬故障。

第1位：FST[1]。当BIAS电压低于0.44V时，报告一次硬故障。

第0位：TX_FAULT。FST[7]至FST[1]中故障信号的拷贝，POR将FST[7:1]复位至0。

发送器状态寄存器2 (TXSTAT2)

Bit #	7	6	5	4	3 (STICKY)	2 (STICKY)	1 (STICKY)	0 (STICKY)	ADDRESS
Name	X	X	X	X	IMODERR	IBIASERR	TXED	X	H0x07
Default Value	X	X	X	X	X	X	X	X	

第3位：IMODERR。当调制增量结果大于IMODMAX时，报告一次软故障，请参考*设置调制电流*部分。

第2位：IBIASERR。当偏置电流增量结果大于IBIASMAX时，报告一次软故障，请参考*设置偏置电流*部分。

第1位：TXED。仅表示发送器输入没有交流信号，并非LOS指示。

偏置电流设置寄存器(SET_IBIAS)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IBIAS [8] (MSB)	SET_IBIAS [7]	SET_IBIAS [6]	SET_IBIAS [5]	SET_IBIAS [4]	SET_IBIAS [3]	SET_IBIAS [2]	SET_IBIAS [1]	H0x08
Default Value	0	0	0	0	0	1	0	0	

第7位至第0位：SET_IBIAS[8:1]。偏置电流DAC共受9位数据控制。SET_IBIAS[8:1]位用于设置从0至510之间偏置电流的偶数值。LSB (SET_IBIAS[0])位受BIASINC寄存器控制，用来设置SET_IBIAS[8:0]偏置电流的奇数值。

调制电流设置寄存器(SET_IMOD)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IMOD [8] (MSB)	SET_IMOD [7]	SET_IMOD [6]	SET_IMOD [5]	SET_IMOD [4]	SET_IMOD [3]	SET_IMOD [2]	SET_IMOD [1]	H0x09
Default Value	0	0	0	1	0	0	1	0	

第7位至第0位：SET_IMOD[8:1]。调制电流DAC共受9位数据控制。SET_IMOD[8:1]位用于设置从0至510之间调制电流的偶数值。LSB (SET_IMOD[0])位受MODINC寄存器控制，用来设置SET_IMOD[8:0]中的奇数值。

最大调制电流设置寄存器(IMODMAX)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	IMODMAX [7] (MSB)	IMODMAX [6]	IMODMAX [5]	IMODMAX [4]	IMODMAX [3]	IMODMAX [2]	IMODMAX [1]	IMODMAX [0] (LSB)	H0x0A
Default Value	0	0	1	1	0	0	0	0	

第7位至第0位：IMODMAX[7:0]。IMODMAX寄存器为8位寄存器，用于限制最大调制电流。连续比较IMODMAX[7:0]与SET_IMOD[8:1]。

最大偏置电流设置寄存器(IBIASMAX)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	IBIASMAX [7] (MSB)	IBIASMAX [6]	IBIASMAX [5]	IBIASMAX [4]	IBIASMAX [3]	IBIASMAX [2]	IBIASMAX [1]	IBIASMAX [0] (LSB)	H0x0B
Default Value	0	0	0	1	0	0	1	0	

第7位至第0位：IBIASMAX[7:0]。IBIASMAX寄存器为8位寄存器，用于限制最大偏置电流。连续比较IBIASMAX[7:0]与SET_IBAS[8:1]。

调制电流递增设置寄存器(MODINC)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IMOD [0]	X	DE_INC	MODINC[4] (MSB)	MODINC[3]	MODINC[2]	MODINC[1]	MODINC[0] (LSB)	H0x0C
Default Value	0	0	0	0	0	0	0	0	

第7位：SET_IMOD[0]。该位是SET_IMOD[8:0]位的最低有效位，仅可利用MODINC[4:0]进行更新。

第5位：DE_INC。该位置1，并且使能发送输出的去加重时，SET_TXDE[3:0]被增加或减少1个LSB。递增或递减由MODINC[4:0]的符号位决定。

第4位至第0位：MODINC[4:0]。这些位用于增大或减小调制电流。写入时，SET_IMOD[8:0]位被更新，MODINC[4:0]为二进制补码。

偏置电流递增设置寄存器(BIASINC)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_IBIAS [0]	X	X	BIASINC[4] (MSB)	BIASINC[3]	BIASINC[2]	BIASINC[1]	BIASINC[0] (LSB)	H0x0D
Default Value	0	0	0	0	0	0	0	0	

第7位：SET_IBIAS[0]。该位是SET_IBIAS[8:0]的最低有效位，仅可利用BIASINC[4:0]进行更新。

第4位至第0位：BIASINC[4:0]。这些位用来增大或减小偏置电流。写入时，SET_IBIAS[8:0]位被更新，BIASINC[4:0]为二进制补码。

模式控制寄存器(MODECTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	MODECTRL [7] (MSB)	MODECTRL [6]	MODECTRL [5]	MODECTRL [4]	MODECTRL [3]	MODECTRL [2]	MODECTRL [1]	MODECTRL [0] (LSB)	H0x0E
Default Value	0	0	0	0	0	0	0	0	

第7位至第0位：MODECTRL[7:0]。MODECTRL寄存器使能常规模式和设置模式之间的转换。将该寄存器置为H0x12时为设置模式。MODECTRL必须在每次写操作之前更新。MODINC和BIASINC除外，它们可在常规模式下更新。

发送器脉宽控制寄存器(SET_PWCTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	X	X	SET_ PWCTRL[3] (MSB)	SET_ PWCTRL[2]	SET_ PWCTRL[1]	SET_ PWCTRL[0] (LSB)	H0x0F
Default Value	X	X	X	X	0	0	0	0	

第3位至第0位：SET_PWCTRL[3:0]。这是一个4位寄存器，通过调节脉冲宽度控制眼图交叉点。

发送器去加重控制寄存器(SET_TXDE)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	X	X	SET_TXDE [3] (MSB)	SET_TXDE [2]	SET_TXDE [1]	SET_TXDE [0] (LSB)	H0x10
Default Value	X	X	X	X	0	0	0	0	

第3位至第0位：SET_TXDE[3:0]。这是一个4位寄存器，控制发送器输出的去加重总量。在计算总调制电流时，必须考虑去加重总量。去加重设置为调制电流的百分比。

设计步骤

设置偏置电流

1) IBIASMAX[7:0] = Maximum_Bias_Current_Value

2) $SET\_IBIAS_i[8:1]$ = Initial_Bias_Current_Value

注：利用SET_IBIAS[8:0]寄存器计算总的偏置电流。SET_IBIAS[8:1]位可手动写入，SET_IBIAS[0]只能利用BIASINC[4:0]寄存器更新。

采用APC环路时，建议使用BIASINC[4:0]寄存器，可保证偏置电流更新速度最快。

3) $BIASINC_i[4:0]$ = New_Increment_Value

4) 如果：($SET\_IBIAS_i[8:1] \le$ IBIASMAX[7:0])，
则：($SET\_IBIAS_i[8:0] = SET\_IBIAS_{i-1}[8:0] + BIASINC_i[4:0]$)

5) 否则：($SET\_IBIAS_i[8:0] = SET\_IBIAS_{i-1}[8:0]$)

总偏置电流计算如下：

6) $I_{BIAS} = [SET\_IBIAS_i[8:0] + 20] \times 40\mu A$

设置调制电流

1) IMODMAX[7:0] = Maximum_Modulation_Current_Value

2) $SET\_IMOD_i[8:1]$ = Initial_Modulation_Current_Value

注：利用SET_IMOD[8:0]寄存器计算总调制电流。SET_IMOD[8:1]位可手动写入，SET_IMOD[0]只能利用MODINC[4:0]寄存器刷新。

当采用调制补偿时，建议使用MODINC[4:0]寄存器，可保证调制电流的更新速度最快。

3) $MODINC_i[4:0]$ = New_Increment_Value

4) 如果：($SET\_IMOD_i[8:1] \le$ IMODMAX[7:0])，
则：($SET\_IMOD_i[8:0] = SET\_IMOD_{i-1}[8:0] + MODINC_i[4:0]$)

5) 否则：($SET\_IMOD_i[8:0] = SET\_IMOD_{i-1}[8:0]$)

下式在假设采用片上100Ω差分电阻和100Ω外部差分负载(Rextd)条件下成立。SET_TXDE[3:0]最大值设置为11。

6) $I_{MOD(Rextd=100\Omega)} = [(20 + SET\_IMOD_i[8:0]) \times 40\mu A] \times \left[1 - \frac{2 + SET\_TXDE[3:0]}{64}\right]$

对于常用的Rextd，采用与如下Rextd = 100Ω相同的设置设定$SET_IMOD_i[8:0]$，得到调制电流。它可以作为$I_{MOD(Rextd = 100\Omega)}$的一个函数写入，仍假设采用100Ω片上负载。

7) $I_{MOD(Rextd)} = 2 \times I_{MOD(Rextd=100\Omega)} \left[\frac{Rext}{Rext + 100}\right]$

编程LOS门限

$$LOS_{TH} = (SET\_LOS[5:0] \times 1.5mV_{P-P})$$

设置发送器输出去加重

TXDE_EN位必须置1才能使能去加重功能。SET_TXDE寄存器用于设置去加重量，它是调制电流的百分比。去加重百分比由下式确定：

$$DE(\%) = \frac{100 \times (2 + SET\_TXDE[3:0])}{64}$$

其中，最大SET_TXDE[3:0] = 11。

对于10mA的I_{MOD}，最大去加重值大约为20%。对于12mA的满幅I_{MOD}，最大去加重限制为15%。

使能去加重功能时，利用计算出的去加重百分比减小调制电流的幅度。为了保持调制电流幅值恒定，SET_IMOD[8:0]寄存器必须增加去加重百分比。如果系统条件，例如温度、所要求的I_{MOD}等在发送期间发生变化，可能需要重新调整去加重设置。对于这种去加重的临时调整情况，建议使用

1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

DE_INC (MODINC[5])位。利用该位可根据MODINC[4:0]的增量符号及此处的SET_IMOD[8:0]设置，将去加重编码增加或减少1个LSB。这有助于在连续发送情况下保持BER，并可灵活地通过适当调整去加重来改善信号质量。这一功能在保持优异的BER性能的同时可以无干扰地调节去加重。

使能接收器输出去加重

为了使能去加重功能，RXDE_EN位必须置1。去加重使ROUT+/ROUT-的输出幅度降低25%，为了保持与去加重使能之前相同的输出幅度，需要将SET_CML寄存器值提高25%。去加重使能时，限幅放大器能够在高达800mV$_{P-P}$的典型输出幅度下保证其交流指标。SET_CML寄存器可以设置0至255位，值得注意的是仅在215位以内保证其性能。

设置脉宽控制

Tx输出的眼图交叉点可利用SET_PWCTRL寄存器进行调整，表6列出了相关设置。

数字符号规定了脉宽偏移方向，编码1111对应于差分输出的平衡状态。脉宽偏移量可围绕平衡状态双向调节(请参见*典型工作特性*部分)。

编程CML输出设置

CML输出幅度由8位DAC寄存器(SET_CML)控制。差分输出幅度高达1000mV$_{P-P}$，分辨率为4.6mV$_{P-P}$ (假设采用理想的100Ω差分负载)。输出CML DAC范围确保高达215。

$$输出电压R_{OUT}\ (mV_{P-P}) = 40 + 4.55\ (SET\_CML)$$

选择耦合电容

对于交流耦合，耦合电容C_{IN}和C_{OUT}的选择应将接收器的确定性抖动降至最小。当输入低频截止点(f_{IN})降低时，抖动会减小。

$$f_{IN} = 1/[2\pi(50)(C_{IN})]$$

推荐MAX3799采用0.1µF的C_{IN}和C_{OUT}。

选择失调修正电容

CAZ1和CAZ2之间的电容决定了信号通路直流失调抑制环路的时间常数。为了保持稳定，使f_{IN}和直流失调抑制环路对应的低频截止点(f_{OC})保持至少10倍频的间隔非常重要。建议MAX3799的CAZ1和CAZ2之间使用1nF电容。

应用信息

布局考虑

为了将寄生电感降至最小，MAX3799的输出引脚与激光二极管应尽可能靠近安装。在靠近激光二极管阳极的位置安装一个旁路电容，以优化激光二极管性能。采用良好的高频布线工艺以及不间断接地区域的多层电路板，将EMI和串扰降至最小。

裸焊盘封装

32引脚TQFN封装的裸焊盘为IC提供了一条低热阻的散热通道。该焊盘也是MAX3799的电气地，必须焊接到电路板地，以保证散热和电气性能。更多信息请参考应用笔记862：*HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

激光器安全和IEC 825

单独使用MAX3799激光驱动器不能保证发送器设计完全符合IEC 825标准。必须考虑整体发送电路和元件选择。每个用户必须确定具体应用的容错等级，了解Maxim产品并非专门设计用于或授权用于外科移植手术以及生命支持、维持系统的器件，或其它任何可能因为Maxim器件失效而导致人员伤亡的应用。

表6. SET_PWCTRL的眼图交叉点设置

SET_PWCTRL[3:0]	PWD	SET_PWCTRL[3:0]	PWD
1000	-7	0111	8
1001	-6	0110	7
1010	-5	0101	6
1011	-4	0100	5
1100	-3	0011	4
1101	-2	0010	3
1110	-1	0001	2
1111	0	0000	1

表7. 寄存器汇总表

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER /TYPE	BIT NAME	DEFAULT VALUE	NOTES
Receiver Control Register 1 **Address = H0x00**	RXCTRL1	R	RW	1	RATE_SEL	0	Mode-select 0: high-gain mode, 1: high-bandwidth mode
Receiver Control Register 2 **Address = H0x01**	RXCTRL2	R	RW	6	LOS_EN	1	LOS control 0: disable, 1: enable (always 0 when RX_EN = 0)
		R	RW	5	LOS_POL	1	LOS polarity 0: inverse, 1: normal
		R	RW	4	RX_POL	1	Rx polarity 0: inverse, 1: normal
		R	RW	3	SQ_EN	0	Squelch 0: disable, 1: enable
		R	RW	2	RX_EN	1	Rx control 0: disable, 1: enable
		R	RW	1	RXDE_EN	0	Rx deemphasis 0: disable, 1: enable
		R	RW	0	AZ_EN	1	Rx autozero control 0: disable, 1: enable (always 0 when RX_EN = 0)
Receiver Status Register **Address = H0x02**	RXSTAT	R	R	0 (sticky)	LOS	X	Copy of LOS output signal
Output CML Level Setting Register **Address = H0x03**	SET_CML	R	RW	7	SET_CML[7]	0	MSB output level DAC
		R	RW	6	SET_CML[6]	1	
		R	RW	5	SET_CML[5]	0	
		R	RW	4	SET_CML[4]	1	
		R	RW	3	SET_CML[3]	0	
		R	RW	2	SET_CML[2]	0	
		R	RW	1	SET_CML[1]	1	
		R	RW	0	SET_CML[0]	1	LSB output level DAC
LOS Threshold Level Setting Register **Address = H0x04**	SET_LOS	R	RW	5	SET_LOS[5]	0	MSB LOS threshold DAC
		R	RW	4	SET_LOS[4]	0	
		R	RW	3	SET_LOS[3]	1	
		R	RW	2	SET_LOS[2]	1	
		R	RW	1	SET_LOS[1]	0	
		R	RW	0	SET_LOS[0]	0	LSB LOS threshold DAC

表7. 寄存器汇总表(续)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER /TYPE	BIT NAME	DEFAULT VALUE	NOTES
Transmitter Control Register **Address = H0x05**	TXCTRL	R	RW	3	TXDE_EN	0	Tx deemphasis 0: disable, 1: enable
		R	RW	2	SOFTRES	0	Global digital reset
		R	RW	1	TX_POL	1	Tx polarity 0: inverse, 1: normal
		R	RW	0	TX_EN	1	Tx control 0: disable, 1: enable
Transmitter Status Register 1 **Address = H0x06**	TXSTAT1	R	R	7 (sticky)	FST[7]	X	TX_POR → TX_VCC low-limit violation
		R	R	6 (sticky)	FST[6]	X	BMON open/shorted to V_{CC}
		R	R	5 (sticky)	X	X	
		R	R	4 (sticky)	X	X	
		R	R	3 (sticky)	FST3]	X	V_{TOUT}+/- common-mode low-limit violation
		R	R	2 (sticky)	FST[2]	X	V_{TOUT}+/- low-limit violation
		R	R	1 (sticky)	FST[1]	X	BIAS open or shorted to GND
		R	R	0 (sticky)	TX_FAULT	X	Copy of FAULT signal in case POR bits 6 to 1 reset to 0
Transmitter Status Register 2 **Address = H0x07**	TXSTAT2	R	R	3 (sticky)	IMODERR	X	Warning increment result > IMODMAX
		R	R	2 (sticky)	IBIASERR	X	Warning increment result > IBIASMAX
		R	R	1 (sticky)	TXED	X	Tx edge detection
		R	R	0 (sticky)	Unused	X	Unused
Bias Current Setting Register **Address = H0x08**	SET_IBIAS	R	RW	8	SET_IBIAS[8]	0	MSB bias DAC
		R	RW	7	SET_IBIAS[7]	0	
		R	RW	6	SET_IBIAS[6]	0	
		R	RW	5	SET_IBIAS[5]	0	
		R	RW	4	SET_IBIAS[4]	0	
		R	RW	3	SET_IBIAS[3]	1	
		R	RW	2	SET_IBIAS[2]	0	
		R	RW	1	SET_IBIAS[1]	0	
		Accessible through REG_ADDR = 13		0	SET_IBIAS[0]	0	LSB bias DAC

表7. 寄存器汇总表(续)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER /TYPE	BIT NAME	DEFAULT VALUE	NOTES
Modulation Current Setting Register **Address = H0x09**	SET_IMOD	R	RW	8	SET_IMOD[8]	0	MSB modulation DAC
		R	RW	7	SET_IMOD[7]	0	
		R	RW	6	SET_IMOD[6]	0	
		R	RW	5	SET_IMOD[5]	1	
		R	RW	4	SET_IMOD[4]	0	
		R	RW	3	SET_IMOD[3]	0	
		R	RW	2	SET_IMOD[2]	1	
		R	RW	1	SET_IMOD[1]	0	
		Accessible through REG_ADDR = 12		0	SET_IMOD[0]	0	LSB modulation DAC
Maximum Modulation Current Setting Register **Address = H0x0A**	IMODMAX	R	RW	7	IMODMAX[7]	0	MSB modulation limit
		R	RW	6	IMODMAX[6]	0	
		R	RW	5	IMODMAX[5]	1	
		R	RW	4	IMODMAX[4]	1	
		R	RW	3	IMODMAX[3]	0	
		R	RW	2	IMODMAX[2]	0	
		R	RW	1	IMODMAX[1]	0	
		R	RW	0	IMODMAX[0]	0	LSB modulation limit
Maximum Bias Current Setting Register **Address = H0x0B**	IBIASMAX	R	RW	7	IBIASMAX[7]	0	MSB bias limit
		R	RW	6	IBIASMAX[6]	0	
		R	RW	5	IBIASMAX[5]	0	
		R	RW	4	IBIASMAX[4]	1	
		R	RW	3	IBIASMAX[3]	0	
		R	RW	2	IBIASMAX[2]	0	
		R	RW	1	IBIASMAX[1]	1	
		R	RW	0	IBIASMAX[0]	0	LSB bias limit
Modulation Current Increment Setting Register **Address = H0x0C**	MODINC	R	R	7	SET_IMOD[0]	0	LSB of SET_IMOD DAC register address = H0x09
		R	R	6	X	0	
		R	R	5	DE_INC	0	Deemphasis increment 0: no update, 1: SET_TXDE updates ±1 LSB
		RW	RW	4	MODINC[4]	0	MSB MOD DAC two's complement
		RW	RW	3	MODINC[3]	0	
		RW	RW	2	MODINC[2]	0	
		RW	RW	1	MODINC[1]	0	
		RW	RW	0	MODINC[0]	0	LSB MOD DAC two's complement

表7. 寄存器汇总表(续)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER /TYPE	BIT NAME	DEFAULT VALUE	NOTES
Bias Current Increment Setting Register **Address = H0x0D**	BIASINC	R	R	7	SET_IBIAS[0]	0	LSB of SET_IBIAS DAC register address = H0x08
		R	R	6	X	0	
		R	R	5	X	0	
		RW	RW	4	BIASINC[4]	0	MSB bias DAC two's complement
		RW	RW	3	BIASINC[3]	0	
		RW	RW	2	BIASINC[2]	0	
		RW	RW	1	BIASINC[1]	0	
		RW	RW	0	BIASINC[0]	0	LSB bias DAC two's complement
Mode Control Register **Address = H0x0E**	MODECTRL	RW	RW	7	MODECTRL[7]	0	MSB mode control
		RW	RW	6	MODECTRL[6]	0	
		RW	RW	5	MODECTRL[5]	0	
		RW	RW	4	MODECTRL[4]	0	
		RW	RW	3	MODECTRL[3]	0	
		RW	RW	2	MODECTRL[2]	0	
		RW	RW	1	MODECTRL[1]	0	
		RW	RW	0	MODECTRL[0]	0	LSB mode control
Transmitter Pulse-Width Control Register **Address = H0x0F**	SET_ PWCTRL	R	RW	3	SET_PWCTRL[3]	0	MSB Tx pulse-width control
		R	RW	2	SET_PWCTRL[2]	0	
		R	RW	1	SET_PWCTRL[1]	0	
		R	RW	0	SET_PWCTRL[0]	0	LSB Tx pulse-width control
Transmitter Deemphasis Control Register **Address = H0x10**	SET_TXDE	R	RW	3	SET_TXDE[3]	0	MSB Tx deemphasis
		R	RW	2	SET_TXDE[2]	0	
		R	RW	1	SET_TXDE[1]	0	
		R	RW	0	SET_TXDE[0]	0	LSB Tx deemphasis

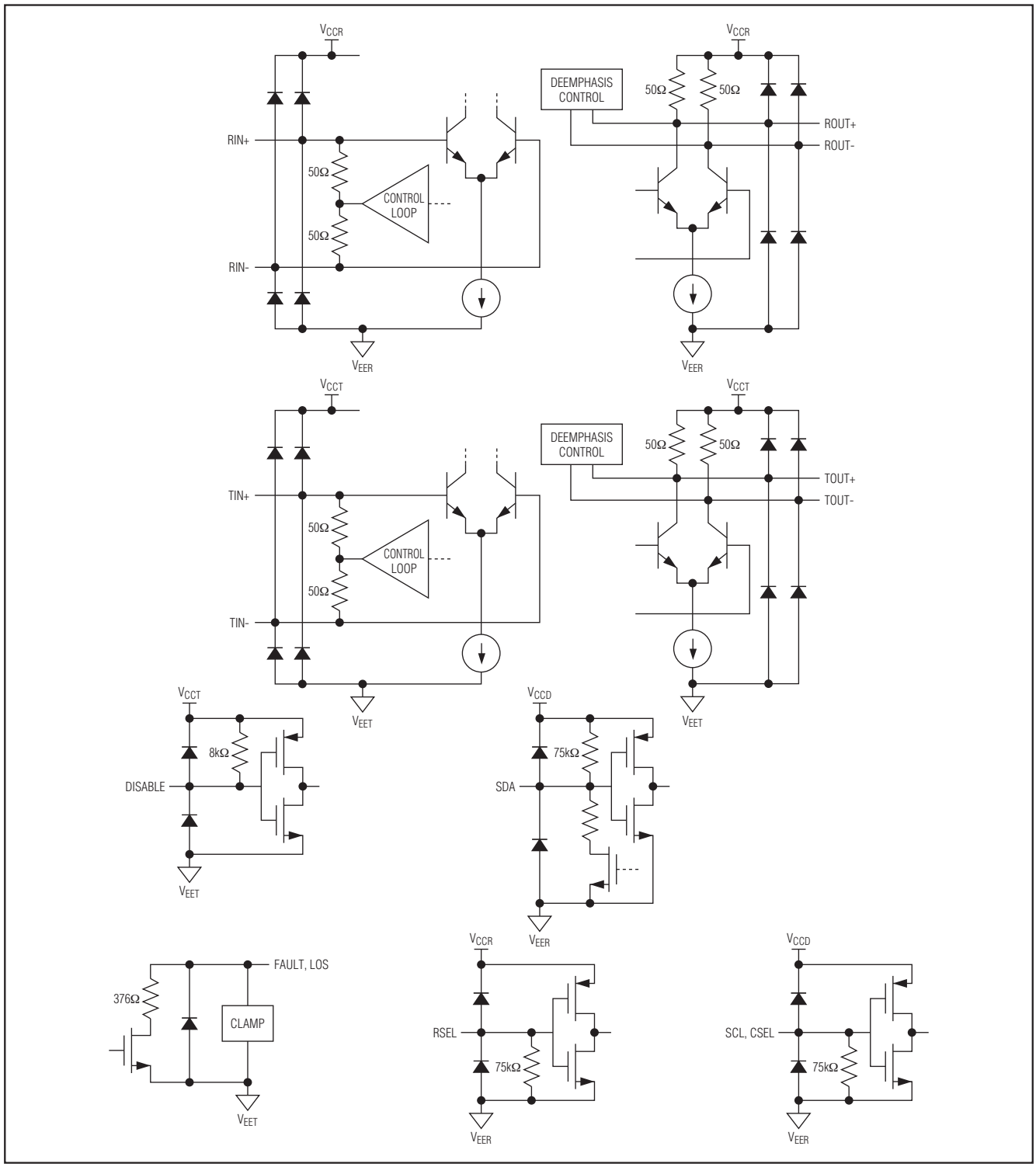
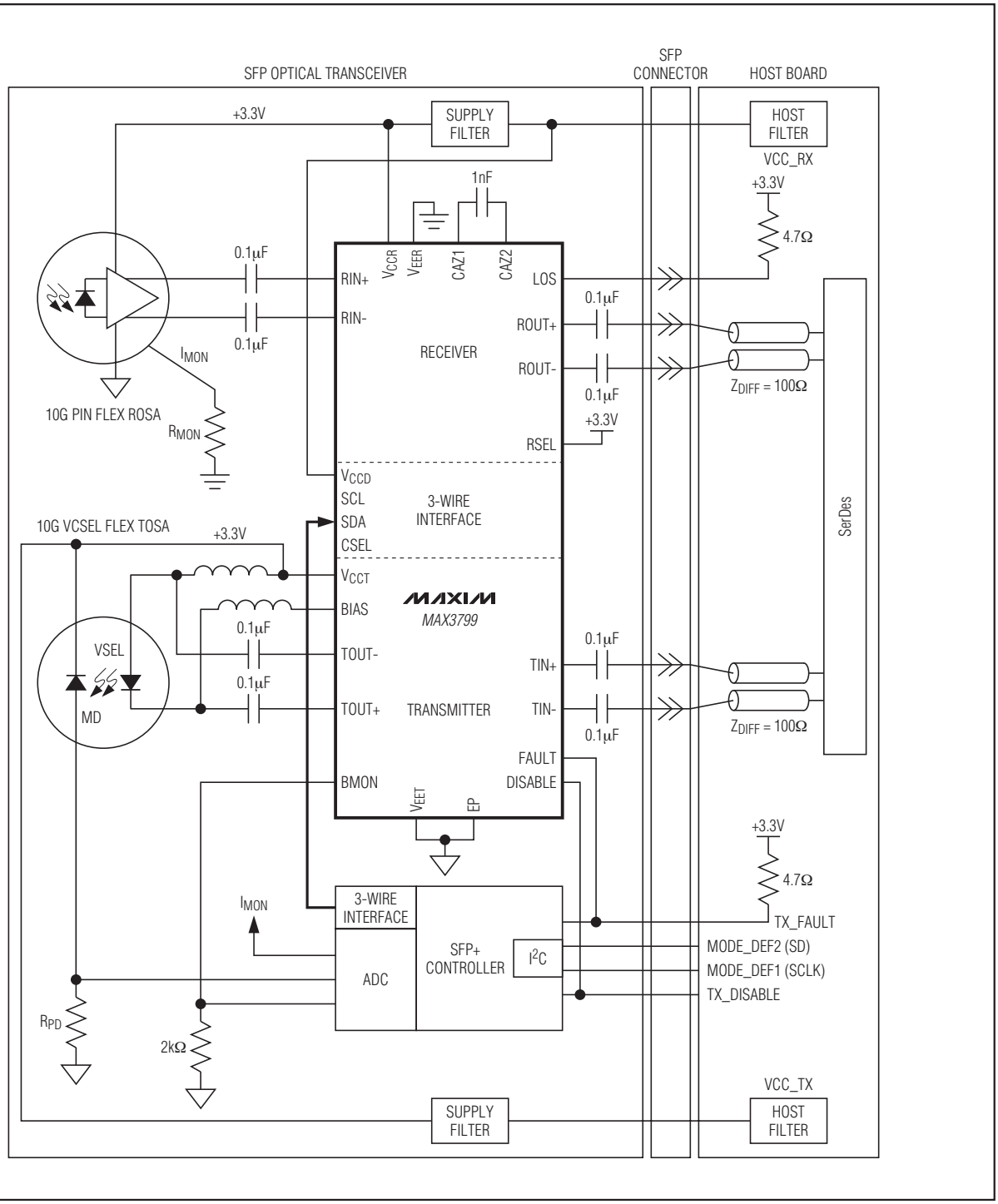

VCCR
RIN+
50Ω
CONTROL LOOP
50Ω
RIN-
VEER
DEEMPHASIS CONTROL
50Ω
50Ω
ROUT+
ROUT-
VCCT
TIN+
TIN-
TOUT+
TOUT-
VEET
VCCD
DISABLE
8kΩ
SDA
75kΩ
FAULT, LOS
376Ω
CLAMP
RSEL
SCL, CSEL

图5. I/O结构简化图

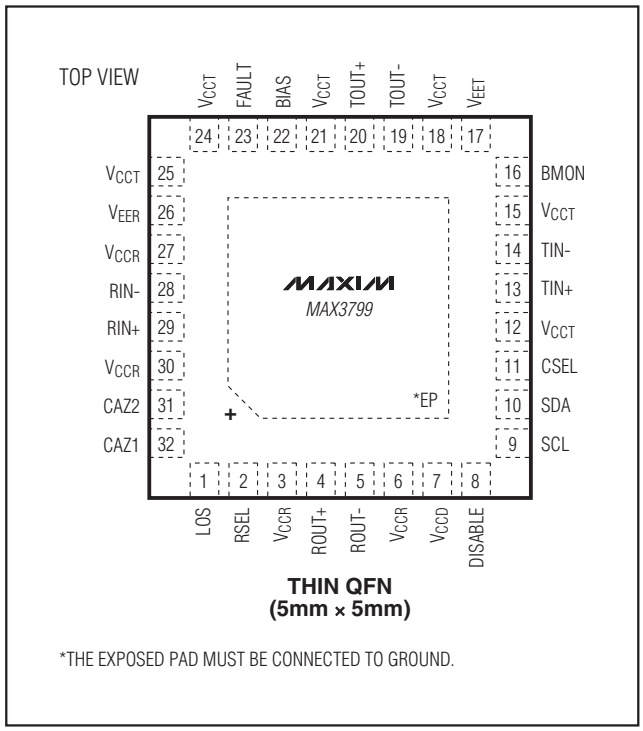
1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

典型应用电路



1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

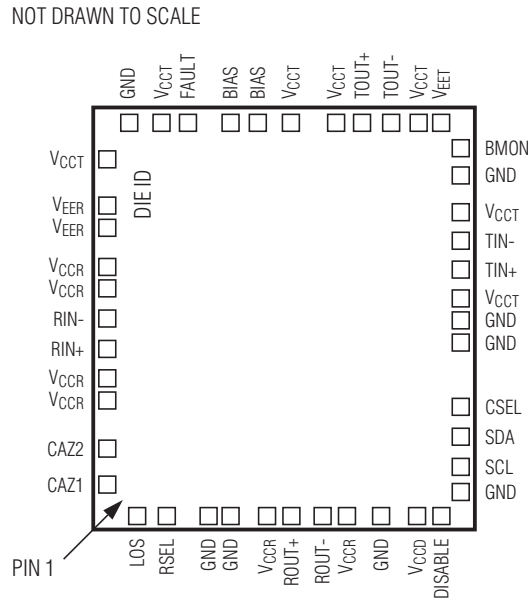
引脚配置



THIN QFN
(5mm × 5mm)

*THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

焊盘配置



DIE MAP
2800µm × 2550µm
(110.24mils × 100.39mils)

芯片信息

PROCESS: SiGe BiPOLAR

封装信息

如需最近的封装外形信息和焊盘布局，请查询 **china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
32 TQFN-EP	T3255+5	21-0140	90-0001

1Gbps至14Gbps、SFP+多速率限幅放大器和VCSEL驱动器

修订历史

修订号	修订日期	说明	修改页
0	8/09	最初版本。	—
1	6/10	在*定购信息*和*焊盘配置*部分中增加了裸片封装和焊盘配置信息。	1, 35

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