



50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

MAX2066

概述

MAX2066高线性度数字可变增益放大器(VGA)是单芯片SiGe BiCMOS衰减器及放大器,工作在50MHz至1000MHz频率范围,用于连接50Ω系统(参见典型应用电路)。可通过SPI™兼容接口控制作为从机外设的数字衰减器;也允许以1dB步长通过并行总线控制,可调节范围为31dB。该器件增加了“速射”增益选择,可直接设置在4种增益选项的一种,用户可通过SPI接口预先设置四种增益选项。2个控制引脚允许用户快速选择4种定制衰减的任何一个,无需SPI总线编程。

因为每一级电路都具有RF输入和RF输出,通过适当配置可以优化NF(第1级为放大器)或OIP3(最后一级为放大器)。该器件还包含具有22dB增益的放大器(放大器本身),增益最大时NF为5.2dB(包括衰减器的插入损耗),并提供+42.4dBm的高OIP3。这些特性使得MAX2066能够为众多接收器和发射器提供一个理想的VGA。

另外,MAX2066采用+5V单电源供电,提供功能完备的解决方案;工作在+3.3V时,性能指标略有降低,可以调节偏置电流在电流损耗和线性度方面进行折衷。器件采用紧凑、带裸焊盘的40引脚、薄型QFN封装(6mm x 6mm)。工作在扩展级温度范围($T_C = -40^{\circ}\text{C}$ 至 $+85^{\circ}\text{C}$)。

应用

IF和RF增益分级设计
蜂窝频段WCDMA和cdma2000®基站
GSM 850/GSM 900 EDGE基站
WiMAX和LTE基站以及用户驻地设备
固定宽带无线接入
无线本地环路
军用系统
视频点播(VOD)和DOCSIS®兼容于EDGE QAM调制
电缆调制解调器端接系统(CMTS)
RFID手持终端及门禁读卡器

SPI是Motorola, Inc.的商标。

特性

- ◆ 50MHz到1000MHz RF频率范围
- ◆ 引脚兼容的系列产品包括:
 - MAX2065 (模拟/数字VGA)
 - MAX2067 (模拟VGA)
- ◆ 20.5dB (典型值)最大增益
- ◆ 100MHz带宽内保持0.4dB增益平坦度
- ◆ 31dB增益范围
- ◆ 支持4种“速射”预编程衰减选项
 - 快速设置4种定制衰减之一,无需SPI总线编程
 - 理想用于快速响应和信号阻塞保护
 - 避免ADC过驱动
- ◆ 优异的线性指标(配置放大器为最后一级)
 - +42.4dBm OIP3
 - +65dBm OIP2
 - +19dBm输出1dB压缩点
 - 68dBc HD2
 - 88dBc HD3
- ◆ 5.2dB典型噪声系数(NF)
- ◆ 25ns快速数字切换
- ◆ 超低数字VGA过冲/欠冲幅度
- ◆ 单电源+5V供电(可选择+3.3V单电源供电)
- ◆ 优异的外部电流设置电阻,提供降功率/降性能两种工作模式

订购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2066ETL+	-40°C to +85°C	40 Thin QFN-EP*
MAX2066ETL+T	-40°C to +85°C	40 Thin QFN-EP*

+表示无铅封装。
*EP = 裸焊盘。
T = 卷带包装。

引脚配置在数据资料的最后给出。

cdma2000是电信工业协会的注册商标。
DOCSIS和CableLabs是Cable Television Laboratories, Inc. (CableLabs®)的注册商标。



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ABSOLUTE MAXIMUM RATINGS

VCC_ to GND	-0.3V to +5.5V	RF Input Power (AMP_IN).....	+18dBm
VDD_LOGIC, DATA, \overline{CS} , CLK, SER/PAR.....	-0.3V to (VCC_ + 0.3V)	Continuous Power Dissipation (Note 1)	6.5W
STATE_A, STATE_B, D0–D4	-0.3V to (VCC_ + 0.3V)	θ_{JA} (Notes 2, 3).....	+38°C/W
AMP_IN, AMP_OUT	-0.3V to (VCC_ + 0.3V)	θ_{JC} (Note 3)	+10°C/W
ATTEN_IN, ATTEN_OUT.....	-1.2V to +1.2V	Operating Temperature Range (Note 4).....	$T_C = -40^\circ\text{C}$ to $+85^\circ\text{C}$
RSET to GND.....	-0.3V to +1.2V	Maximum Junction Temperature	+150°C
RF Input Power (ATTEN_IN, ATTEN_OUT).....	+20dBm	Storage Temperature Range	-65°C to +150°C
		Lead Temperature (soldering, 10s)	+300°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a printed-circuit board (PCB). See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com.cn/thermal-tutorial.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, high-current (HC) mode, $V_{CC} = V_{DD} = +3.0\text{V}$ to $+3.6\text{V}$, $T_C = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values are at $V_{CC} = V_{DD} = +3.3\text{V}$ and $T_C = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 5)	3.0	3.3	3.6	V
Supply Current	I_{CC}			58	80	mA
LOGIC INPUTS (DATA, \overline{CS}, CLK, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}			2		V
Input Low Voltage	V_{IL}			0.8		V

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, $V_{CC} = V_{DD} = +4.75\text{V}$ to $+5.25\text{V}$, $T_C = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values are at $V_{CC} = V_{DD} = +5\text{V}$ and $T_C = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	Low-current (LC) mode		70	90	mA
		High-current (HC) mode		121	144	
LOGIC INPUTS (DATA, \overline{CS}, CLK, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}		3			V
Input Low Voltage	V_{IL}				0.8	V
Input Current Logic-High	I_{IH}		-1		+1	μA
Input Current Logic-Low	I_{IL}		-1		+1	μA

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+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, $V_{CC} = V_{DD} = +3.0V$ to $+3.6V$, $T_C = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{CC} = V_{DD} = +3.3V$, HC mode with attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^{\circ}C$, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 5, 7)	50		1000	MHz
Small-Signal Gain	G			20		dB
Output Third-Order Intercept Point	OIP3	$P_{OUT} = 0dBm/$ tone, maximum gain setting		38		dBm
Noise Figure	NF	Maximum gain setting		5.6		dB
Total Attenuation Range				31		dB

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, $V_{CC} = V_{DD} = +4.75$ to $+5.25V$, HC mode with attenuator set for maximum gain, $50MHz \leq f_{RF} \leq 1000MHz$, $T_C = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{CC} = V_{DD} = +5.0V$, HC mode, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^{\circ}C$, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 5, 7)	50		1000	MHz
Small-Signal Gain	G	200MHz		20.5		dB
		350MHz, $T_C = +25^{\circ}C$	18.6	19.9	21.1	
		450MHz		19.5		
		750MHz		18.1		
		900MHz		17.4		
Gain Variation vs. Temperature				-0.004		dB/ $^{\circ}C$
Gain Flatness vs. Frequency		Any 100MHz frequency band from 50MHz to 500MHz		0.4		dB
Noise Figure	NF	200MHz		5.2		dB
		350MHz, $T_C = +25^{\circ}C$ (Note 5)		5.5	6.6	
		450MHz		5.6		
		750MHz		6.2		
		900MHz		6.4		
Total Attenuation Range				31		dB
Output Second-Order Intercept Point	OIP2	$P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz$, $f_1 + f_2$		65		dBm
Output Third-Order Intercept Point	OIP3	$P_{OUT} = 0dBm/$ tone, HC mode, $\Delta f = 1MHz$	200MHz		42.4	dBm
			350MHz		40.4	
			450MHz		39.5	
			750MHz		37.3	
			900MHz		36.2	
		$P_{OUT} = 0dBm/$ tone, LC mode, $\Delta f = 1MHz$	200MHz		40	
			350MHz		38	
			450MHz		37	
			750MHz		35	
			900MHz		33	

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+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(Typical Application Circuit, $V_{CC} = V_{DD} = +4.75$ to $+5.25V$, HC mode with attenuator set for maximum gain, $50MHz \leq f_{RF} \leq 1000MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = V_{DD} = +5.0V$, HC mode, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output -1dB Compression Point	P_{1dB}	$f_{RF} = 350MHz$, $T_C = +25^\circ C$ (Note 5, 8)	17	18.7		dBm
Second Harmonic		$P_{OUT} = +3dBm$, $f_{IN} = 200MHz$, $T_C = +25^\circ C$ (Note 5)	-60	-68		dBc
Third Harmonic		$P_{OUT} = +3dBm$, $f_{IN} = 200MHz$, $T_C = +25^\circ C$ (Note 5)	-72	-88		dBc
Group Delay		Includes EV kit PCB trace delay		0.8		ns
Input Return Loss		50Ω source, maximum gain setting		23		dB
Output Return Loss		50Ω load, maximum gain setting		18		dB
DIGITAL ATTENUATOR						
Insertion Loss				2.5		dB
Input Second-Order Intercept Point	IIP2	$P_{RF1} = 0dBm$, $P_{RF2} = 0dBm$, $\Delta f = 1MHz$, $f_1 + f_2$		52		dBm
Input Third-Order Intercept Point	IIP3	$P_{RF1} = 0dBm$, $P_{RF2} = 0dBm$, $\Delta f = 1MHz$		41		dBm
Attenuation Range				31.2		dB
Step Size				1		dB
Relative Step Accuracy				0.2		dB
Absolute Step Accuracy				0.45		dB
Insertion Phase Step		$f_{RF} = 170MHz$	0dB to 16dB	4.8		degrees
			24dB	8		
			31dB	10.8		
Amplitude Overshoot/Undershoot		Between any two states	ET = 15ns	1.0		dB
			ET = 40ns	0.05		
Switching Speed		RF settled to within $\pm 0.1dB$	31dB to 0dB	25		ns
			0dB to 31dB	21		
Input Return Loss		50Ω source, maximum gain setting		19		dB
Output Return Loss		50Ω load, maximum gain setting		19		dB
SERIAL PERIPHERAL INTERFACE (SPI)						
Maximum Clock Speed	f_{CLK}			20		MHz
Data-to-Clock Setup Time	t_{CS}			2		ns
Data-to-Clock Hold Time	t_{CH}			2.5		ns
Clock-to- \overline{CS} Setup Time	t_{ES}			3		ns
\overline{CS} Positive Pulse Width	t_{EW}			7		ns
\overline{CS} Setup Time	t_{EWS}			3.5		ns
Clock Pulse Width	t_{CW}			5		ns

Note 5: Guaranteed by design and characterization.

Note 6: All limits include external component losses. Output measurements are performed at RF output port of the *Typical Application Circuit*.

Note 7: Operating outside this range is possible, but with degraded performance of some parameters.

Note 8: It is advisable not to continuously operate the VGA RF input above +15dBm.

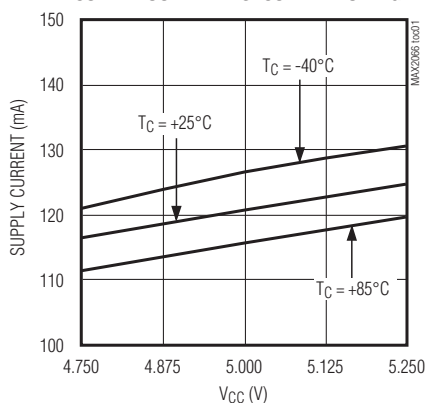
50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

典型工作特性

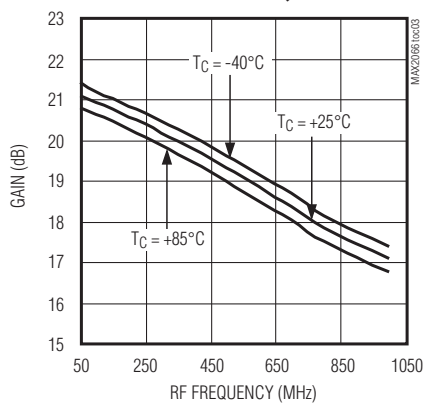
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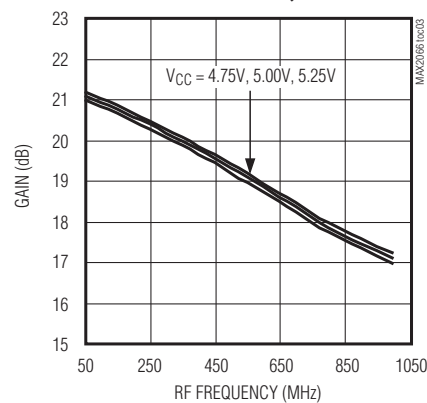
SUPPLY CURRENT vs. SUPPLY VOLTAGE



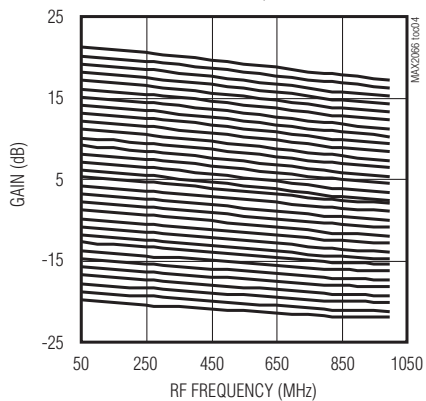
GAIN vs. RF FREQUENCY



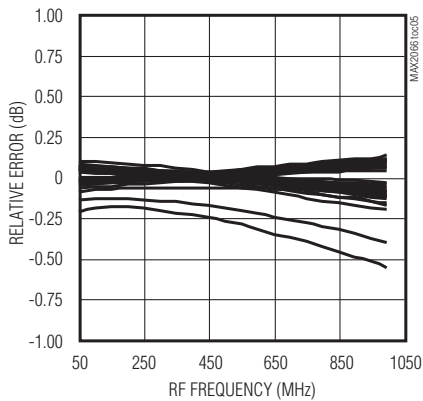
GAIN vs. RF FREQUENCY



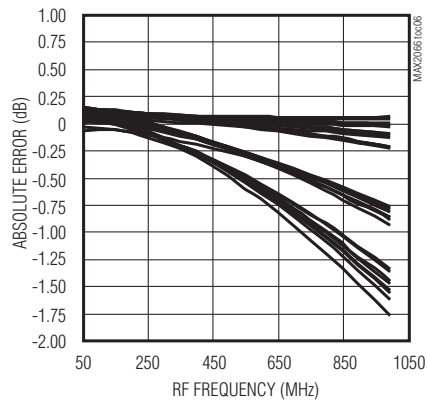
GAIN OVER ATTENUATOR SETTING vs. RF FREQUENCY



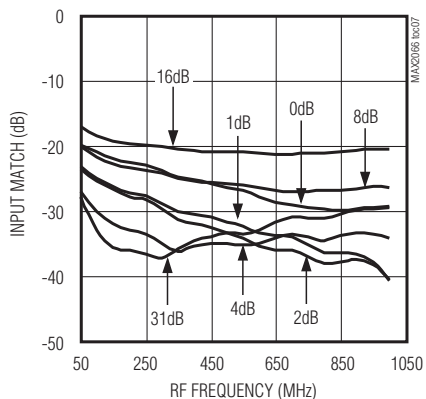
ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY



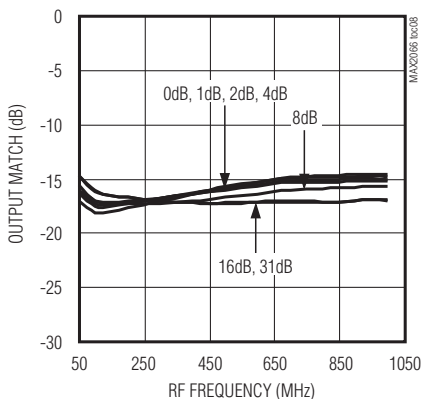
ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY



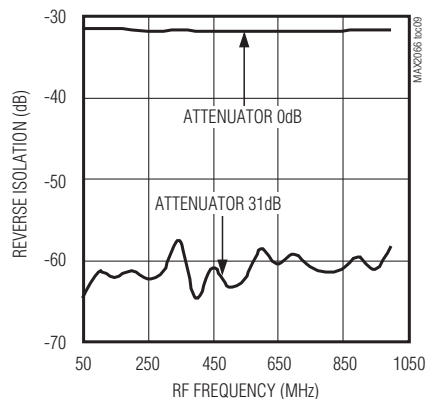
INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



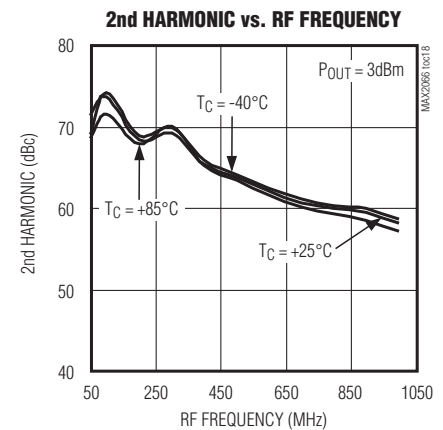
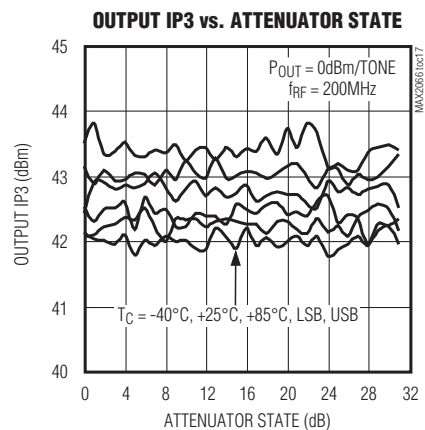
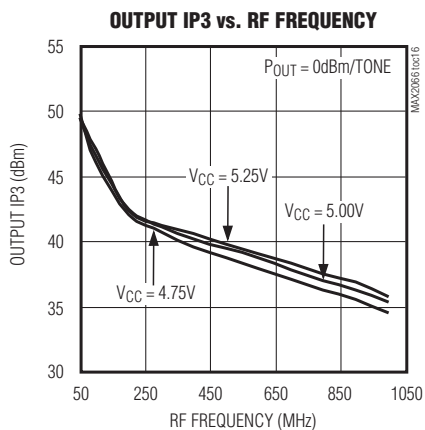
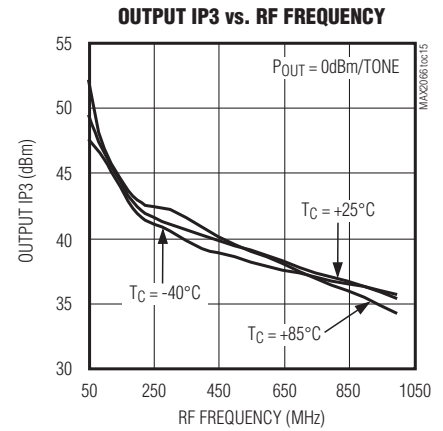
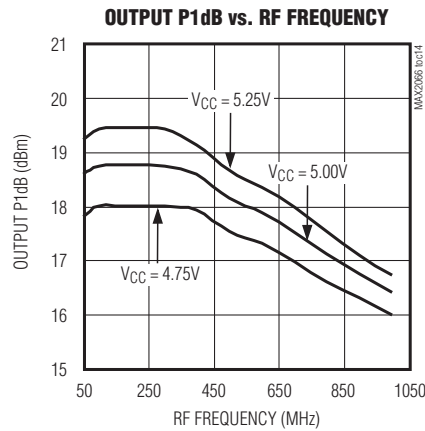
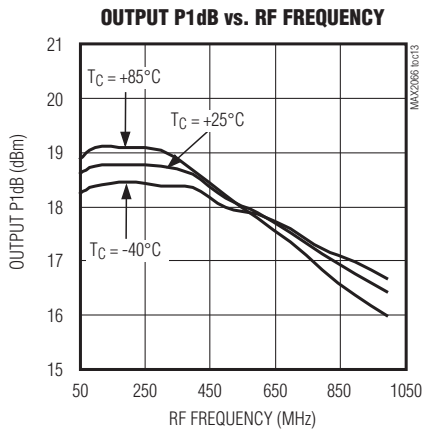
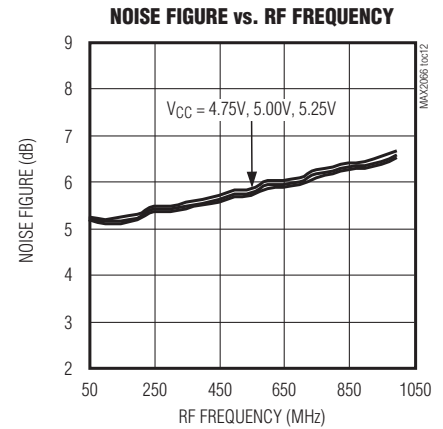
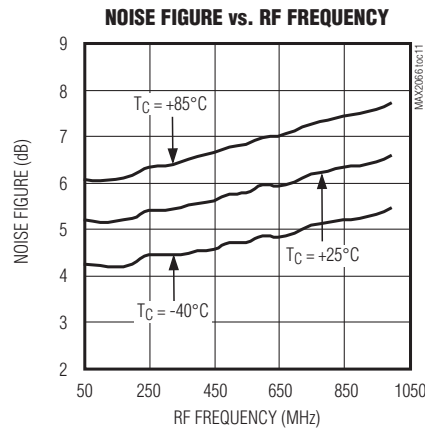
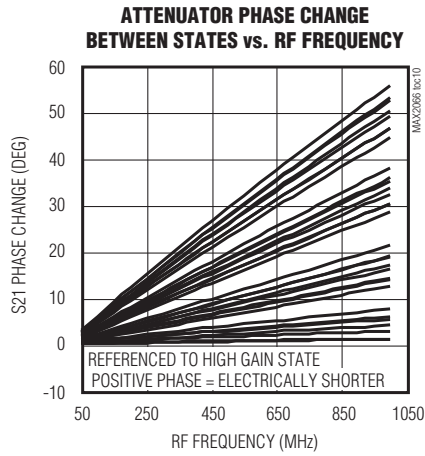
REVERSE ISOLATION OVER ATTENUATOR SETTING vs. RF FREQUENCY



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典型工作特性(续)

($V_{CC} = V_{DD} = +5.0V$, HC mode, digital attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^{\circ}C$, unless otherwise noted.)

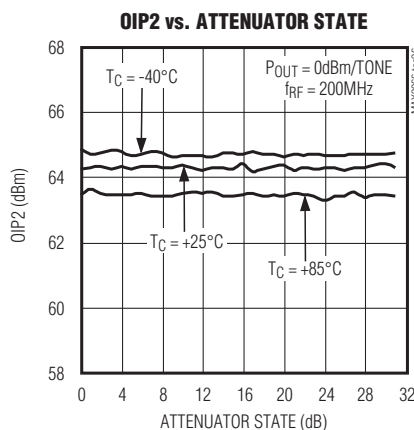
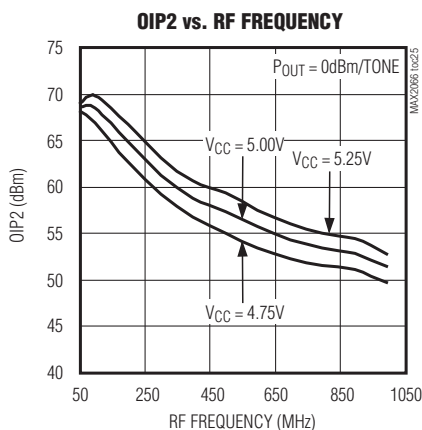
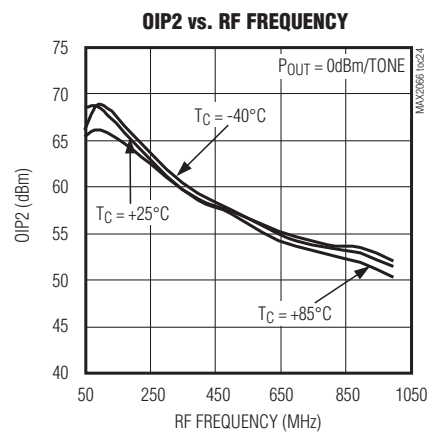
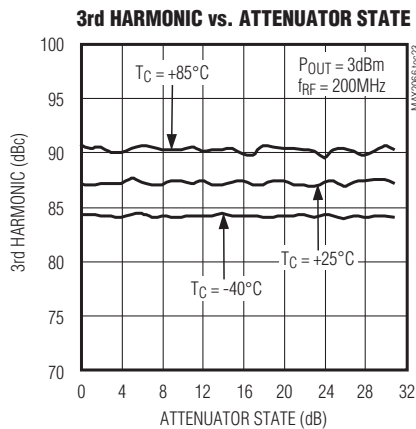
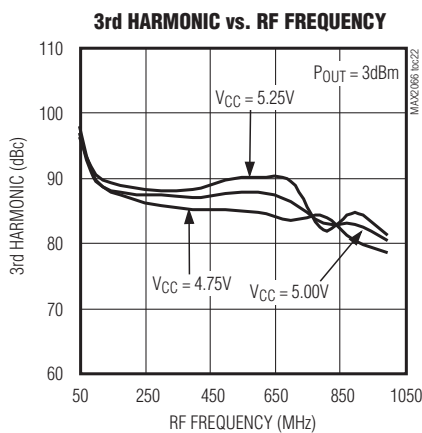
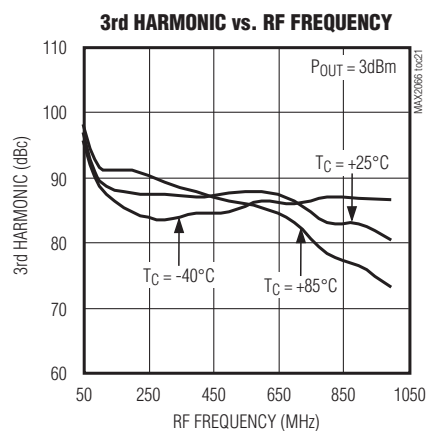
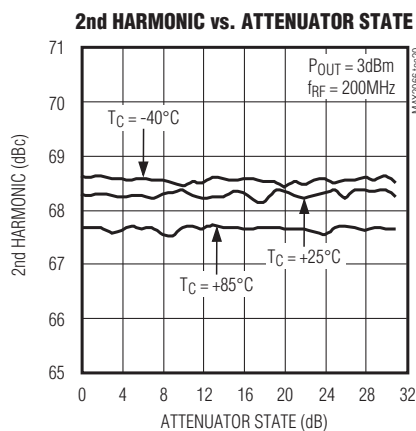
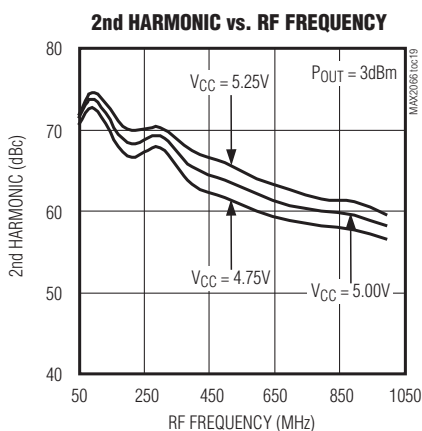


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典型工作特性(续)

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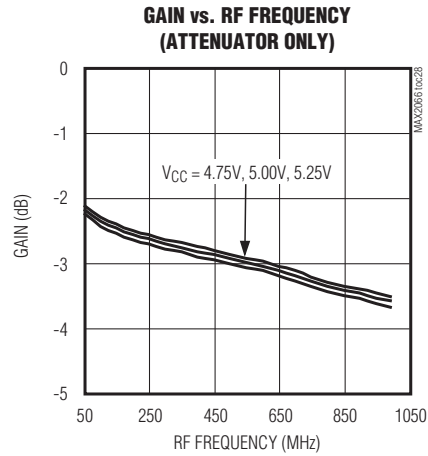
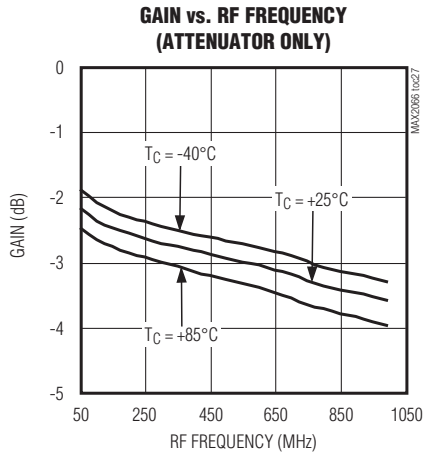
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典型工作特性(续)

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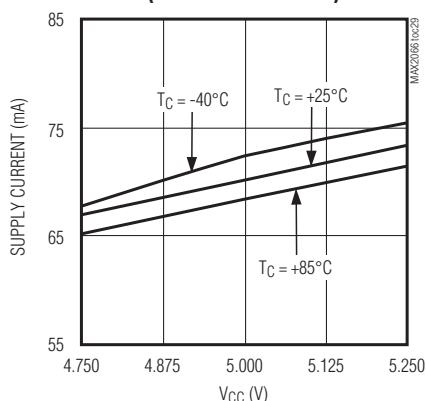
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典型工作特性(续)

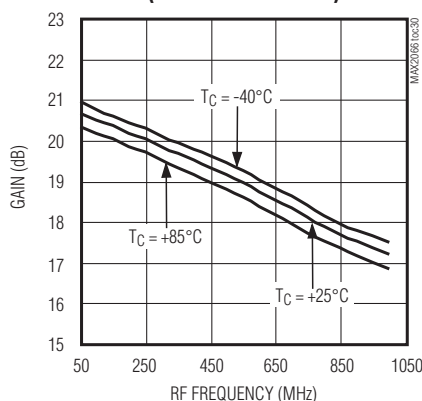
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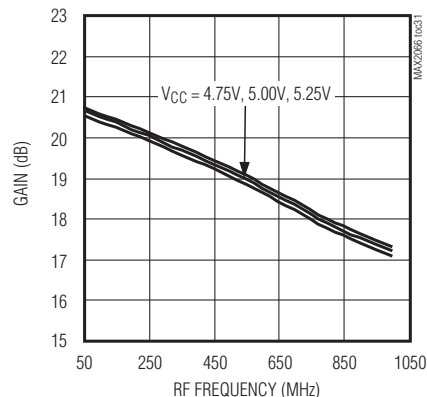
SUPPLY CURRENT vs. SUPPLY VOLTAGE (LOW-CURRENT MODE)



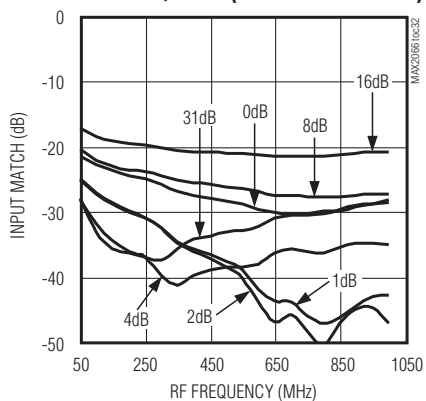
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



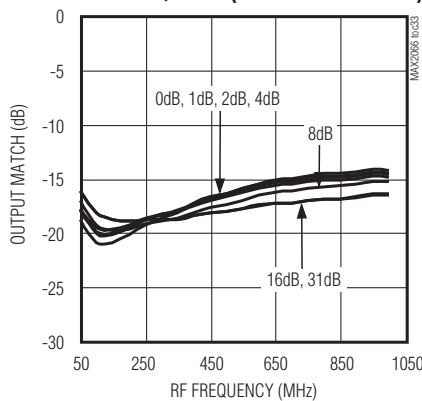
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



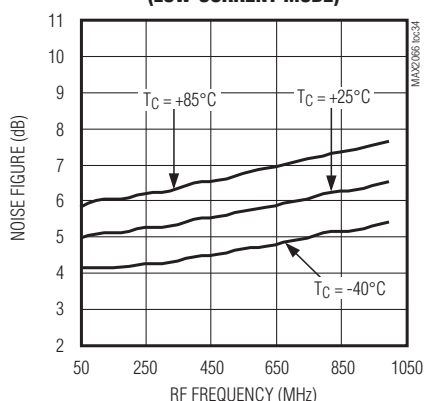
INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY (LOW-CURRENT MODE)



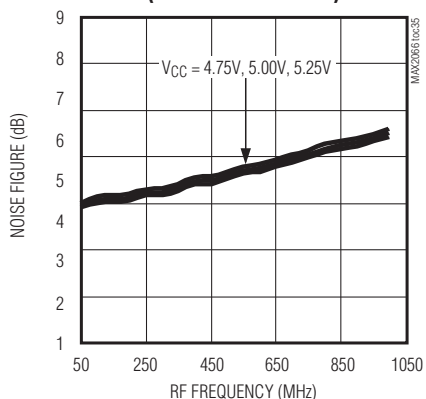
OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY (LOW-CURRENT MODE)



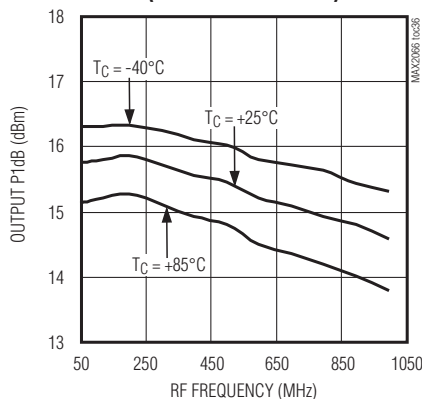
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



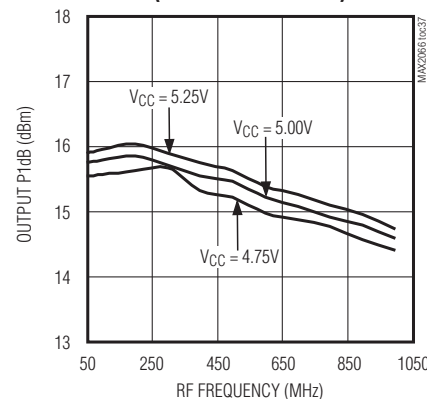
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



OUTPUT P1dB vs. RF FREQUENCY (LOW-CURRENT MODE)



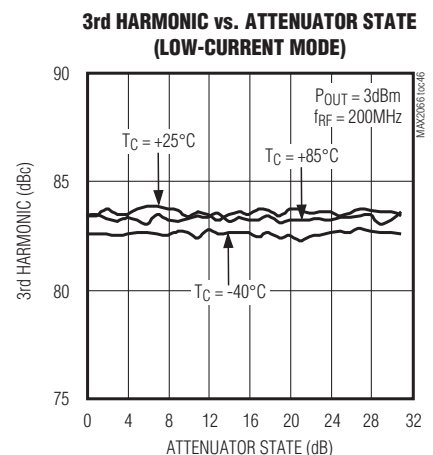
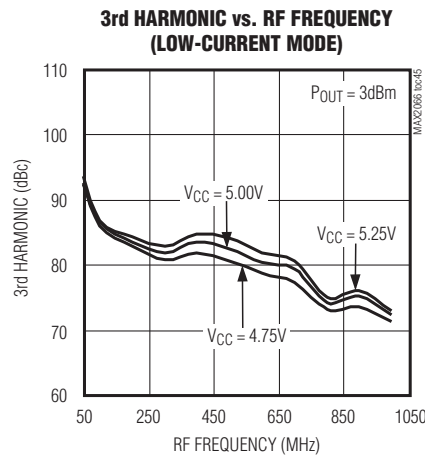
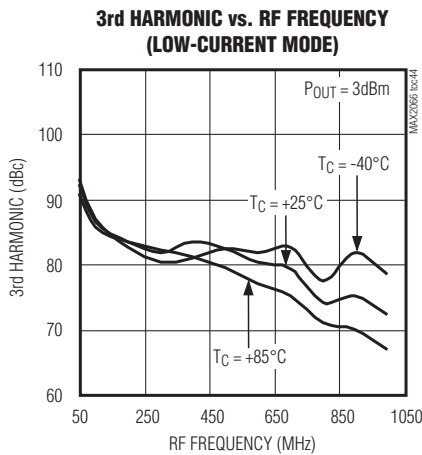
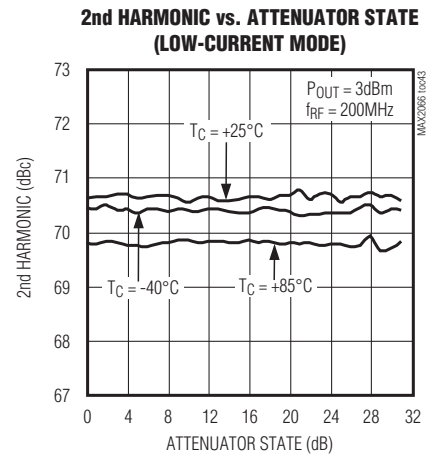
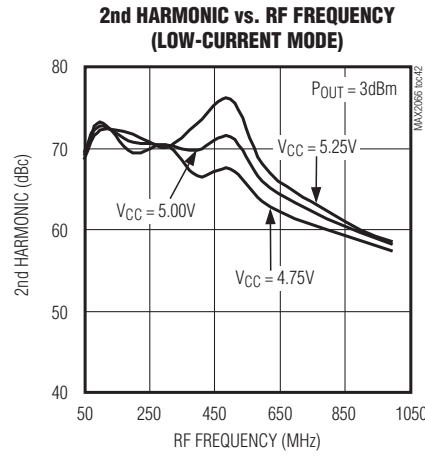
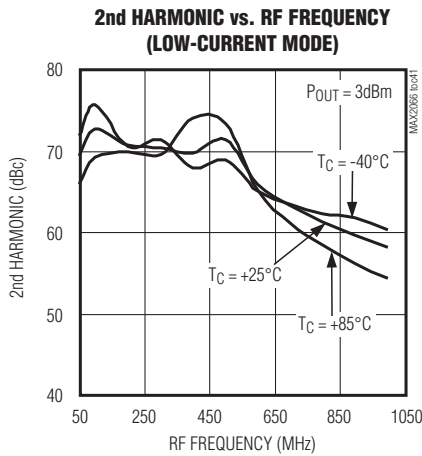
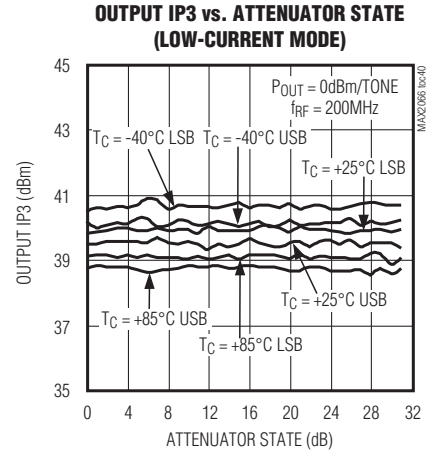
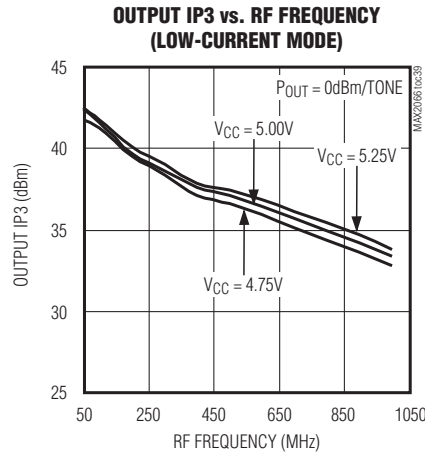
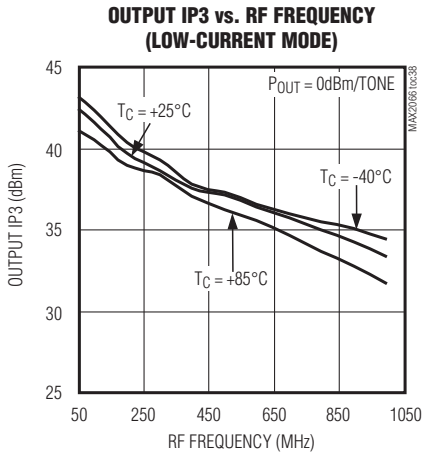
OUTPUT P1dB vs. RF FREQUENCY (LOW-CURRENT MODE)



50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

典型工作特性(续)

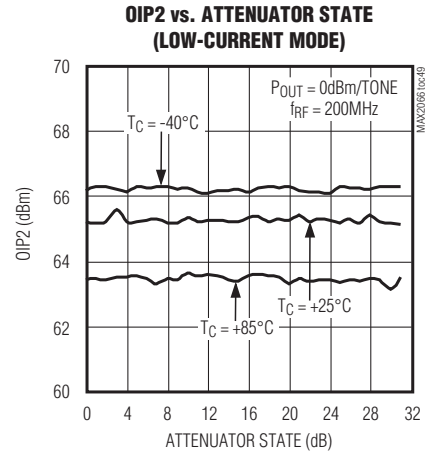
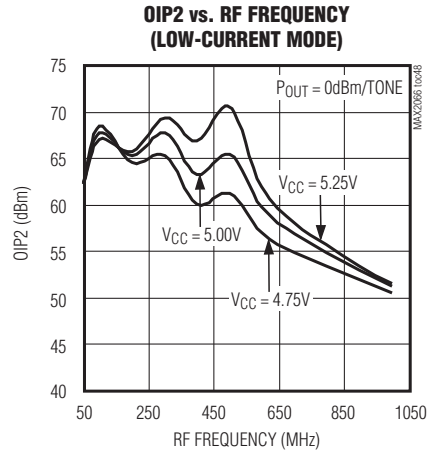
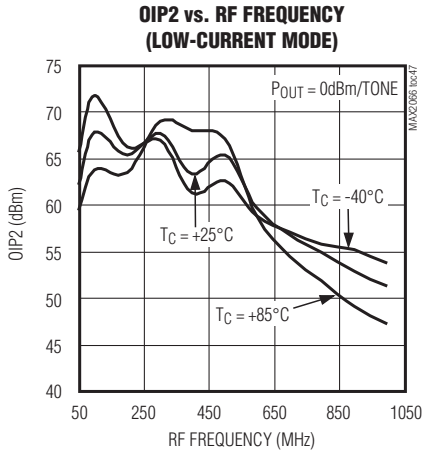
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50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

典型工作特性(续)

($V_{CC} = V_{DD} = +5.0V$, LC mode, digital attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.)

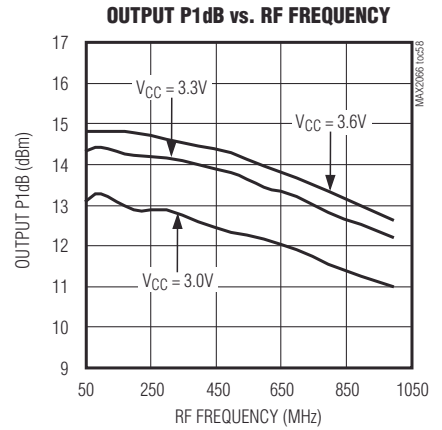
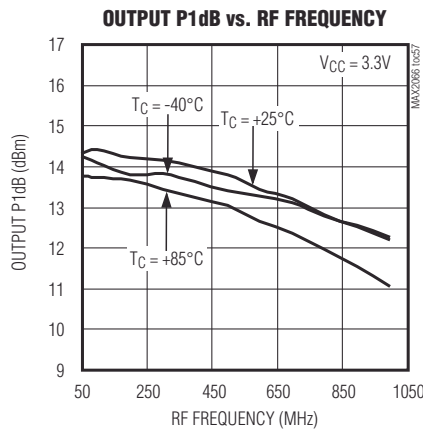
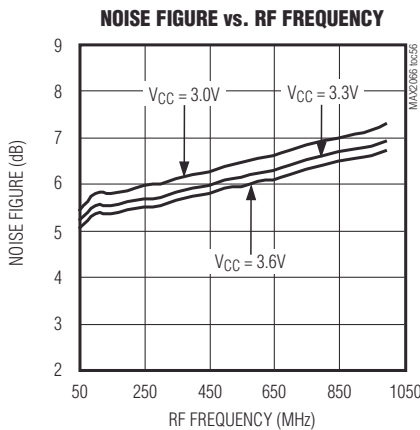
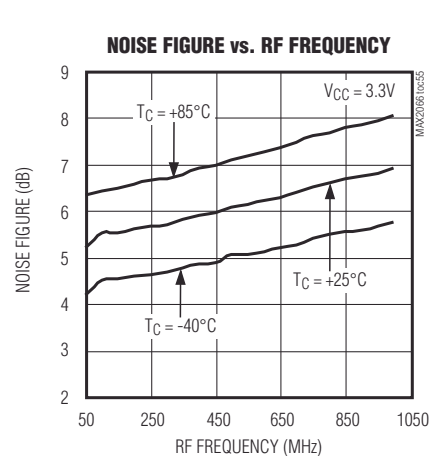
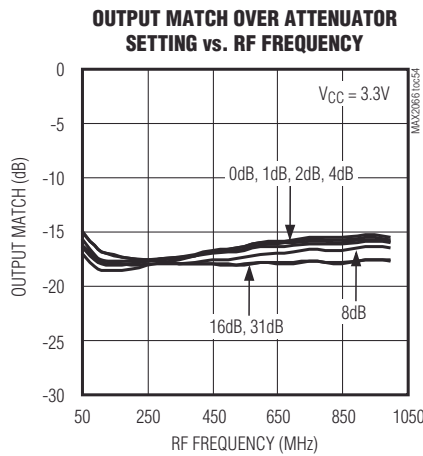
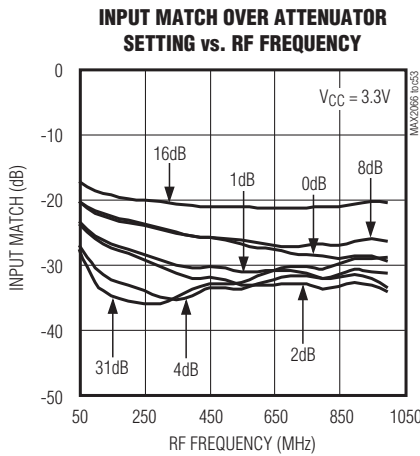
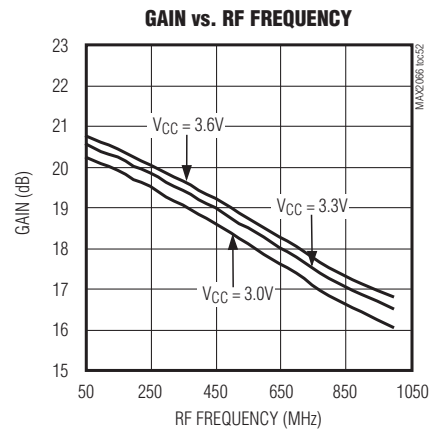
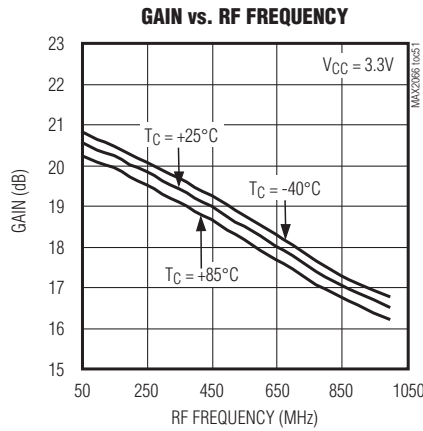
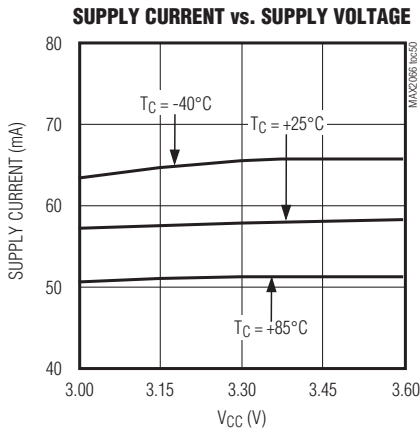


MAX2066

50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

典型工作特性(续)

($V_{CC} = V_{DD} = +3.3V$, HC mode, digital attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.)

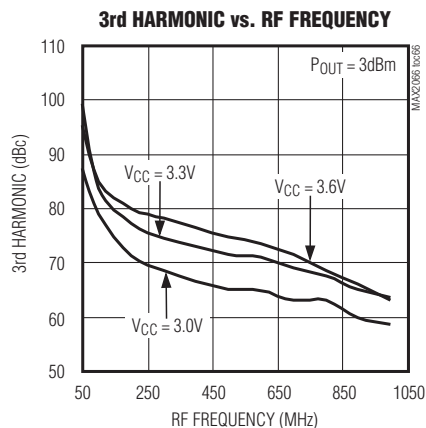
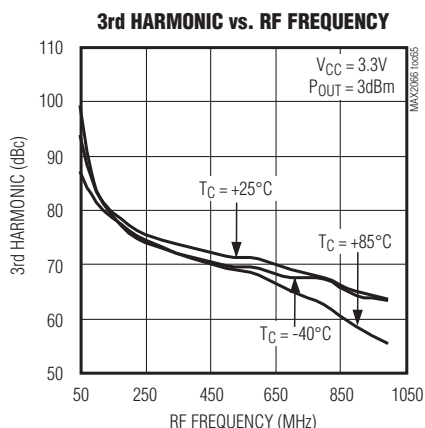
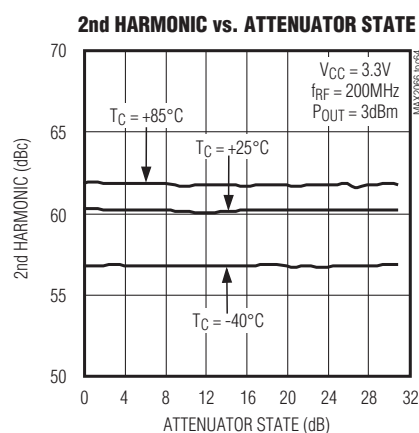
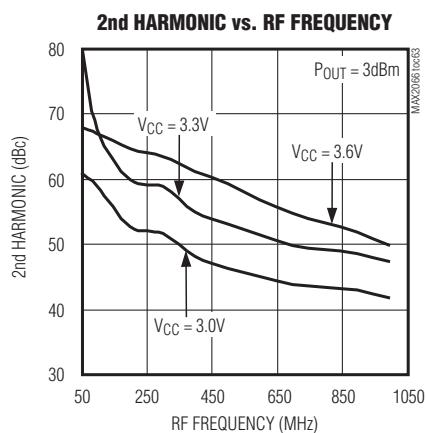
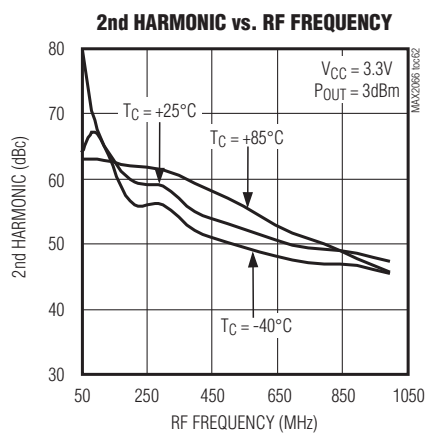
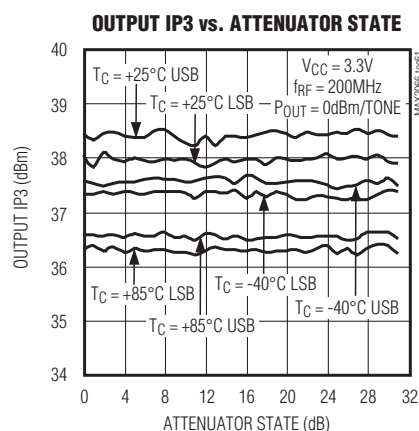
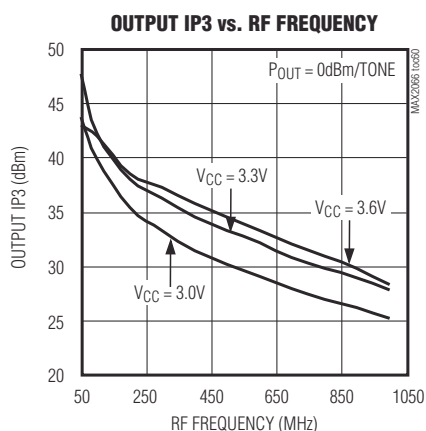
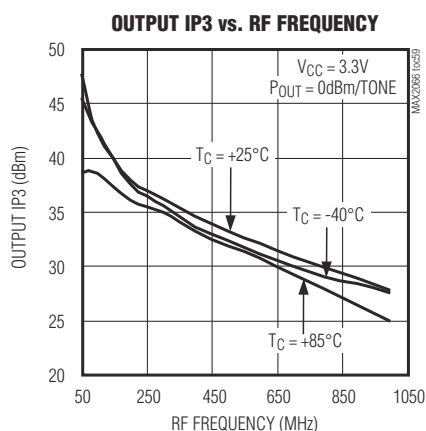


50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

典型工作特性(续)

($V_{CC} = V_{DD} = +3.3V$, HC mode, digital attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.)

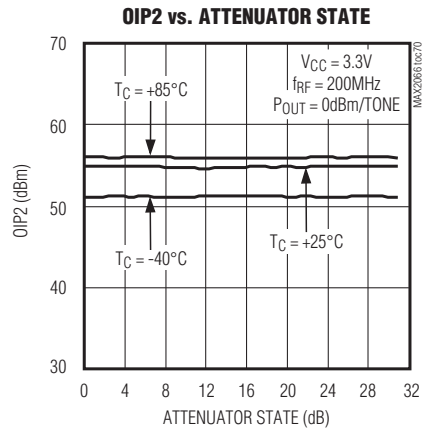
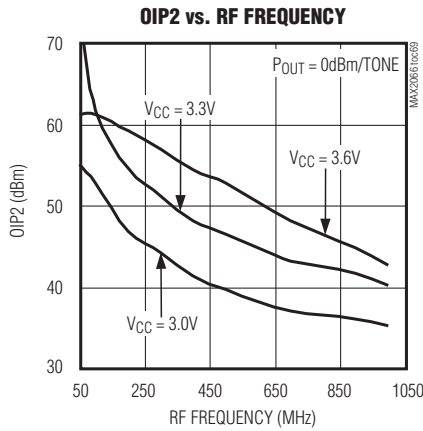
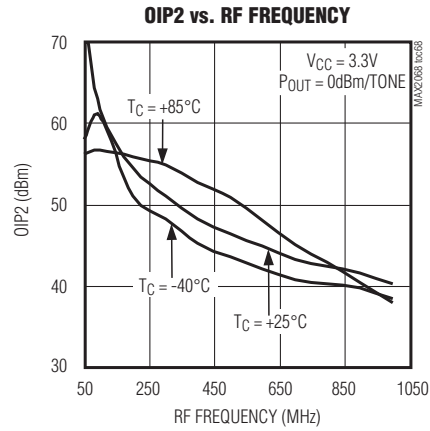
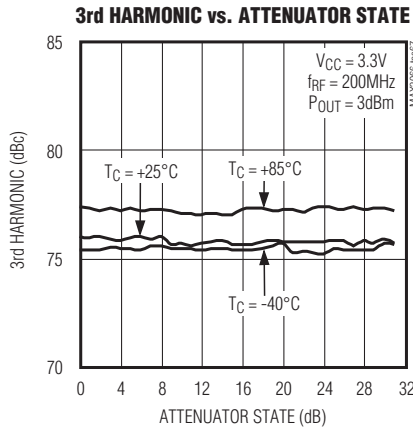
MAX2066



50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

典型工作特性(续)

($V_{CC} = V_{DD} = +3.3V$, HC mode, digital attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.)



50MHz至1000MHz高线性度、 可串行/并行控制的数字VGA

引脚说明

MAXX2066

引脚	名称	功能															
1, 16, 19, 22, 24-28, 30, 31, 33-36	GND	地。															
2, 3, 32, 37-40	GND	地, 请参考引脚兼容性考虑部分。															
4	DATA	SPI数字数据输入。															
5	CLK	SPI数字时钟输入。															
6	\overline{CS}	SPI数字片选输入。															
7	VDD_LOGIC	数字逻辑电路供电输入, 连接到数字逻辑电源, V_{DD} 。在尽可能靠近该引脚的位置安装10nF电容, 将其旁路至GND。															
8	SER/PAR	数字衰减器SPI或并行控制选择输入。逻辑0 = 并行控制; 逻辑1 = 串行控制。															
9	STATE_A	数字衰减器预编程衰减状态逻辑输入。															
10	STATE_B	<table border="0"> <thead> <tr> <th>状态A</th> <th>状态B</th> <th>数字衰减器</th> </tr> </thead> <tbody> <tr> <td>逻辑电平 = 0</td> <td>逻辑电平 = 0</td> <td>预编程状态1</td> </tr> <tr> <td>逻辑电平 = 1</td> <td>逻辑电平 = 0</td> <td>预编程状态2</td> </tr> <tr> <td>逻辑电平 = 0</td> <td>逻辑电平 = 1</td> <td>预编程状态3</td> </tr> <tr> <td>逻辑电平 = 1</td> <td>逻辑电平 = 1</td> <td>预编程状态4</td> </tr> </tbody> </table>	状态A	状态B	数字衰减器	逻辑电平 = 0	逻辑电平 = 0	预编程状态1	逻辑电平 = 1	逻辑电平 = 0	预编程状态2	逻辑电平 = 0	逻辑电平 = 1	预编程状态3	逻辑电平 = 1	逻辑电平 = 1	预编程状态4
状态A	状态B	数字衰减器															
逻辑电平 = 0	逻辑电平 = 0	预编程状态1															
逻辑电平 = 1	逻辑电平 = 0	预编程状态2															
逻辑电平 = 0	逻辑电平 = 1	预编程状态3															
逻辑电平 = 1	逻辑电平 = 1	预编程状态4															
11	D4	16dB衰减器逻辑输入。逻辑0 = 关闭; 逻辑1 = 使能。															
12	D3	8dB衰减器逻辑输入。逻辑0 = 关闭; 逻辑1 = 使能。															
13	D2	4dB衰减器逻辑输入。逻辑0 = 关闭; 逻辑1 = 使能。															
14	D1	2dB衰减器逻辑输入。逻辑0 = 关闭; 逻辑1 = 使能。															
15	D0	1dB衰减器逻辑输入。逻辑0 = 关闭; 逻辑1 = 使能。															
17	AMP_OUT	放大器驱动输出(50 Ω), 详细信息请参考典型应用电路。															
18	RSET	放大器驱动偏置电流设置, 请参考外部偏置部分。															
20	AMP_IN	放大器驱动输入(50 Ω), 详细信息请参考典型应用电路。															
21	VCC_AMP	放大器驱动电源输入, 连接到电源 V_{CC} 。在尽可能靠近该引脚的位置安装1000pF和10nF电容, 将其旁路至GND, 较小容值的电容离器件更近。															
23	ATTEN_OUT	5位数字衰减器输出(50 Ω), 内部匹配至50 Ω 。需外接隔直流电容。															
29	ATTEN_IN	5位数字衰减器输入(50 Ω), 内部匹配至50 Ω 。需外接隔直流电容。															
—	EP	裸焊盘, 内部连接到GND。将EP连接至GND有利于改善RF性能和散热。															

50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

详细说明

MAX2066高线性度、数字可变增益放大器是一款通用的高性能放大器，针对50MHz至1000MHz频率范围、50Ω系统接口的应用而设计。

MAX2066集成了一个数字衰减器，可提供31dB的增益控制，同时可优化放大器驱动设计来提供高增益、高IP₃、低噪声系数和低功耗指标。在对线性度要求不高的应用中，可通过调节外部电阻改变放大器的偏置电流，以进一步降低功耗。

可通过SPI兼容接口控制作为从机外设的数字衰减器；也允许以1dB步长通过并行总线控制，可调节范围为31dB。该器件还增加了“速射”增益选择，直接将增益设置在4种选项(用户可通过SPI接口预先设置)的一种。2个控制引脚允许用户快速选择4种定制衰减的任何一个，无需SPI总线编程。因为每级电路都具有RF输入和RF输出，通过适当配置可以优化NF(第1级为放大器)或OIP₃(最后一级为放大器)。该器件还包含具有22dB增益的放大器(放大器本身)，增益最大时NF为5.2dB(包括衰减器的插入损耗)，并提供+42.4dBm的高OIP₃。这些特性使得MAX2066能够为众多接收器和发射器提供一个理想的VGA。

另外，MAX2066采用+5V单电源供电，提供功能完备的解决方案；工作在+3.3V时，性能指标略有降低，可调节偏置电流在电流损耗和线性度方面进行折衷。

5位数字衰减器控制

MAX2066集成了一个5位数字衰减器，用于实现高动态范围控制。该数字衰减器具有31dB控制范围，1dB步长，并可通过专用的5位并行总线或3线SPI接口设置。请参考应用信息和表1所示衰减器设置，获得更多信息。该衰减器可用于静态和动态功率控制。

驱动放大器

MAX2066包括一个22dB固定增益的高性能驱动器。该驱动放大器优化于50MHz至1000MHz频率范围的高线性度指标。

应用信息

SPI接口和衰减器设置

该数字衰减器可采用5位字节通过3线SPI/MICROWIRE™兼容串行接口进行控制。移入28位数据，MSB在前，并通过CS打包。当CS为低电平时，时钟有效，数据在时钟的上升沿移入。当CS跳变到高电平时，数据被锁存，改变衰减器设置(图1)。表2给出了SPI数据格式的详细信息。

表1. 控制逻辑

SER/PAR	ATTENUATOR
0	Parallel controlled
1	SPI controlled

50MHz至1000MHz高线性度、 可串行/并行控制的数字VGA

MAX2066

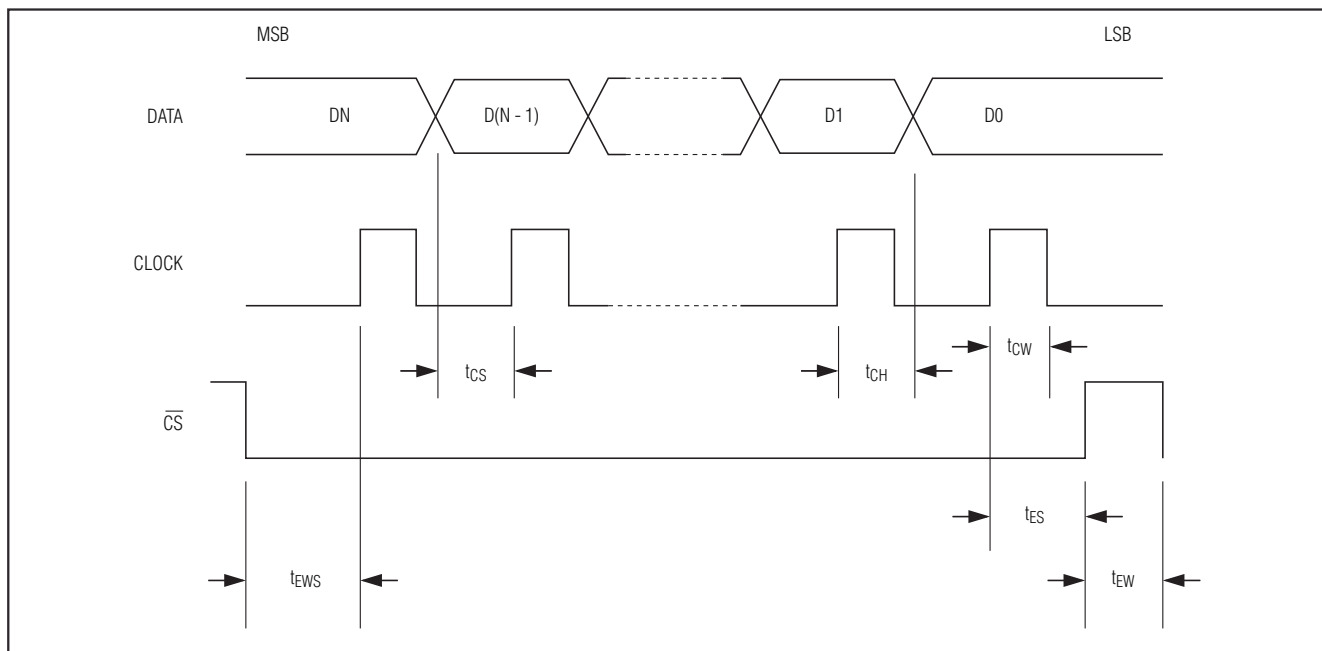


图1. SPI时序图

表2. SPI数据格式

FUNCTION	BIT	DESCRIPTION
Digital Attenuator State 4	D27 (MSB)	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D26	8dB step
	D25	4dB step
	D24	2dB step
	D23	1dB step (LSB)
Digital Attenuator State 3	D22	5-bit word used to program the digital attenuator state 3 (see the description for digital attenuator state 4)
	D21	
	D20	
	D19	
Digital Attenuator State 2	D18	5-bit word used to program the digital attenuator state 2 (see the description for digital attenuator state 4)
	D17	
	D16	
	D15	
Digital Attenuator State 1	D14	5-bit word used to program the digital attenuator state 1 (see the description for digital attenuator state 4)
	D13	
	D12	
	D11	
Digital Attenuator State 0	D10	5-bit word used to program the digital attenuator state 0 (see the description for digital attenuator state 4)
	D9	
	D8	
	D7	

50MHz至1000MHz高线性度、可串行/并行控制的数字VGA

表2. SPI数据格式(续)

FUNCTION	BIT	DESCRIPTION
Reserved	D7	Bits D[7:0] are reserved. Set to logic 0.
	D6	
	D5	
	D4	
	D3	
	D2	
	D1	
	D0 (LSB)	

利用并行控制总线设置数字衰减器

为了达到25ns的快速切换能力，MAX2066提供一个辅助的5位并行控制接口。这些数字逻辑衰减器控制引脚(D0–D4)用于设置衰减器的工作状态(表3)。

直接访问5位总线可以使用户省去SPI接口的编程延时。任何SPI总线的速率都受限于指令逐位传递到外围器件的时间。通过直接访问5位并行接口，用户可以在“快速建立”自动增益控制(AGC)应用中实现数字衰减状态的迅速切换。

“速射”预编程衰减状态

MAX2066能够在4个预置衰减等级之间提供“速射”增益选择。与上述辅助5位总线类似，“速射”增益选择能够快速进入4个预先设定的数字衰减状态的任意一个，消除了通过SPI总线进行设置的相关延时。

这种方式的切换速度与采用辅助5位并行总线的速度相当。但这一特殊功能可以使衰减器的数字控制I/O降低5倍或2.5倍(5个控制位相比于1个或2个控制位)，具体取决于所要求的状态数。

用户可通过STATE_A和STATE_B输入引脚设置所要求的状态(表4)。利用STATE_A引脚(1个控制位)可以得到2个预先设定的衰减状态，同时使用STATE_A和STATE_B引脚(2个控制位)，可以得到4个预先设定的衰减状态。

表3. 数字衰减器设置(并行控制)

INPUT	LOGIC = 0 (OR GROUND)	LOGIC = 1
D0	Disable 1dB attenuator, or when SPI is default programmer	Enable 1dB attenuator
D1	Disable 2dB attenuator, or when SPI is default programmer	Enable 2dB attenuator
D2	Disable 4dB attenuator, or when SPI is default programmer	Enable 4dB attenuator
D3	Disable 8dB attenuator, or when SPI is default programmer	Enable 8dB attenuator
D4	Disable 16dB attenuator, or when SPI is default programmer	Enable 16dB attenuator

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例如，假设AGC应用需要静态调节衰减器，以调整接收器增益。该AGC电路还需要对可能引起接收器灵敏度下降以及ADC过驱动的干扰信号进行动态衰减。该实例中，MAX2066可以预先设置(通过SPI总线) 2种衰减状态：一个状态用于处理静态增益调节，另一个状态用于处理干扰信号。用户只需要对一个I/O引脚(即STATE_A)进行控制，即可在静态和动态衰减控制之间快速切换。

需要时，用户还可以使用第二个I/O引脚，即STATE_B控制引脚，设置另外2个衰减状态。这两个附加的衰减设置非常适合软件定义的无线通信装置，这些装置往往需要多个静态增益设置，以满足不同工作频率的要求；也需要多个动态衰减设置以处理不同阻塞电平(由多个无线通信标准定义)。

外部偏置

驱动放大器偏置电流可通过外部电阻设置并进行优化。将电阻R1和R1A连接到RSET(引脚18)，可以设置放大器的偏置电流。增大外部偏置电阻可降低工作电流，代价是降低系统性能。详细信息请参考表6和表7。

+5V和+3.3V供电

MAX2066的另外一个供电选择是采用+3.3V供电，但在这种情况下系统的线性指标略有下降。

引脚兼容性考虑

MAX2066是MAX2065模拟/数字VGA的简化版本，MAX2066不含模拟衰减器、片上DAC或内部基准。相应的输入/输出引脚在内部接地(表5)。将不使用的输入/输出引脚接地有助于提高隔离度(请参考典型应用电路)。

表4. 预编程衰减状态设置

STATE_A	STATE_B	DIGITAL ATTENUATOR
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

布局考虑

MAX2066经过优化的引脚配置有助于实现紧凑的器件布局和相关分立元件的布局。

MAX2066采用40引脚薄型QFN-EP封装，其裸焊盘(EP)提供了一条到管芯的低热阻通道。安装MAX2066的PCB设计需要利用EP散热，这一点非常关键。另外，EP与电气地的连接需要通过低电感路径。EP必须直接或通过一系列过孔焊接到PCB的地层。

表5. MAX2065/MAX2066的引脚兼容性

PIN	MAX2065	MAX2066
2	VREF_SELECT	GND
3	VDAC_EN	GND
32	ATTEN1_OUT	GND
37	ATTEN1_IN	GND
38	VCC_ANALOG	GND
39	ANALOG_VCTRL	GND
40	VREF_IN	GND

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表6. 典型应用电路元件值(HC模式)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9	1000pF	0402	Murata Mfg. Co., Ltd.	COG ceramic capacitors
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1, R1A	10Ω	0402	Vishay	1%
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2066ETL+

表7. 典型应用电路元件值(LC模式)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9	1000pF	0402	Murata Mfg. Co., Ltd.	COG ceramic capacitors
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1	24Ω	0402	Vishay	1%
R1A	0.01μF	0402	Murata Mfg. Co., Ltd.	X7R
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2066ETL+

过冲幅度衰减

为降低数字衰减器状态变化时产生的过冲，需要在ATTEN_OUT (引脚23)和地之间连接一个带通滤波器(并联LC)。工作在169MHz频率时，推荐使用 $L = 18\text{nH}$ ， $C = 47\text{pF}$ (图2)。关于其它工作频率的推荐元件，请与工厂联系。

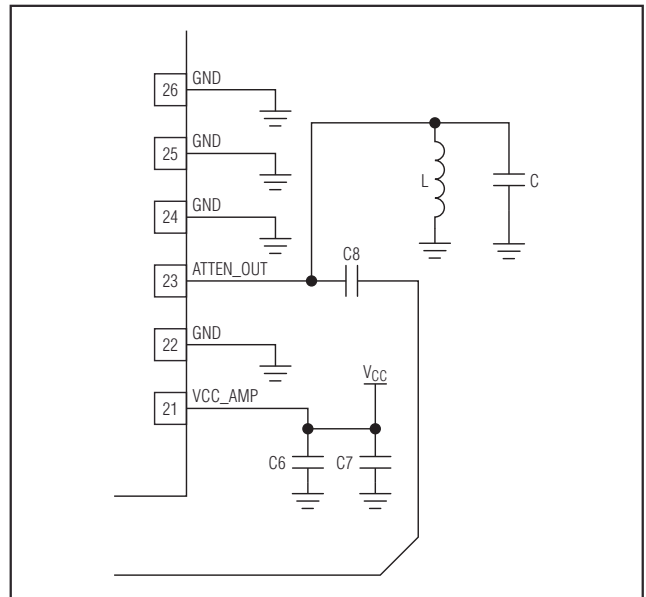
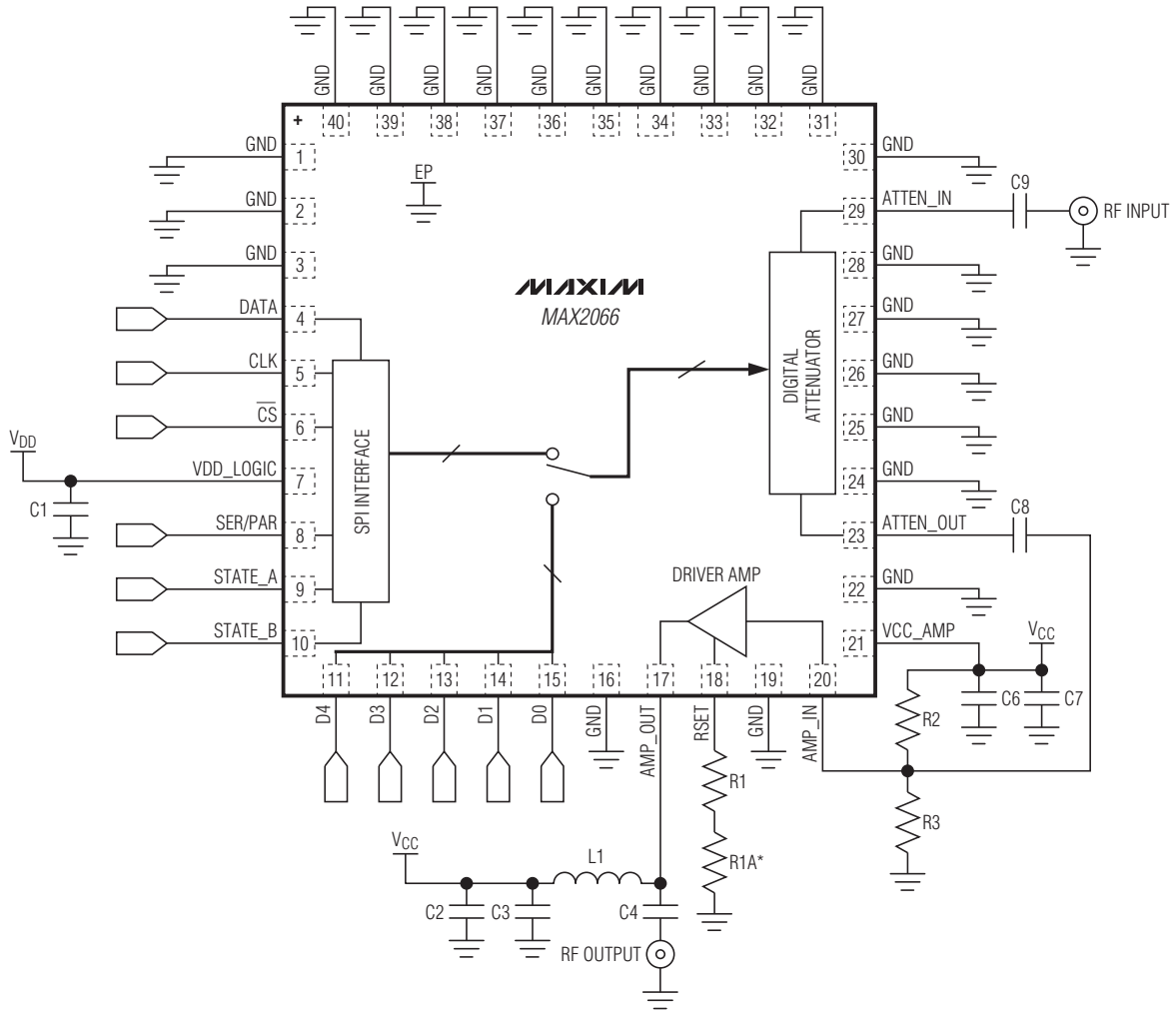


图2. 带通滤波器降低过冲幅度

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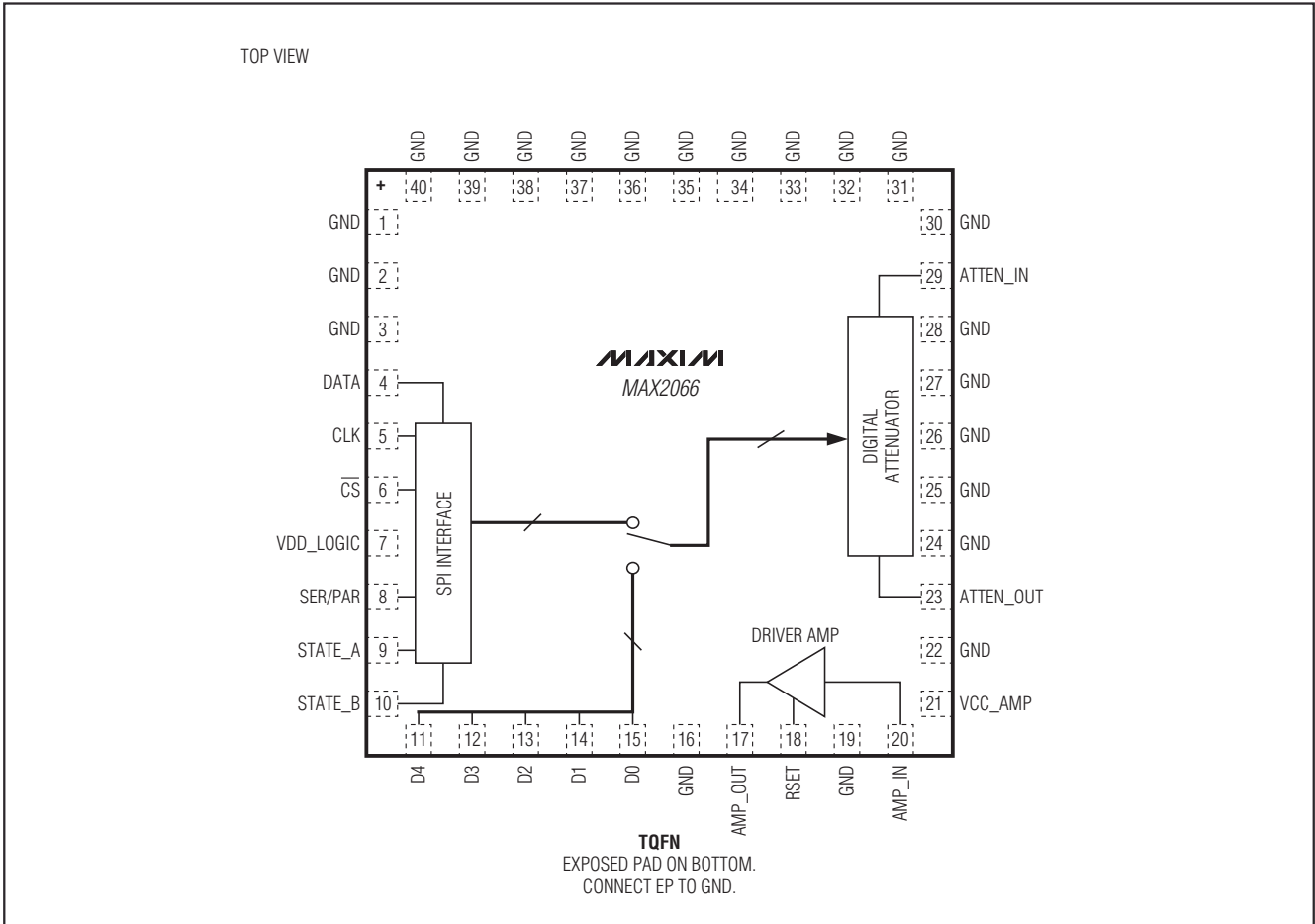
典型应用电路

MAX2066



*IN LC MODE, R1A IS A 0.01 μ F CAPACITOR. SEE TABLE 7 FOR DETAILS.

50MHz至1000MHz高线性度、 可串行/并行控制的数字VGA



芯片信息

PROCESS: SiGe BiCMOS

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MAXX2066

封装信息

(如需最近的封装外形信息，请查询
www.maxim-ic.com.cn/packages。)

封装类型	封装编码	文档编号
40薄型QFN-EP	T4066-3	21-0141

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