ANALOG DEVICES

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APPLICATION NOTE

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ADN2812 Evaluation Board

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INTRODUCTION

This application note describes the use of the EVAL-ADN2812EB. The ADN2812 is a continuous rate clock-recovery, data-retiming device based on a multiloop PLL architecture. The ADN2812 can automatically lock to any data rate from 10 Mbps to 2.7 Gbps, recover the clock, and retime the data without programming and without the need for an external reference clock as an acquisition aid. An I²C® interface is available to access special features of the ADN2812; however, it is not required for normal operation.

The EVAL-ADN2812EB is fabricated using standard FR-4 materials. All high speed differential signal traces are matched to within 3 mils length and maintain a 50 Ω characteristic impedance to preserve signal integrity.

QUICK START GUIDE FOR NORMAL OPERATING MODE (NO REFCLK AND NO I²C PROGRAMMING REQUIRED)

1. Populate jumpers P2 and P3. This disables the SLICE adjust function by tying those pins to GND.
2. Populate jumpers P4 and P6 to tie off the REFCLK inputs. P4 connects REFCLKP to VCC and P6 connects REFCLKN to GND. Note that a reference clock is not required as an acquisition aid for the ADN2812. The device will lock to any rate without the use of any REFCLK.
3. It is unnecessary to make any connections to the I²C interface of the ADN2812 for normal operation.
4. Apply a 3.3 V supply to vector pins VCC and GND, TP5 and TP4, respectively. No supply needs to be connected to I²C_VCC and GND, TP11 and TP10, respectively, for the ADN2812 to operate. Those pins are used in case an external I²C interface requires power to be supplied via the target (the ADN2812 evaluation board).
5. Connect PIN/NIN to a pattern generator that can supply a differential input to the ADN2812. It is important to use cables of matching length.
6. Connect CLKOUTP/N, DATAOUTP/N to measurement equipment using cables of matching length.
7. Apply a single-ended or differential NRZ data pattern to the inputs of the ADN2812. The frequency of the data pattern can be set to any data rate from 10 Mbps to 2.7 Gbps. An amplitude of >100 mV p-p is recommended for initial testing. The recovered clock and retimed data will be present at the CLKOUTP/N and DATAOUTP/N outputs, respectively.

POWER SUPPLY

The ADN2812 evaluation board requires a single 3.3 V nominal supply for basic operation. This supply is brought on board through vector pins VCC (TP5) and GND (TP4)

PIN/NIN INPUTS

PIN/NIN inputs are brought onto the ADN2812 evaluation board through SMA connectors J3 and J4. Capacitors C3, C4 provide ac coupling to the on-chip 50 Ω termination resistors. The capacitors used are 1.5 μF, X7R ceramic chip capacitors. It is recommended that the inputs to the ADN2812 are ac-coupled.

If dc coupling is required, C3 and C4 would need to be replaced with 0 Ω resistors. The common-mode level of the input signal must be greater than 2.3 V and the maximum input level cannot exceed 1 V p-p on either PIN or NIN.

CLOCK/DATA OUTPUTS

The CLKOUTP, CLKOUTN and DATAOUTP, DATAOUTN outputs are CML type outputs. CLKOUTP and CLKOUTN are brought out through 0.1 μF ac coupling caps to SMA connectors J13 and J14, respectively. DATAOUTP and DATAOUTN are brought out through 0.1 μF ac coupling caps to SMA connectors J1 and J2, respectively.

There are 100 Ω resistors to VCC placed at each of the outputs, R1–R4. These are in parallel with on-chip 100 Ω resistors to VCC to provide a 50 Ω near-side termination for the CML outputs.

R10, R11, R16, and R17 are resistive terminations to GND that should not be populated for the CML output version of the ADN2812.

SLICEP/SLICEN

SLICE allows the ADN2812's input quantizer decision level to be adjusted to accommodate amplified spontaneous emission (ASE) in long optical links that use fiber amplifiers. The slicing level can be adjusted by up to ±100 mV by applying a differential input voltage of up to ±1 V to SLICEP/SLICEN.

The SLICEP and SLICEN inputs are brought onto the ADN2812 evaluation board through SMA connectors J6 and J5, respectively. When not being used, the SLICEN/SLICEP inputs should be tied to GND using the jumpers P2 and P3.

LOOP FILTER CAPACITOR

The loop filter capacitor, C_F, is connected between CF1 and CF2, pins 14 and 15. The C_F capacitor needs to be a low leakage, 0.47 μF ceramic chip capacitor, >6.3 V, ±20%. The leakage of the capacitor needs to be <10 nA. If a leakage specification is not available for the capacitor, the leakage can be calculated using the insulation resistance specification. Assuming a max voltage of 3 V across the C_F capacitor, the leakage will be equal to

$$3\ V/I.R.$$

where *I.R.* is the capacitor's insulation resistance.

The capacitor used on the ADN2812 evaluation board is a 0.47 μF ceramic chip capacitor, X7R dielectric, 1G Ω insulation resistance.

LOSS OF SIGNAL DETECTOR

The ADN2812 has an on-chip loss of signal (LOS) detector. The LOS detector detects when the input level drops below a user programmable threshold and asserts an alarm on the SDOUT output pin. The threshold is set by connecting a resistor between the THRADJ pin and VEE. The ADN2812 comes populated with a 10 kΩ THRADJ resistor, R6, which corresponds to a LOS threshold of ~5 mV p-p. If the input level drops below this threshold, the SDOUT pin will be asserted to a logic 1 by default. Writing a 1 to I^2C register bit CTRLC[2] will configure the SDOUT pin to be active low.

There is an LED on the EVAL-ADN2812EB that will turn on when the SDOUT pin signals a loss of signal condition. This is only true if SDOUT is configured to be active high.

LOSS OF LOCK DETECTOR

The ADN2812 has a loss of lock (LOL) detector that signals when the ADN2812 has lost lock. Detailed descriptions of the various modes of operation of the LOL detector can be found in the ADN2812 data sheet. The LOL pin will be asserted to a logic 1 when a loss of lock condition has been detected. There is an LED on the EVAL-ADN2812EB that will turn on when the LOL pin signals a loss of lock condition.

I^2C INTERFACE

The ADN2812 supports a 2-wire, I^2C compatible serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any device connected to the bus. There are two ways to interface to the I^2C. There is a 4-pin header that has the SCK, SDA, I^2C supply, VEE. There is also a Molex 15-83-0064 receptacle available to the user. If the I^2C controller interfacing with the ADN2812 requires that the EVAL-ADN2812EB supply the power, then a power supply can be attached to TP11.

The SCK and SDA pins are open collector outputs that are pulled up to 3.3 V on the EVAL-ADN2812EB with 1.8 kΩ resistors, R9 and R22. The SDA and SCK pins should not be connected to an I^2C controller that has pull-ups to 5 V. This could damage the device.

The slave address of the ADN2812 is a 7-bit word where the MSB, SADDR6 is factory programmed to a 1; SADDR5 can be set to a 1 or a 0 by the SADDR5 jumper on the eval board. SADDR[4...0] are all set to 0 on chip.

Detailed descriptions of the I^2C programmability and functionality can be found in the ADN2812 data sheet.

REFERENCE CLOCK (OPTIONAL)

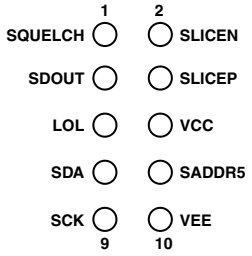
There are two optional uses for a reference clock on the ADN2812. The reference clock can be used to read back the acquired data rate to within 100 ppm, and there is also a lock-to-reference mode where the ADN2812 is programmed to lock to a specific data rate using the reference clock as an acquisition aid. There is a detailed description of the reference clock modes in the ADN2812 data sheet.

The reference clock is brought onto the EVAL-ADN2812EB on J9, REFCLKP and J8, REFCLKN. The ADN2812 reference clock input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (e.g., LVPECL or LVDS) or a standard single-ended low voltageTTL input, providing maximum system flexibility. Phase noise and duty cycle of the reference clock are not critical and 100 ppm accuracy is sufficient. Reference clock frequencies from 10 MHz to 160 MHz are supported.

When the reference clock is not being used, REFCLKP should be tied to VCC with P4 and REFCLKN can be left floating or tied to VEE with jumper P6. If a high speed reference clock is used, a 100 Ω differential characteristic impedance should be maintained. R5 should then be populated with a 100 Ω 0603 chip resistor. The REFCLK PCB traces are 50 Ω transmission lines.

TEST POINTS

Test points are supplied on a 10-pin, 5 × 2 header as follows:



CHOOSING AC COUPLING CAPACITORS

The choice of ac coupling capacitors at the input (PIN, NIN) and output (dataoutp, dataoutn) of the ADN2812 must be chosen such that the device works properly over the full range of data rates used in the application. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander, causing pattern dependent jitter (PDJ).

The user must determine how much droop is tolerable and choose an ac coupling capacitor based on that amount of droop. The amount of PDJ can then be approximated based on the capacitor selection. The actual capacitor value selection may require some trade-offs between droop and PDJ.

Assuming that 2% droop can be tolerated, the maximum differential droop will be 4%. Normalizing to V p-p:

$$Droop = \Delta V = 0.04\ V = 0.5\ V\ p\text{-}p\ (1–e^{t/–\tau})$$

therefore $\tau = 12t$

where:

τ = RC time constant

(C is the ac coupling cap, R = 100 Ω seen by C)

t = total discharge time = nT

n = number of CIDs

T = bit period

The capacitor value can then be calculated by combining the equations for τ and t:

$$C = 12nT/R$$

Once the capacitor value is selected, the PDJ can be approximated as

$$PDJ_{pspp} = 0.5t_r(1–e^{(–nT/RC)})/0.6$$

where:

PDJ_{pspp} = amount of pattern dependent jitter allowed;

< 0.01 UI p-p typical

t_r = rise time = 0.22/BW, where BW ~ 0.7(Bit Rate)

This expression for t_r is accurate only for the inputs; the output rise time for the ADN2812 is ~100 ps regardless of data rate.

The EVAL-ADN2812EB comes populated with 1.5 μF ac coupling capacitors on the inputs and 0.1 μF ac coupling capacitors on the outputs. For lower data rates, e.g., in the tens of MHz, and/or very high numbers of consecutive identical digits, these values may not be optimum.

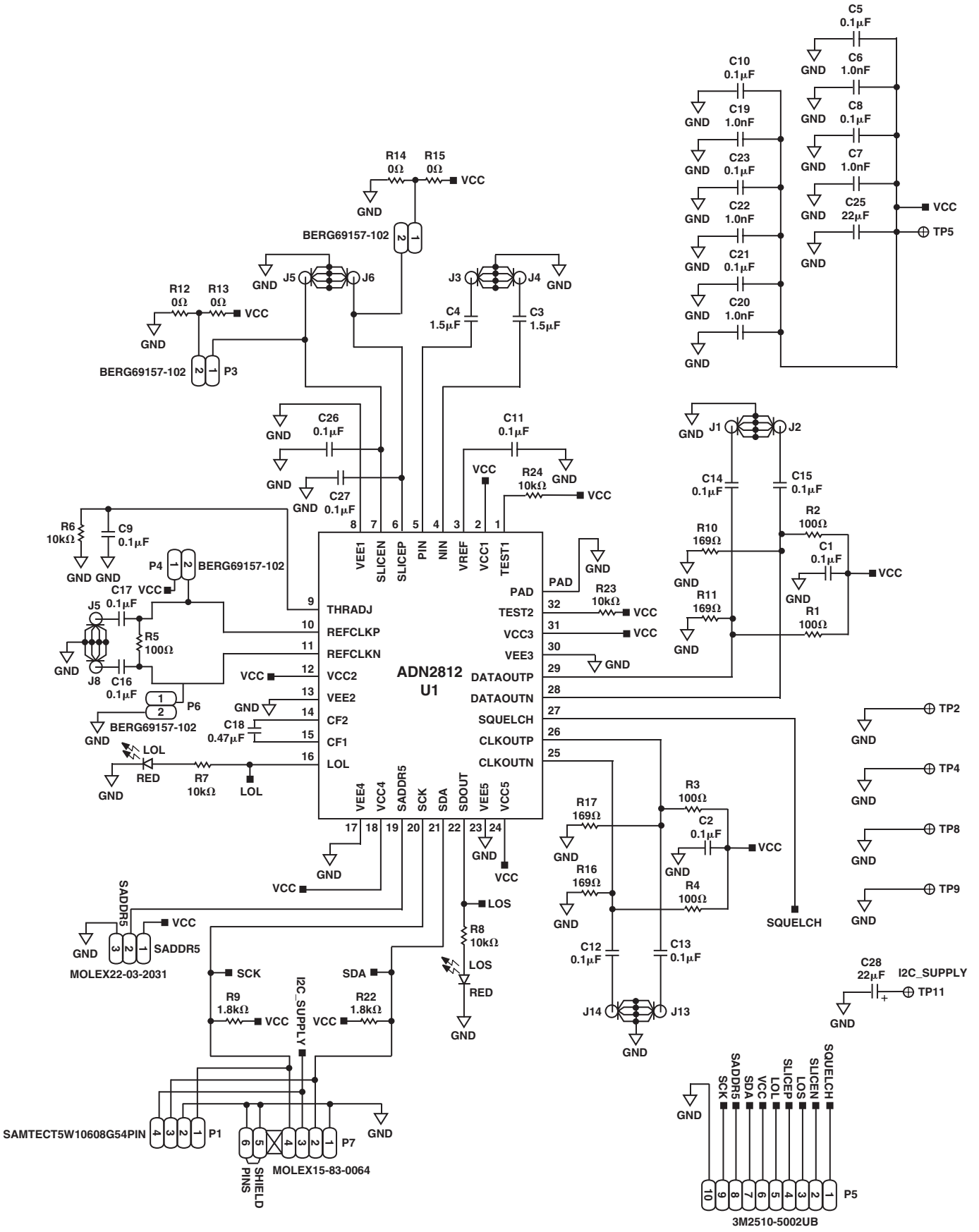


Figure 1. EVAL-ADN2812EB

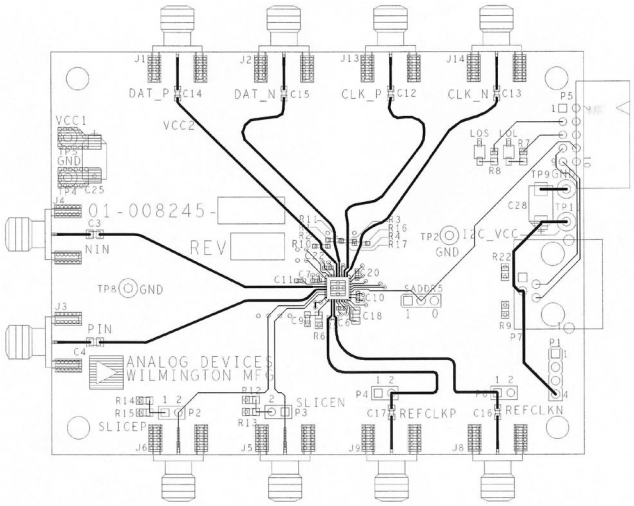


Figure 2. Primary Layer

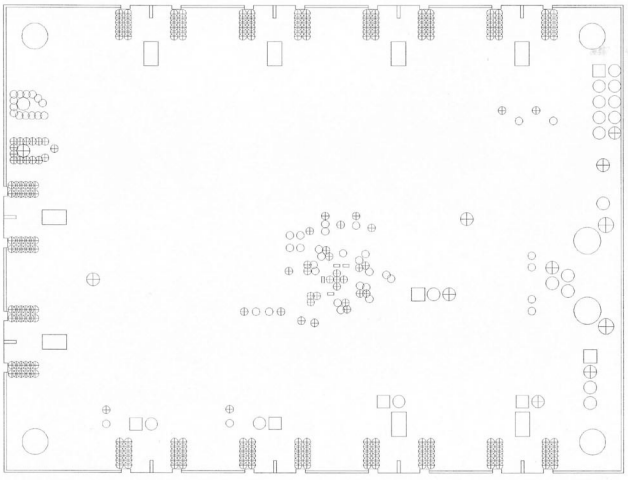


Figure 3. VEE Plane

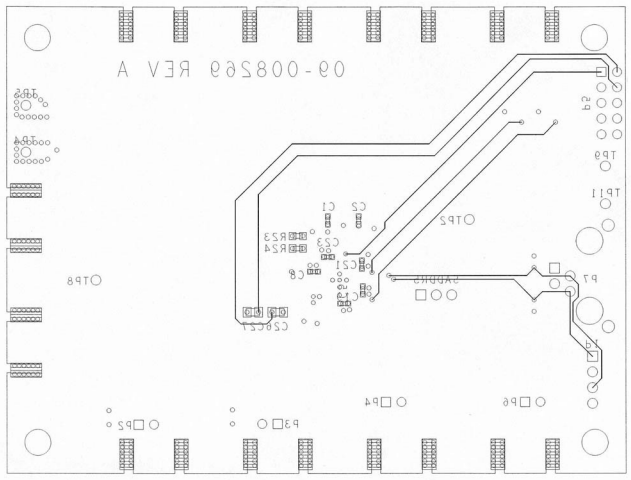


Figure 4. Secondary Layer

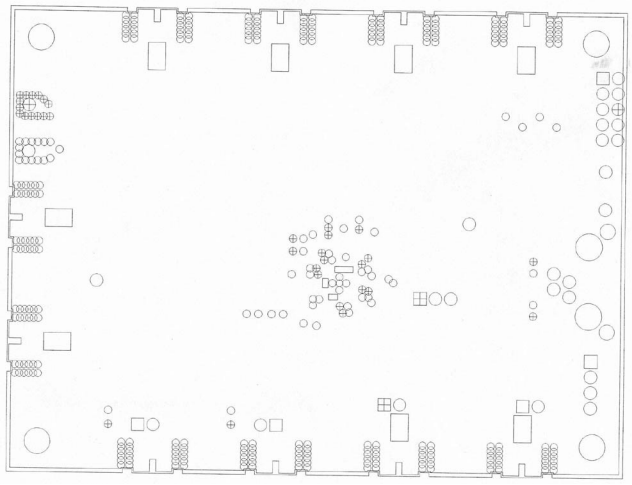


Figure 5. VEE Plane

Table I. Component List

REF. DES.	Manufacturer	Part Number	Value	Description
C1, C2, C5, C8, C11, C19, C21, C23	Yageo American	04022f104Z7B20D	0.1 μF	0.1 μF 16 V Ceramic Y5V 0402
C23, C4	Panasonic	ECJ-2YBOJ155K	1.5 μF	1.5 μF 6 .3 V ±10% Ceramic X5R 0805
C6, C7, C10, C20, C22	Panasonic	ECJ-0EB1E102K	1000 pF	1000 pF 25 V ±10% Ceramic X7R 0402
C9, C12–C17	Panasonic	ECJ-1VB1C104	0.1 μF	0.1 μF 16 V Ceramic X7R 0603
C28	Panasonic	ECJ-2YB1C474K	0.47 μF	0.47 μF 16 V ±10% Ceramic X7R 0805
C25, C28	Panasonic	ECS-H1CD226R	22 μF	22 μF 16 V ±20% Tantalum D Case
C26, C27	Panasonic	ECJ-2VB1E104K	0.1 μF	0.1 μF 25 V Ceramic 0805
J1–J6, J8, J9, J13, J14	Johnson	142-0701-851	0.1 μF	SMA PC Mount End Launch
P7	Molex	15-83-0064	0.1 μF	Receptical
LOL, LOS	Chicago Mini Lamp	CMD28-21SRC/TR8/T1	LED	LED Red Clear LC Gull Wing SMD
R1–R5	Panasonic	ERJ-2GEJ101X	100 kΩ	100 Ω 1/16 W 0402 Chip Resistor
R6–R8	Panasonic	ERA-6YEB103V	10 kΩ	10 kΩ 1/10 W 0805 Chip Resistor
R9, R22	Panasonic	ERA-6YEB182V	1.8 kΩ	1.8 kΩ 1/10 W 0805 Chip Resistor
R12, R14	Panasonic	ERJ-6GEY0R00V	0 kΩ	0 Ω 1/10 W 0805 Chip Resistor
R23, R24	Panasonic	ERJ-3EKF1002V	10 kΩ	10 kΩ 1/16 W 0603 Chip Resistor

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