A System Solution for IEDs Based on IEC 61850

Smart Grid and IED
A smart grid is an electrical grid that uses information and communications technology to gather and act on information, such as information about the behaviors of suppliers and consumers, in an automated fashion to improve the efficiency, reliability, economics, and sustainability of the production and distribution of electricity. The intelligent electronic device (IED) is a basic element of the smart grid, delivering the sensing, measurement, protection, and control functionality required by the system.

Digital Substation and IEC 61850 Standard
A smart grid in a power transmission and distribution system means power automation and substation digitalization plays a major role in this. Modern digital power substation designs now favor IEC 61850 as a means of tying the system together.

All the IEDs will communicate with each other based on the IEC 61850 standard. IEC 61850 features include: data modeling, reporting schemes, fast transfer of events (GOOSE and GSSE), setting groups, digital sampling data transfer (SV), commands configuration, and data storage.

Main Challenges and IED Design Considerations

Complicated Communication Protocol and Multiple Communication Stacks
There are several different protocols that can be mapped to the IEC 61850. An MMS stack based on TCP/IP is used to handle the server-client type communication, which is very complicated but general has low real-time requirement; GOOSE, which is used for exchanging the substation event information, requires a very low latency; SMV messages should always be real-time and come within a very precise time slot.

Real-Time Signal Processing and System Level Functional Safety
In modern IEDs, like protection relay devices or power quality analyzer, a DFT or FFT based algorithm is widely used to detect the over current fault condition or harmonic content. In some extreme cases, the IEDs designer wants a processor to handle more than 60 channels of FFT in just several hundred microsecond. Combined with the complicated communication tasks required by IEC 61850, the IED designers start to realize that a single core processor is now reaching its limitation.

On the other hand, the power line protection devices should never fail even if something abnormal happens on the communication network. Driven by both requirements above, IED designers are now using at least two processors for separation of signal processing and communication tasks. Now, the IED designer has to face another question: how do these processors communicate with each other and how efficient is that communication?

Global Synchronization
Digital substations require global level synchronization, which means all of the devices in the substation should be able to align their sampling points with the same time reference. PPS, IRIG-B or IEEE1588, is widely used for the time synchronization. IEEE1588 is based on Ethernet and has very high timing accuracy leading to the probability that it will become a standard timing synchronization protocol in digital substation in the near future.

System Cost and Development Cost
When we are talking about the multiprocessor system, we usually need to consider the following questions: are the processors the same? How will they communicate with each other? Can they share the same system memories and power supply or must they have separated memories and power system for development do we need two development tools, two operation systems?

“Platform” Development
When the system becomes more and more complex, the development cost and time to marketing now become more and more important. Nowadays, most IED design teams are dreaming of a common platform (including hardware and software), which can cover both high end and low end products. The platform (hardware and software) should be easily expanded and upgraded. An operation system like Linux could be welcomed due to its sufficient open resources. However, Linux is not real-time and knowing how to keep real-time performance in a system when using Linux is a serious topic.
**ADI IEC 61850 Demo Design**

A joint project between ADI and DiGiGrid (ADI third party) was started in 2012 to develop a general platform that focuses on digital substation IEDs, which requires IEC 61850.

- Dual core Blackfin® processor — ADSP-BF60x (2 × 500 MHz)
- 4 × Ethernet ports (two on processor with IEEE1588, two on FPGA)
- 16-channel analog input (2 × AD7606)
- 2 × UART (1 × RS-232, 1 × RS-485)
- 128 MB, 16-bit DDR2
- 16 MB NOR + 4 MB SPI + 2 GB NAND Flash
- Cyclone IV FPGA
- Additional I/O board with 11-channel voltage and current transformer and 8 × DI, 8 × DO

**Hardware Consideration of IEC 61850 Demo Design**

Using ADI’s ADSP-BF60x Blackfin Processor

- Powerful 2 × 500 MHz dual core processor (60 × channels, 32 points, 16-bit FFT in 0.17 ms with single core)
- Each core has private 148 kB L1 SRAM
- 128 kB/256 kB L2 SRAM for dual core data exchange
- System crossbar bus system makes concurrent memory and peripheral access possible
- 2 × UART, 1 × CAN, 2 × SPI, 3 × SPORT, 2 × TWI (I²C) and 1 × USB
- Separated DDR bus and system local memory bus make concurrent external memory access possible
- Safety functionality like L2 SRAM ECC, dual watchdog, system protection
- Dual ethernet MAC with IEEE1588v2
One good reason for using ADI’s ADSP-BF60x is because it has dual independent processors inside that can run at up to 500 MHz each. Another good reason is it has two independent Ethernet MACs (two MAC addresses) which make it very suitable for IEC 61850 applications. In this demonstration system, Core 0 runs the $\mu$CLinux operation system which handles non real-time tasks like MMS stacks, LCD and keypads, and other server applications like TFTP. Core 1 runs the sampling tasks and relay protection algorithm (DFT) and can send out GOOSE messages without the intervention of the operation system. The dual cores communicate to each other via L2 on-chip memory, which can run up to 250 MHz to ensure the highest data exchange efficiency.

In some HV IEDs (110 kV and above), there may be a need for more Ethernet ports (dedicated Ethernet port for GOOSE and SMV) and the demo board also offers the possibility to add more Ethernet ports via an FPGA. The communication interface here is important because the bandwidth of this interface determines the real-time performance of SMV message. The ADSP-BF60x has $4 \times$ link port interfaces which offer up to 125 Mb/s each providing sufficient bandwidth to pull in the SMV data real time.

**Other ADI Featured Products in the Demo Board**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Key Features</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Processor</strong></td>
<td>ADSP-BF606/ADSP-BF607 Dual core Blackfin DSP</td>
<td>400 MHz/500 MHz dual core processor, $2 \times$ 148 kB L1 SRAM, 128 kB/256 kB SRAM, system bus crossbar, dual ethernet MAC with IEEE1588</td>
<td>High performance dual core processor with dual IEEE1588 Ethernet</td>
</tr>
<tr>
<td><strong>ADC</strong></td>
<td>AD7606 8-channel, 16-bit simultaneous ADC</td>
<td>True bipolar analog input ranges: $\pm$10 V, $\pm$5 V, single 5 V analog supply, 2.3 V to $+5 \text{ V}_{\text{sup}}$, 1 M$\Omega$ analog input impedance, analog input clamp protection</td>
<td>8-channel simultaneous sampling AFE with single 5 V supply</td>
</tr>
<tr>
<td><strong>Voltage Reference</strong></td>
<td>ADR421B Voltage reference</td>
<td>Initial accuracy $\leq 0.05%$ with drift $\leq 3\text{ ppm}/^\circ\text{C}$, high output current: 10 mA, different output voltage option 2.5 V, low noise (0.1 Hz to 10.0 Hz): 1.75 $\mu$V p-p at 2.5 V output</td>
<td>High performance (3 ppm), high output current: 10 mA</td>
</tr>
<tr>
<td><strong>Amplifier</strong></td>
<td>AD8275 Difference op amp</td>
<td>Fixed gain = 0.2, $+10 \text{ V}$ to $0 \text{ V}$/4 V level translation with single supply, 1 ppm/$^\circ\text{C}$ gain drift, 80 dB CMRR, $+40 \text{ V}$ to $-35 \text{ V}$ 0VP with single 5 V supply, rail-to-rail output</td>
<td>$\pm10 \text{ V}$ to 0/4 V level translation with single 5 V supply, 16-bit ADC driver</td>
</tr>
<tr>
<td>AD8657 Low power high precision dual op amp</td>
<td>Low power (22 $\mu$A), RRIO, low offset voltage (350 $\mu$V max), unity gain stable, dual op amp</td>
<td>Low power, low cost, low offset voltage dual op amp</td>
<td></td>
</tr>
<tr>
<td><strong>Interface</strong></td>
<td>ADM2587E Isolated RS-485/RS-422 transceiver</td>
<td>Half or full duplex, 500 kbps, 5 V or 3.3 V operation, 3 in 1 (power isolation, signal isolation, and RS-485 driver)</td>
<td>RS-485 with integrated isolated dc-to-dc converter, $+15 \text{ kV} / -15 \text{ kV}$ ESD protection</td>
</tr>
</tbody>
</table>
Circuits from the Lab® Reference Circuits

- Layout considerations for an expandable multichannel simultaneous sampling data acquisition system (DAS) based on the AD7606 16-bit, 8-channel DAS (CN0148)—www.analog.com/CN0148
- A low cost, 8-channel, simultaneously sampled, data acquisition system with 84 dB SNR and excellent channel-to-channel matching (CN0175)—www.analog.com/CN0175
- Half-duplex, isolated RS-485 interface (CN0031)—www.analog.com/CN0031
- More reference circuits are available at www.analog.com/circuits

Other Useful Links

- ADSP-BF60x related resources—www.analog.com/BF609
- ADI DSP development environment (CCES)—www.analog.com/adswt-cces
- ADI µCLinux related resources—docs.blackfin.uclinux.org/doku
- DiGiGrid (ADI IEC 61850 third party)—www.digigrid.com.cn/productview.asp?/34

Software Consideration of IEC 61850 Demo Design

- Core 0 runs µCLinux and non real-time tasks like MMS stacks, LCD and keypads, TFTP serve; Ethernet Port 0 is linked to Core 0 (MMS)
- All µCLinux kernels, customized u-boot make files, and µCLinux drivers are given by source code and image
- SISCO-MMS lite stack is ported on µCLinux (SISCO-MMS license is not included in the demo kit and needs to be purchased additionally)
- A simple modeling example shows how to map a basic relay protection function to the related logic device (LD) and logic node (LN)—the example is given in the demo kit with source code
- Core 1 runs real-time tasks (relay protection algorithm, GOOSE publish) without operation system; Ethernet Port 1 is linked to Core 1 (GOOSE)
- Relay protection algorithm is given by source code
- Real-time GOOSE publish is given by assembly source code (need to contact DiGiGrid in case C source code is required)

Part Number | Description | Key Features | Benefit
--- | --- | --- | ---
ADM3053 | Isolated CAN transceiver | Signal and power isolated CAN transceiver, complies with ISO 11898 standard, high speed data rates up to 1 Mbps, 3 in 1 (power isolation, signal isolation, and CAN transceiver) | CAN bus Interface with integrated isolated dc-to-dc

Power Management

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Key Features</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADP7104</td>
<td>LDO</td>
<td>500 mA output current, $V_{out}$ up to 20 V, PSRR performance of 60 dB at 10 kHz when $V_{out} = 3.3$ V, initial accuracy: ±0.8%, reverse current protection</td>
<td>LDO which can be used as the power supply sourced from ac-to-dc to 16 bits above analog system</td>
</tr>
<tr>
<td>ADP2119</td>
<td>Synchronous, step-down dc-to-dc regulators</td>
<td>145 MΩ and 70 MΩ integrated MOSFETs, input voltage range from 2.3 V to 5.5 V, output voltage from 0.6 V to $V_{out}$, continuous output current: 2 A</td>
<td>High efficiency 2 A ac-to-dc regulator with integrated MOSFET</td>
</tr>
<tr>
<td>ADP2384</td>
<td>Synchronous, step-down dc-to-dc regulator</td>
<td>Input voltage: 4.5 V to 20 V, integrated MOSFET: 44 MΩ/11.6 MΩ, continuous output current: 4 A, 180° out-of-phase clock synchronization, very high efficiency</td>
<td>High efficiency 4 A ac-to-dc regulator with integrated MOSFET</td>
</tr>
<tr>
<td>ADM13305</td>
<td>Dual processor power supply supervisors</td>
<td>Dual supervisory circuits with pretrimmed threshold options: 1.8 V, 2.5 V, 3.3 V, and 5 V, watchdog integrated, maximum supply current of 40 µA</td>
<td>Dual processor power supply supervisors with watchdog</td>
</tr>
</tbody>
</table>

Circuits from the Lab® Reference Circuits

- Layout considerations for an expandable multichannel simultaneous sampling data acquisition system (DAS) based on the AD7606 16-bit, 8-channel DAS (CN0148)—www.analog.com/CN0148
- A low cost, 8-channel, simultaneously sampled, data acquisition system with 84 dB SNR and excellent channel-to-channel matching (CN0175)—www.analog.com/CN0175
- Half-duplex, isolated RS-485 interface (CN0031)—www.analog.com/CN0031
- More reference circuits are available at www.analog.com/circuits
If you need more ADI energy applications and products information, please visit: energy.analog.com.

Customer Interaction Center

Technical Hotline 1-800-419-0108 (India)
1-800-225-5234 (Singapore)
0800-055-085 (Taiwan)
82-2-2155-4200 (Korea)

Email cic.asia@analog.com
EngineerZone ez.analog.com
Free Sample www.analog.com/sample