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Project Code: APM_AWG_2018

ADI ARBITRARY WAVEFORM GENERATOR SOLUTIONS

Application Introduction

In analog or analog-to-digital mixed-mode signal processing applications, arbitrary waveform generators (AWGs) are very popular and versatile. For instance, AWGs can generate signals to simulate sensors, such as signal duplication in a car crash test, or generate high speed analog signals to test the functions of a chip. There are many applications that range from a simple sine wave generator to somewhat more sophisticated AM/FM modulated signals, or even more sophisticated QAM modulated signals. ADI's arbitrary waveform generator solutions, which focus on bandwidths below 300 MHz applications, will be introduced below.

Design Difficulties

High Speed and Large Swing

A lot of high speed operation amplifiers are available. However, very few of them can drive large amplitudes, so we have to use some discrete transistors in high speed signal amplification circuits, which drastically increases design difficulty.

Good Flatness Performance

A pass band with insufficient flatness will cause signal distortion. The flatness of a sine wave can be compensated by amplitude in each frequency. However, it is not applicable to arbitrary waveforms. This is why an excellent signal generator's hardware circuits must have outstanding flatness performance.

Low Noise

In order to generate a signal of 1 mV p-p or lower, the signal-to-noise ratio (SNR) is an inevitable issue that needs to be considered in every step of the product design.

Low Jitter Square and Pulse Wave

A pure direct digital synthesis (DDS) architecture can produce jitter up to 1/fsa when it is generating a square wave at a non-fsa/n frequency. Such a jitter is large and visible, usually unacceptable, and must be improved by special methods. Point-by-point waveform generators with variable sample rates don't have this problem.

Jitter Between the Trigger Channel and Analog Channel

Jitters between trigger output and analog output channels are mainly caused by alignment problems between digital and analog signals. The output trigger is a digital signal coming from the FPGA. When it operates at non-fsa/n frequencies, it cannot align with the phase zero-crossing point of the analog signal, thus causing cycle jitter. Jitter between the input trigger and the analog channels is caused by the randomness of the external input trigger. In most cases, the input trigger signal cannot be aligned with the FPGA's main clock, which causes obvious jitter when it is sampled and used to burst an analog signal output.

Phase Alignment Between Two Channels

Theoretically, if the same clock is provided to two digital-to-analog converters (DACs) with careful layout and delay control, the phase synchronization between two channels should be easily achieved; however, there is a delay-locked loop (DLL) in the high speed DAC, and its initial phase may vary after each power-up. For this reason, getting a picosecond-level phase alignment is still a challenging task. With regards to this problem, it is much easier to use a dual-channel DAC, but the channel isolation performance may degrade.

Solution from ADI

System Block Diagram

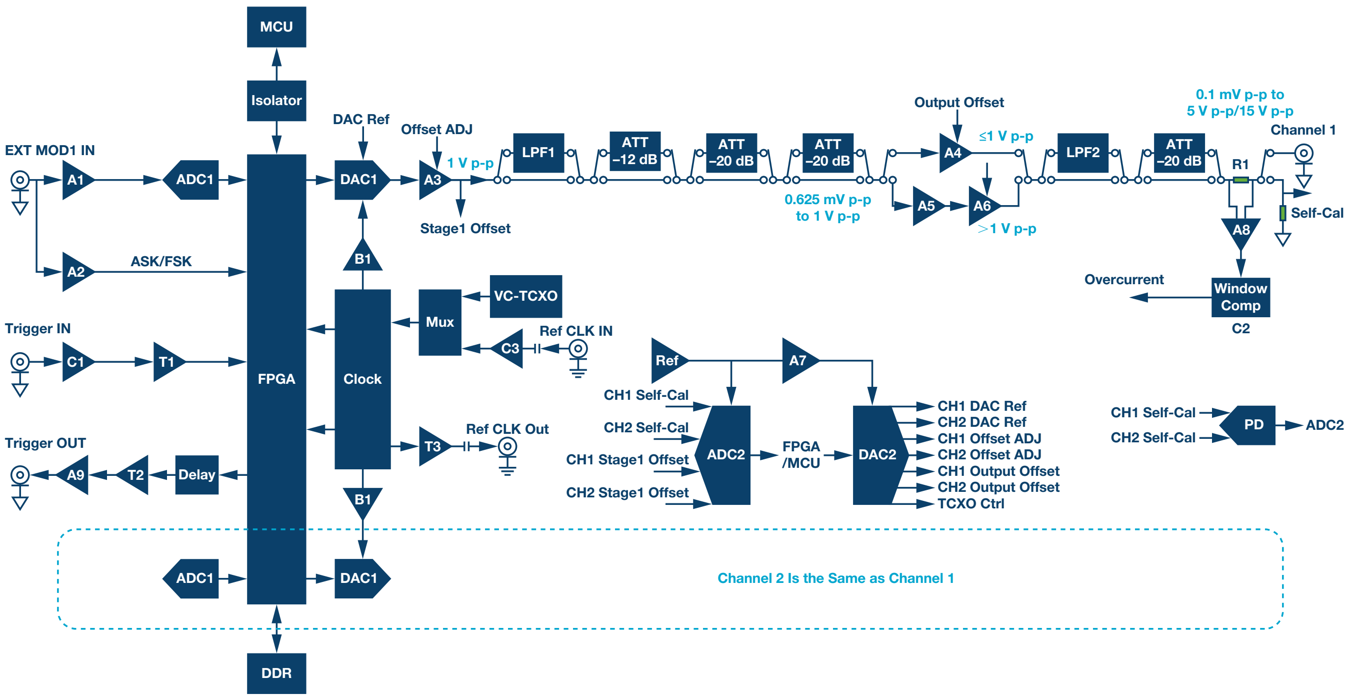

Figure 1. AWG system block diagram.

Figure 1 shows the system block diagram of an arbitrary waveform generator. The following sections will refer to this figure and introduce ADI's overall solution.

MCU	Isolator	Clock	DAC 1	DAC 2
ADSP-BF70x	ADN4651/ADuM14xx	LTC6952/HMC7044	AD9739/AD9739A/LTC2000/LTC2000A/AD9152/AD9121	LTC2666-16/AD5362/AD5676
ADC 1	**ADC 2**	**A1/A7**	**A2**	**A3**
ADAQ7980/AD4000	AD7124-4	AD8672	LT1395	AD8000/ADA4927-1
A4/A5	**A6**	**A8**	**A9**	**PD**
AD8009/AD8000	ADA4870/AD8000	AD8421	LT1397	AD8302
B1	**C1**	**C2**	**C3**	**T1**
ADCLK914/ADCLK905/ADCLK925	CMP401/ADCMP605	CMP401	ADCMP605/ADN4662	ADN4661

T2/T3	Ref
ADN4662	ADR4525/LT6657

Clock Circuits

AWGs usually have requirements for good jitter performance, therefore we recommend ultralow jitter clock generation, such as that found in LTC6952 or HMC7044. Besides providing GHz clocks to the high speed DACs, we also need to provide a 200 MHz to 300 MHz main clock for the FPGA, as well as a 200 MHz to 300 MHz clock for the double data rate (DDR) interface IP in the FPGA. In order to satisfy phase alignment requirements, the ability to support analog delay adjustment in the ps range is necessary. The AWG also has very stringent demands on frequency precision, so a low drift VC-TCXO with temperature compensation should be chosen, while simultaneously requiring a frequency counter to calibrate the 10 MHz reference clock. High speed instruments always have input and output reference clock ports, however, they usually have a long distance from the main clock circuits. If routing is done using single-ended signals, it is usually unmatched impedance that causes crosstalk on the analog signals. Differential signal can be considered to avoid such problems. We recommend using a comparator ADCMP605 as reference clock input, which generates differential output signal. Then, near the clock IC, ADN4662 can be used to convert the differential signal to single-ended signals. The same approach can be applied to the output reference clock. The outputs of HMC7044 are differential, thus only a differential to single-end IC such as ADN4662 is needed near the output port. On the other hand, high speed DACs also have signal integrity and amplitude requirements for their GHz input clocks. Sometimes it may not possible to place the clock IC close to the DAC, and the input impedance may not be 100 Ω. In such cases, it is necessary to place a clock buffer, such as ADCLK905 or ADCLK914, near the DAC to improve signal integrity. ADCLK925 with 1:2 fanout can also be used to distribute the DCO output clock of the dual-channel DACs and sync signals.

Processor and Isolation Interface

If the AWG is designed to provide channels with floating-ground outputs, placing the MCU at the ground (GND) of the chassis can simplify the design of the external interface, such as GPIB/USB/LCD (no isolation required). For example, the recommended MCU ADSP-BF70x has abundant external interfaces and a fast processing speed. An AWG with floating ground output capability is a relatively safe design. Even if the device under test (DUT) is not operating with voltages referenced to the GND, neither the DUT nor the AWG will be damaged. DAC and analog circuits can be powered with floating ground and isolation, thus minimizing the number of interface signals between the FPGA and the MCU. Considering that the FPGA needs to download firmware and other configurations when powering up, the 150 Mbps ADuM14xx can be chosen as the isolation IC. For big data transmission, the 600 Mbps LVDS isolation IC ADN4651 is a good option. Sufficient communication bandwidth is the key to downloading extremely long length waveforms. For example, a 64 MB data point, 14-bit waveform has a data size of around 1024 MB.

Arbitrary Waveform Generation

The most popular AWG consists of an FPGA and DAC based on the DDS architecture. For example, to realize a 2.5 GSPS AWG, it takes 10 sets of DDS running in parallel inside the FPGA, each operating at 250 MHz with each DDS operating at 250 MHz with 36 degrees phase-shift with adjacent DDS. The 10 sets of DDS share the same waveform look up table (LUT). In the end, they serialize their output into two sets of 14 channels, 1.25 Gbps high speed LVDS data streams, and send it to the DAC. In the 2.5 GSPS DAC category, the most popular DAC is AD9739, while LTC2000/LTC2000A also have very good SFDR performance. For dual-channel DACs, the 2.25 GSPS, 16-bit AD9152 is a good option, as well as the 1.23 GSPS, 14-bit AD9121 with outstanding cost-performance balance. Sometimes the dual-channel DAC sharing one data interface I/O only, that will reduce the max data update rate to ½.

The DAC completes data and conversion clock synchronization as well as digital-to-analog conversion. In addition, 3 dB to 6 dB of linear amplitude adjustment can be achieved by adjusting the V_{REF} of the DAC, and along with adjustments of the DAC's internal F_{SC} current, 12 dB of amplitude adjustment range can be achieved without degrading vertical resolution. If a 16-bit DAC is used to adjust V_{REF}, then the amplitude step adjustment capability is usually less than 0.2 mV. Of course, directly adjusting amplitude in digital domain also changes the amplitude, such as only using 13 bits out of 14 bits. This decreases the amplitude by 6 dB, and at the same time also decreases SNR by 6 dB, so it is usually not recommended.

Most high speed DACs' output current signals require an external resistor to convert current to voltage, then amplify the signal with an A3 amplifier, such as the 1.5 GHz bandwidth AD8000. The main purpose of this amplifier is differential to single-end conversion and offset zeroing. It adjusts the signal to a maximum of ±500 mV for output. The first stage of the amplifier can be replaced by ADA4927-1 and AD8000. The advantage of doing so is that the output common voltage of ADA4927-1 can be adjusted to 0 V, which improves the common-mode drift of AD8000's input bias and at the same time enhances the common-mode rejection of AD8000. With ADA4927-1, impedance transformation can be done conveniently to match the output impedance of the DAC. It enhances common-mode rejection and provides low impedance input signals to the next amplifying stages. The AD8000 converts a differential signal to a single-end signal. Its gain can be directly set to 1× to optimize bandwidth. The offset adjustment is used to zero the offset, while the stage 1 offset signal is fed to ADC2 for dc bias calibration. The LPF1 is a low-pass filter normally used for nonsinusoidal waveforms. It is thus designed to have a slow roll-off to preserve more high frequency bands, such as the Bessel filter. Too much high frequency band energy may exceed the frequency response range of the final stage amplifier and cause oscillation. It is therefore necessary to place the low-pass filter in the front to pre-adjust the signal bandwidth. LPF2 is also a low-pass filter that is normally designed for sine waves. Sine waves require lower harmonic distortion, therefore the filter is placed after the final amplifying stage. Usually an elliptical filter with a sharp roll-off is selected. Three pi-type attenuators after LPF1 realize different attenuation levels between 0 dB and 52 dB. They are used to adjust signals with amplitudes between 0.625 mV p-p and 1 V p-p.

To enhance the SNR, we recommend that the final amplifying stage be designed as two separate paths. When the output signal is smaller than 1 V p-p, it can be directly used as an A4 amplifier with 2× gain, such as AD8000 or AD8009. AD8000 is faster, while AD8009 supports a higher slew rate. In this way, small signals will have better SNR than the second path with A5 and A6 amplifiers. Path A5 and A6 are used to drive large output signals greater than 1 V p-p. We can select AD8000 with 3× gain for A5, and AD4870 with 10× gain for A6. The A6 produces an output signal bandwidth under 50 MHz and 15 V p-p (with 50 Ω load). For high speed applications requiring 300 MHz bandwidth, A6 can be replaced by an operational amplifier and a transistor to support a large output swing, such as using an AD8000 and high speed NPN bipolar junction transistor to implement 5 V p-p output. The 20 dB attenuator after LPF2 is designed to enhance SNR for signals less than 10 mV p-p, especially when the signal is used to simulate some sensor outputs. For example, when generating a 1 mV p-p signal, the SNR of directly amplifying a 1 mV p-p signal is definitely worse than generating a 10 mV p-p signal. With the 20 dB attenuator at the end, the 10 mV p-p signal is attenuated to produce a 1 mV p-p output signal, then the noise will also be attenuated, preserving the SNR of the 10 mV p-p signal.

If the customer encounters unintentional accidents, such as connecting the analog output port to a power supply, they will damage the DUT or AWG. Therefore, overcurrent protection circuits must be included to protect against overcurrent in both directions. In this case, a current-sampling resistor, R1, can be used with a value of 0.5 Ω for example, impedance matching will be difficult if R1 is selected too large. The output impedance of A4/A6 needs to be configured to 49.5 Ω to ensure the precision of the dc signal. For A8, we recommend the use of a wideband instrumentation amplifier, AD8421, which has a very good common-mode rejection ratio (CMRR). C2 is a window comparator used to setup the acceptable maximum and minimum currents. CMP401 is recommended. Once overcurrent occurs, the FPGA will be notified to turn off the output relay.

Note 1: Making rising and falling edges like a slope helps to minimize jitters in square/pulse waves. Since it takes two dots to draw a line, it is necessary to ensure that there are at least two points on each edge. In this case, this edges become a real analog signal instead of a digital waveform that switches between 0 and 1. With an external low-pass filter, the jitter can be controlled within a certain range.

Note 2: A tip on the layout of a high speed signal chain—if there is a larger resistance (R) in the high speed circuit, reducing the parasitic capacitance (C) in the surrounding must be considered. Otherwise the low-pass filter formed by RC will severely reduce the signal bandwidth. For example, the feedback resistor of high speed operation amplifiers are usually hundreds of ohms. The ground layer or power layer under this resistor will need to be removed to reduce parasitic capacitance. On the other hand, the thickness of the insulating layers between the high speed signal and the reference layer can be sufficiently increased. The advantages are two-fold: first, the width of the signal traces will be increased accordingly, lowering the difficulty of impedance control process, making it easier to implement 50 Ω/100 Ω configurations. Secondly, increased spacing can reduce parasitic capacitance caused by soldering pads, which can raise the bandwidth and improve frequency response.

Self-Calibration and DC Parameters Configuration

Normally, if the change in room temperature exceeds a certain range, the instrument will need to be recalibrated. ADC2 is used to implement self-calibration. The other end of the last relay in the analog output path can be used for self-calibration, essentially calibrating the signal amplitude and offset at various settings ranges. AD7124-4 is a 24-bit, multi-input channel ADC. It includes an internal PGA and directly supports a ±1.8 V power supply, cancelling the external level-shift amplifier and avoiding errors introduced by external amplifiers. DAC2 is used to configure amplitude adjustment, dc bias adjustment, output current threshold adjustment, and to fine tune VCO control voltage. Usually a 16-bit DAC should be chosen, such as AD5362, LTC2666-16, AD5676, etc. For the reference voltage, we recommend LT6657, which has a low temperature drift coefficient of 1.5 ppm/°C. Also, the self-calibration of ac signals generally indicates a phase alignment between two channels, which can be implemented by a phase detector (PD). We recommend using AD8302, which has 2.7 GHz input bandwidth, 10 mV/°C dc output, and nonlinearity that is less than 1°.

External Modulation Signals

The input of external modulation signals can be roughly divided into two categories. One is for pure analog signals that require sampling by the ADC, such as AM/FM modulation. The other is for pulse signals, which can be sent directly to the FPGA after signal conditioning, such as ASK/FSK modulation. INL/DNL errors are inevitable in the ADC sampling process, therefore we should choose ADCs that are 2 bits higher than the 14-bit analog channel DAC. The ADC also must support real-time sampling requirements, so we recommend a highly integrated SAR ADC, such as ADAQ7980 or AD4000. ADI also provides other ADCs with higher bandwidth, which can be chosen for practical needs. For A2, the current feedback amplifier LT1395, with its high speed current feedback, can be selected to process pulse signals.

Trigger Input and Output

It can be difficult to design the trigger input and trigger output circuits, as there is generally jitter between the trigger input channel and analog output channel. Signals coming in from the trigger input port may be analog, requiring a high speed comparator to convert it into digital levels. For example, the ADCMP605 directly feeds differential output to the FPGA, reducing analog channel crosstalk that arises from lengthy signal routing.

Another trigger output port output digital signal is generated by the FPGA. This signal cannot be phase-synchronized with the zero crossing of the delicate analog output channel, creating relative jitter, but the FPGA operator knows the timing error between the main clock-based output trigger and the zero crossing of the analog channel. By externally controlling a dynamically adjustable delay, the relative jitter can be dynamically cancelled. For T2, ADN4662 performs differential to single-end conversion. For A9, LT1397 is a four-channel, 400 MHz, high speed amplifier. When the four paths amplify in parallel and combine to the same output, the driving capability is improved and a 50 Ω output impedance can be realized.

Power Supply Block Diagram

Figure 2 shows the AWG power supply topology, which essentially uses highly integrated low noise power ICs.

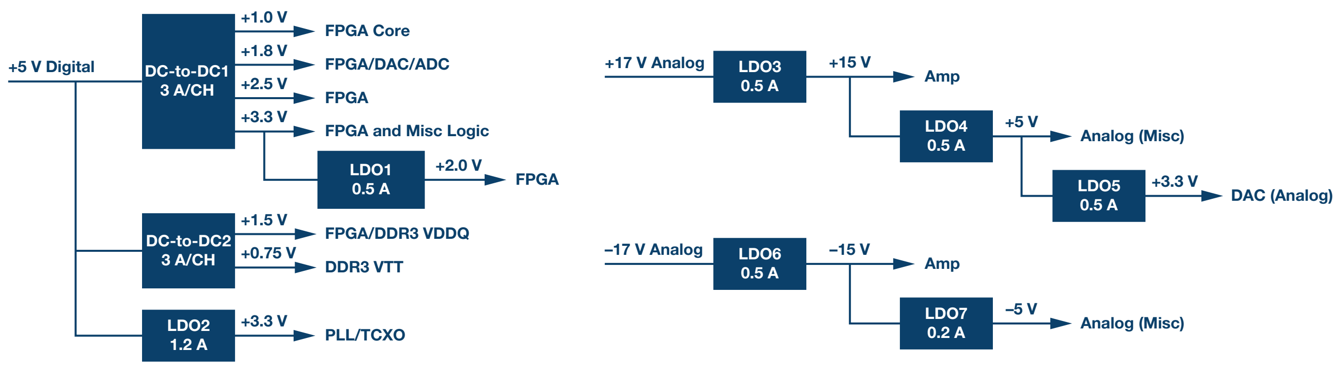

Figure 2. AWG power supply topology.

DC-to-DC1	DC-to-DC2	LDO1/LDO3/LDO4/LDO5	LDO2	LDO6	LDO7
LTM4643/LTM4644	LTC3618	LT3045-1	ADP7157	LT3094	ADP7182

The signal source product requires noise to be as low as possible and the SNR to be as high as possible; however, most power supplies come from ac-to-dc or dc-to-dc power sources, which generate a lot of switching noise and high frequency spurs. Therefore, PSRR is a major concern when choosing a low dropout (LDO) regulator. It is better to choose one that is capable of suppressing wideband noise so that ripples and harmonics from dc-to-dc can be suppressed as much as possible. LT3045-1 is recommended with a PSRR above 50 dB at 10 MHz. For an FPGA that needs larger current and more supply channels, a power module such as LTM4643/LTM4644 is recommended in order to save the layout area and to simplify design complexity. A single chip satisfies most of an FPGA's power needs. A DDR3 has special supply specifications, requiring the use of VTT termination voltage. The LT3618 is one such IC that can satisfy the specific needs of DDR3 chips.

Main Products

Part	Specifications	Usage
DAC		
AD9739/ AD9739A	2.5 GSPS, 14-bit, LVDS interface, SFDR 69.5 dBc at 100 MHz, INL ±1.3 LSB, DNL ±0.8 LSB	Generate high performance arbitrary waveforms
LTC2000/ LTC2000A	2.5 GSPS/2.7 GSPS, 14-/16-bit, LVDS interface, SFDR 76 dBc at 100 MHz, INL ±0.2 LSB, DNL ±0.5 LSB	Generate high performance arbitrary waveforms
AD9152	Dual, 2.25 GSPS, 16-bit, 4 lanes JESD204B interface, SFDR 72 dBc at 150 MHz, INL ±10 LSB, DNL ±5 LSB	High performance and cost-effective arbitrary waveform generator with simplified interface for easy PCB layout
AD9121	Dual, 1.23 GSPS, 14-bit, LVDS interface, SFDR 72 dBc at 70 MHz, INL ±0.5 LSB, DNL ±1 LSB	High performance, cost-effective arbitrary waveform generation
LTC2666-16	8-channel, 16-bit, INL ±2.2 LSB, DNL ±0.2 LSB, ±10 V_{OUT}	Configuration of multiple precision dc parameter in AWG
AD5362	8-channel, 16-bit, INL ±4 LSB max, DNL ±1 LSB max, ±10 V_{OUT}	Configuration of multiple precision dc parameter in AWG
AD5676	8-channel, 16-bit, INL ±1.8 LSB, DNL ±0.7 LSB, 0 V to 5 V_{OUT}	Configuration of multiple precision dc parameter in AWG, requires external level shift operation amplifiers
ADC		
ADAQ7980	SAR ADC, 1 MSPS, 16-bit, SFDR 106 dB at 10 kHz, THD –105 dB, INL ±8 ppm, DNL ±7 ppm, input voltage 0 V to 5 V, integrated ADC driver, ref buffer, and LDO	Highly integrated SAR ADC, suitable for AWG's external modulation signal acquisition, which simplifies design and reduces layout size
AD4000	SAR ADC, 2 MSPS, 16-bit, SFDR 115 dB at 1 kHz, THD –95 dB at 100 kHz, INL ±0.2 LSB, DNL ±0.15 LSB, input voltage 0 V to 5 V, integrated high-Z ADC driver	SAR ADC with higher speed, suitable for acquire AWG's external modulation signals that require higher speed
AD7124-4	4-channel Σ-Δ ADC, max 19.2 kSPS, 24-bit, INL ±1 ppm, input voltage ±2.5 V, integrated mux, PGA, ref buffer, and LDO	Highly integrated 24-bit ADC, good for AWG self-calibration circuit
Clock		
LTC6952	11-channel max 4.5 GHz PLL, low jitter 6 fs rms, –229 dBC/Hz in-band phase noise floor, delay step 11 ps	High performance AWG clock generation, requires an external high frequency VCO
HMC7044	14-channel max 3.2 GHz, low jitter 44 fs rms, phase noise –120 dBc/Hz at 2.4576 GHz with 10 kΩ offset, delay step 25 ps	High performance AWG clock generation
Clock Buffer		
ADCLK914	7.5 GHz clock/data buffer, 100 ps rise/fall, 110 fs jitter, diff output swing >3 V at 2.5 GHz	Improvement of clock signal integrity, increases amplitude
ADCLK925	Dual, 1:2, 7.5 GHz clock/data buffer, 60 ps rise/fall, 60 fs jitter, diff output swing >1.5 V at 2.5 GHz	Improvement of clock signal integrity, provides 1:2 clock fanout
ADCLK905	7.5 GHz clock/data buffer, 60 ps rise/fall, 60 fs jitter, diff output swing >1.5 V at 2.5 GHz	Improvement of clock signal integrity
Isolator		
ADN4651	Dual-channel, 600 Mbps, LVDS isolator, 5 kV rms	Isolation of digital communication interfaces using a floating-ground signal source, suitable for large amounts of data transmission
ADUM14xx	Quad-channel, 150 Mbps, digital isolator, 3.75 kV rms	Isolation of digital communication interfaces for a floating-ground signal source
MCU		
ADSP-BF70x	400 MHz Blackfin+ core, 16-/32-bit, 136 kB L1 SRAM, 256 kB to 1 MB L2 SRAM, on-chip ROM 512 kB, USB 2.0 × 1	Good for embedded systems and applications that require high speed floating-point calculation

Part	Specifications	Usage
Reference		
LT6657-2.5	2.5 V, 1.5 ppm/°C, initial voltage error ±0.1%, noise 0.5 ppm p-p	Low noise, extremely low temperature drift, high precision voltage reference for precision ADC/DAC
ADR4525	2.5 V, 2 ppm/°C, initial voltage error ±0.025%, noise 1.25 µV p-p	Low noise, low temperature drift, high initial precision voltage reference for precision ADC/DAC
Phase Detector		
AD8302	LF~2.7 GHz, nonlinearity <1°, 10 mV/°	Self-calibration of AWG two-channel phase alignment with ps level
Comparator		
CMP401	Quad, 23 ns propagation delay, input range –5 V to +3.9 V, TTL out	Suitable as a window comparator for overcurrent protection circuit
ADCMP605	Single, 1.6 ns propagation delay, input range 0 V to 5.5 V, LVDS out	Suitable for the conversion of external reference clock and input trigger signal
Driver and Receiver		
ADN4661	300 MHz single to differential driver	Single-end to differential conversion for crosstalk reduction
ADN4662	200 MHz differential to single receiver	Differential to single-end conversion for crosstalk reduction
AMP		
AD8000	±6 V, current feedback, 1.5 GHz BW, ±3.9 V swing, slew rate 4.1 kV/µs, 3rd harmonic 79 dBc at 20 MHz, 2 V p-p out, 1.6 nV/$\sqrt{Hz}$	Suitable for high speed signal condition, for the first and second stage amplification
ADA4927-1	±5 V, current feedback differential amp, 2.3 GHz BW, ±3.8 V swing, slew rate 5 kV/µs, 3rd harmonic 98 dBc at 70 MHz, 2 V p-p out, 1.4 nV/$\sqrt{Hz}$	Suitable for high speed signal condition, as the first driver of DAC output
AD8009	±5 V, current feedback, 1 GHz BW, ±3.9 V swing, slew rate 5.5 kV/µs, 3rd harmonic 75 dBc at 20 MHz, 2 V_{P-P} out, 1.9 nV/$\sqrt{Hz}$	Suitable for high speed signal condition, for the first and second stage amplification
ADA4870	±20 V, current feedback, 52 MHz BW, ±18 V swing 1 A out, slew rate 2.5 kV/µs, 3rd harmonic 74 dBc at 1 MHz, 20 V p-p out, 2.1 nV/$\sqrt{Hz}$	Suitable for AWG final stage signal amplification that below 50 MHz
AD8672	Dual, ±15 V, voltage feedback, 10 MHz GBW, input offset voltage 20 µV, offset drift 0.3 µV/°C, 2.8 nV/$\sqrt{Hz}$, output current ±20 mA	Suitable for dc signal fine condition
LT1395	Single, ±6 V, current feedback, 400 MHz BW, input offset voltage 1 mV, offset drift 15 µV/°C, 4.5 nV/$\sqrt{Hz}$, output current ±80 mA	Wideband, good for PWM waveform condition, used for external modulation input
LT1397	Quad, ±6 V, current feedback, 400 MHz BW, input offset voltage 1 mV, offset drift 15 µV/°C, 4.5 nV/$\sqrt{Hz}$, output current ±80 mA	Wideband, good for PWM waveform condition, four channel parallel connection enhances driving capability, suitable for driving trigger output signal
AD8421	±18 V, INST AMP, 10 MHz BW, CMRR 100 dB at 20 kHz G = 10, input offset voltage 25 µV, offset drift 0.2 µV/°C, 3 nV/$\sqrt{Hz}$	Wide bandwidth instrument amplifier, high common-mode rejection, especially suitable for current-to-voltage conversion in AWG's overcurrent protection circuits
Power		
LTM4643/ LTM4644	Quad dc-to-dc module, 4 V to 20 V and 4 V to 14 V_{IN}, 3 A/4 A_{OUT} per channel	Highly integrated power module, no external inductor needed, suitable for supplying large current to multivoltage IC such as FPGA
LTC3618	Dual, 2.25 V to 5.5 V_{IN}, ±3 A out, max 4 MHz	Power supply exclusively for DDR
LT3045-1	LDO, 1.8 V to 20 V_{IN}, 500 mA out, PSRR 76 dB at 1 MHz	Extremely wide PSRR, suitable as power supply for analog circuits such as amplifiers
ADP7157	LDO, 2.3 V to 5.5 V_{IN}, 1.2 A out, PSRR 55 dB at 1 MHz	Low noise, high current LDO, good for PLL/TXCO
LT3094	LDO, –1.8 V to –20 V_{IN}, 500 mA out	High voltage, high PSRR, low noise negative power supply
ADP7182	LDO, –2.7 V to –28 V_{IN}, 200 mA out, PSRR –45 dB at 1 MHz	Negative power supply with wideband PSRR, good for analog circuits such as operational amplifiers

Design Resources

- AD9739A Native FMC Card/Xilinx Reference Designs—*analog.com/en/AD9739A*
- LTC2000A-14 Demo Board (FMC), 14-Bit 2.7 GSPS DAC with DDR LVDS Interface—*analog.com/en/ltc2000a*
- Current Feedback (CFB) Op Amps—*analog.com/en/mt-034* *analog.com/en/mt-057*
- CN-0393: Simultaneous Sampling Signal Chain Featuring μModule™ Data Acquisition System—*analog.com/en/cn-0393*
- CN-0384: Completely Integrated Thermocouple Measurement System—*analog.com/en/cn-0384*

Design Tools/Forums

- LTspice®: ADI Circuit Simulator Tool—*analog.com/en/ltspice-simulator.html*
- EngineerZone®: Online Technical Support Community—*ez.analog.com*

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