

20位、1.8 MSPS、±2.5 ppm INL、低漂移、高精度数据采集解决方案

功能

数据采集解决方案在0°C至70°C范围内经过完全表征
保证20位无失码

INL: ±2 ppm, DNL: ±0.25 ppm

吞吐速率: 1.8 MSPS

失调误差漂移: ±3.5 ppm/°C, 增益误差漂移: ±6 ppm/°C

SNR: 98 dB (G = 1时), 92 dB (G = 10时), $f_{IN} = 1$ kHz

THD: -120 dB (G = 1时), -116 dB (G = 10时), $f_{IN} = 1$ kHz

过采样动态范围: 102 dB (900 kSPS), OSR = 2

软件可编程双极输入范围 (±1 V至±10 V)

允许单端和差分信号

CMRR: 92 dB (典型值)

GΩ输入阻抗允许与传感器直接接口

易用特性可降低系统功耗和复杂性

高达50 mA的ADC输入过压箝位保护吸电流

片内5 V基准电压和缓冲

第一转换精度, 无延迟/流水线延迟

快速转换时间支持低SPI时钟速率

SPI/QSPI/MICROWIRE/DSP兼容串行接口

应用

数据采集和系统监控

自动测试设备

仪器仪表

医疗设备

参考设计解决方案

开发数据采集信号链的系统设计人员通常需要高输入阻抗才能与各种传感器直接接口, 这些传感器可能具有变共模电压和单极或双极单端或差分输入信号。大多数仪器和可编程增益仪器仪表放大器(PGIA)传统上是单端输出, 不能直接驱动全差分、高分辨率、逐次逼近寄存器(SAR)模数转换器(ADC), 并且至少需要一个信号调理/驱动级。但是, 这种方法可能并不总是有助于严格的高精度性能, 即输入电平的线性、漂移和速度。

此参考设计采用了ADI公司独特的离散PGIA架构20位1.8 MSPS SAR ADC [AD4020](#)、带片内电源电路的5 V基准电压和基准缓冲。该解决方案提供了一个针对高精度而优化的经过完全表征、验证的设计, 从而在所有增益选项在0°C到70°C温度范围内全速提供前所未有的线性度(典型INL为±2 ppm)、低失调/增益误差漂移, 以及可跟踪噪声和失真(超过-115 dB)性能。差分输出PGIA使用现成离散元件, 获得具有GΩ输入阻抗、超过92 dB的共模抑制比、低输出噪声和低失真的数字可编程增益, 使其适合于直接与各种传感器类型接口并驱动高吞吐量、高分辨率SAR ADC而不影响性能。

有关如何测试基于[AD4020](#)的高精度数据采集解决方案的更多信息, 请参阅[UG-1280](#), 而要获取所有设计文件, 请联系Referencedesign@analog.com。

Rev. 0

Circuits from the Lab® reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

简化功能框图

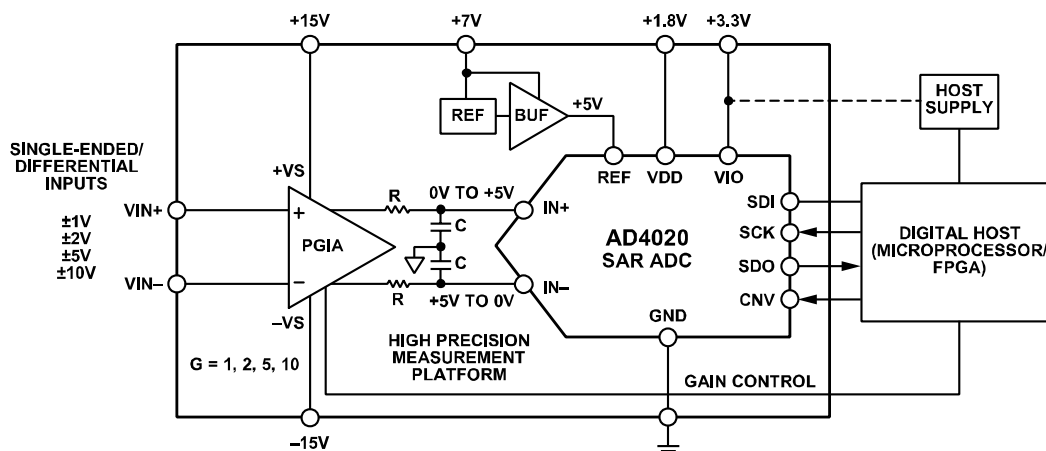


图1.

20173-001

参考设计解决方案

此参考设计可使用四个软件可编程增益选项 ($G = 1$ 、 2 、 5 和 10) 解决高达 ± 10 V的双极或单极单端或全差分输入范围。此外，它还允许PGIA中的高阶抗混叠滤波器和超量程校准选项。此解决方案提供了精准比率性能，并通过消除信号缓冲/放大/衰减、共模电平转换、抑制、建立时间简化了设计挑战，也避免了任何其他模拟信号调理挑战，并实现了更小的尺寸、更短的上市时间和更低的成本。

易于驱动的ADC [AD4020](#)采用减少非线性输入电流的高阻态模式，结合长采集阶段，允许与PGIA直接接口，并在中间使用一个简单的RC滤波器。[AD4020](#)高吞吐量可精确捕获高频信号，并允许信号抽取以实现宽动态范围，用于准确捕获低电平信号，并减少抗混叠滤波器的挑战。[AD4020](#)在 1.8 MSPS时仅消耗 15 mW功率，其功率与吞吐量呈线性关系。

[AD4020](#)串行外设接口(SPI)与 1.8 V、 2.5 V、 3 V和 5 V逻辑兼容，提供用户可编程模式和读写功能以启用/禁用易于使用的功能。请注意，参考设计的功能与[AD4020](#)器件本身的功能不同，同样也提供不同的性能参数。

表1. 典型输入范围选择

输入信号(V)	增益选项
差分	
± 1	$G = 5$
± 2.5	$G = 2$
± 5	$G = 1$
单端	
± 1	$G = 10$
± 2	$G = 5$
± 5	$G = 2$
± 10	$G = 1$

参考资料

[AD4020数据手册](#)

修订历史

2019年5月—修订版0：初始版

典型性能图

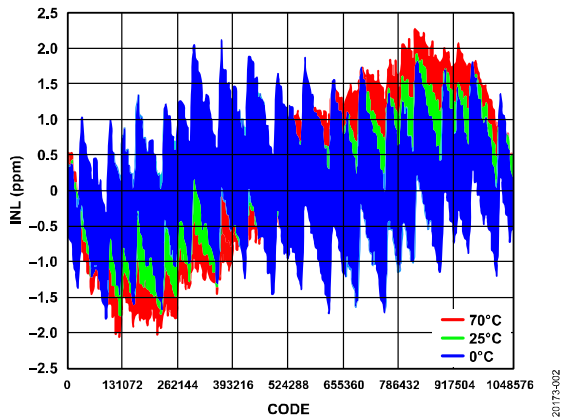


图2. 不同温度下INL与代码的关系, 高阻态模式禁用

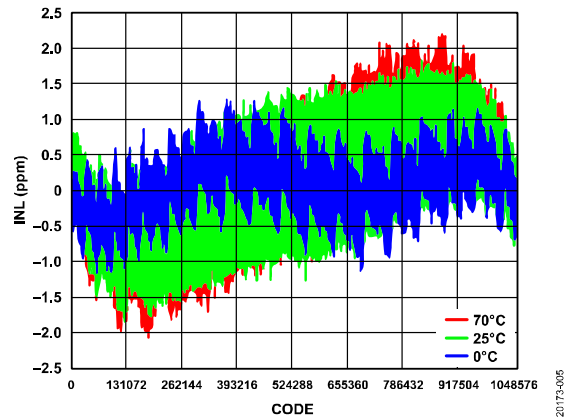


图5. 不同温度下INL与代码的关系, 高阻态模式启用

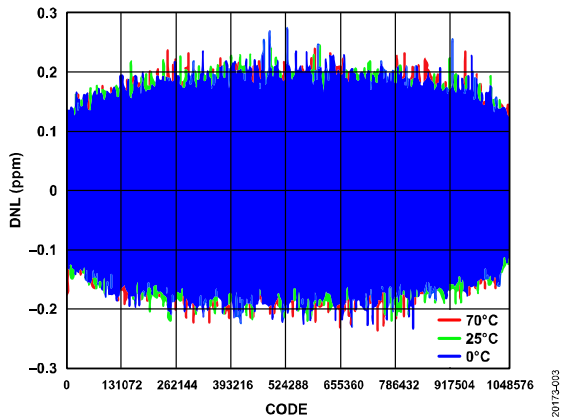


图3. 不同温度下DNL与代码的关系, 高阻态模式禁用

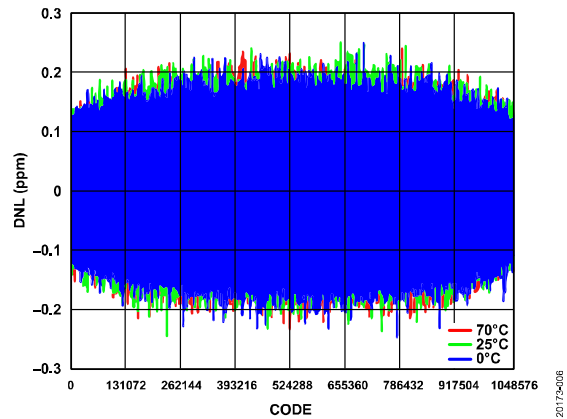


图6. 不同温度下DNL与代码的关系, 高阻态模式启用

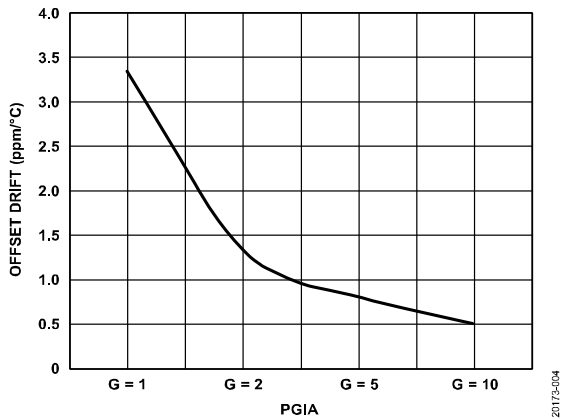


图4. 各种PGA增益的失调误差漂移

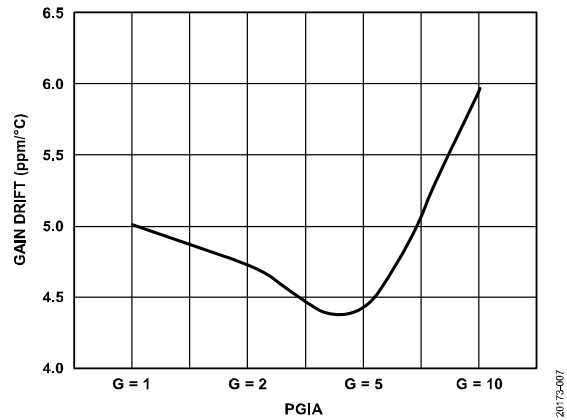


图7. 各种PGA增益的增益误差漂移

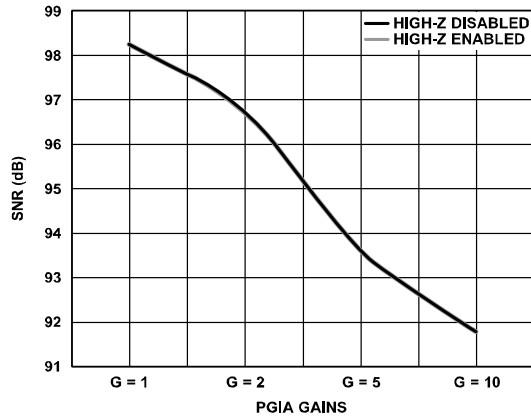


图8. 各种PGIA增益的SNR

2017-5-08

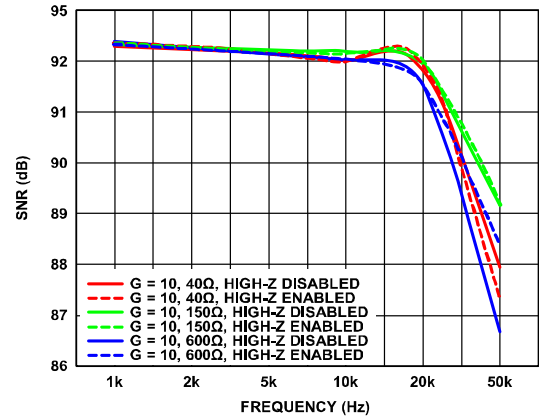


图11. SNR与输入频率的关系

2017-5-11

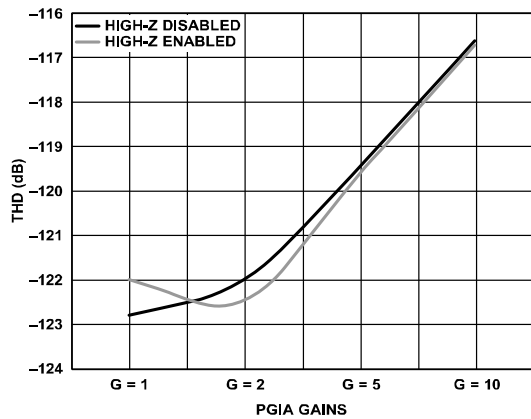


图9. 不同PGIA增益的THD

2017-5-08

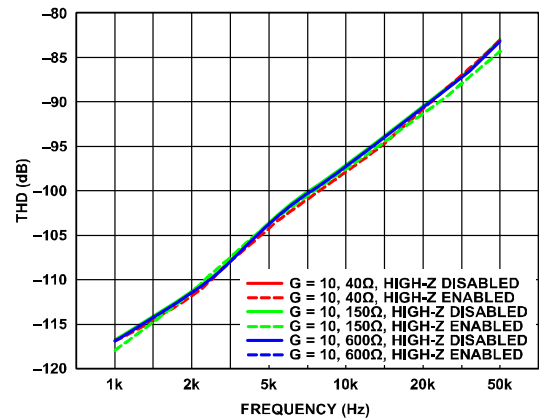


图12. 各种源阻抗下THD与输入频率的关系

2017-5-11

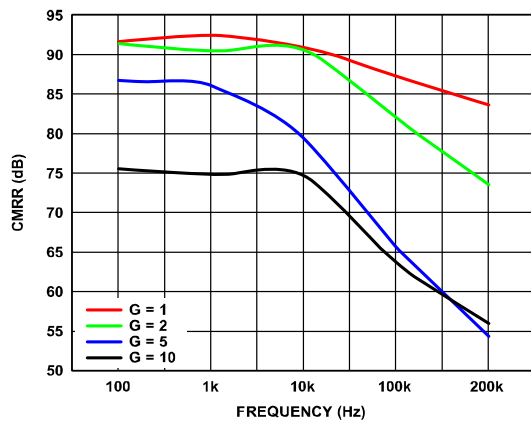


图10. 各种PGIA增益下CMRR与输入频率的关系

2017-5-10

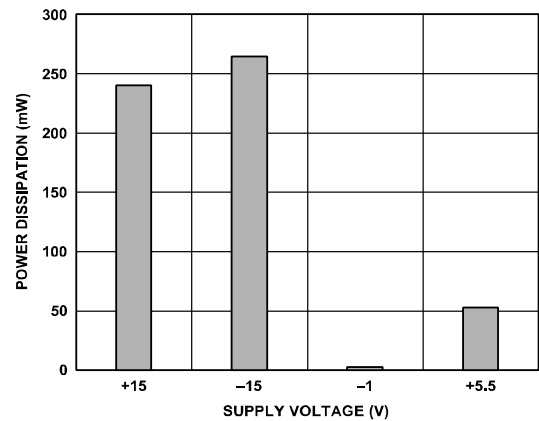


图13. 用于PGIA的各种电源轨的功率消耗

2017-5-13

注意

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.