

Circuits from the Lab®
Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0143.

连接/参考器件

AD8042	双通道、160 MHz轨到轨运算放大器
AD5620	单通道、12位缓冲电压输出DAC
AD5443	高带宽12位CMO电流输出DAC
ADR444	4.096 V精密低噪声基准电压源

利用运算放大器AD8042构建用于电压输出和电流输出DAC的单端差分转换器

电路功能与优势

采用单端信号走线时，来自信号源的一条导线贯穿于整个系统，直至数据采集接口。所测量的电压为信号与地的差值。遗憾的是，因为接地阻抗绝不可能为0，所以“地”在不同的地方可能具有不同的电平。这样，使用单端信号走线就可能产生误差，特别是当信号走线较长且地电流含有较大数字瞬变时。单端信号走线对噪声拾取敏感，因为它会起到天线的作用，拾取电活动的噪声。对于单端输入，无法区分信号与干扰噪声。大部分接地和噪声问题都通过差分信号技术来解决。

采用差分信号走线时，两条信号线从信号源接到数据采集接口，这就可以解决单端连接所引起的上述问题。发送接地层与接收接地层之间的噪声充当一个共模信号，因而得以大大衰减。使用双绞线会使噪声拾取表现为共模信号，它在接收端也会得到大大衰减。差分传输还有一个优势，即差分信号的幅度是等效单端信号的两倍，因此噪声抗扰度更高。

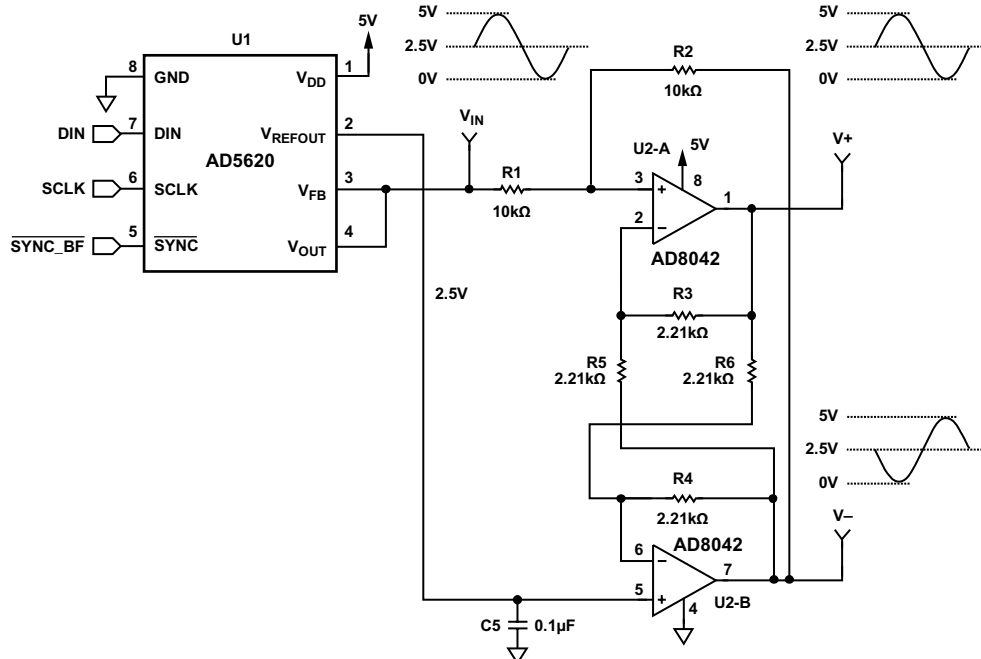


图1. 用于电压输出DAC AD5620的差分驱动器

Rev. A

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本文所述电路是一个差分驱动器，经过调整后，它既可用于电压输出DAC，也可用于电流输出DAC。该驱动器基于双通道运算放大器AD8042，配置为交叉耦合差分驱动器。AD8042具有一个轨到轨输出级和一个输入级，输出级在任一电源轨的30 mV范围内工作，输入级则可在负电源(本电路中为地)以下200 mV和正电源的1 V范围内工作。此外，AD8042具有160 MHz带宽和快速建立时间，堪称输出驱动器的理想选择。

电压输出DAC为nanoDAC®系列的12位AD5620。它内置一个5 ppm/°C片内基准电压源，采用8引脚SOT-23或MSOP封装。电流输出DAC为12位AD5443，它采用10引脚MSOP封装。

针对从工业CMOS DAC产生差分信号的应用，这两个电路代表一种高性价比、低功耗、小尺寸解决方案。两个电路均采用+5 V单电源供电。

电路描述

图1所示电路采用+5 V单电源供电，并使用电压输出DAC AD5620。DAC的输入由一个SPI端口控制。DAC的输出摆幅为0 V至+5 V。DAC片内基准电压源(+2.5 V)用来设置AD8042差分驱动器电路的共模电压。该基准电压源的温度系数为5 ppm/°C。V-端的输出是以+2.5 V共模电压为中心的反向

DAC输出。反馈网络和U2-B迫使V+端的电压与V-端的电压相位相差180°。该驱动器输入端和输出端的波形如图2所示。差分输出限制在各电源轨的大约30 mV范围内；因此，如果DAC在这些区间工作，将会发生一定的削波。

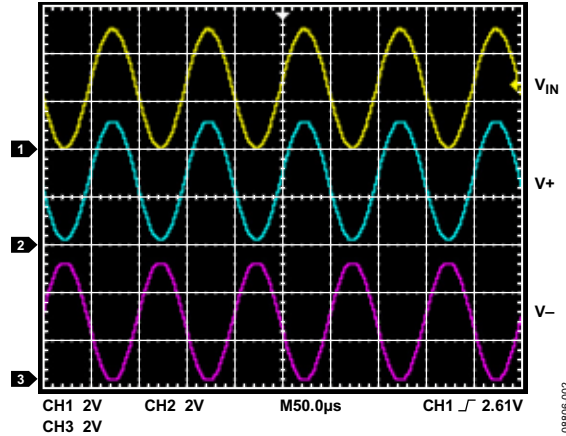


图2. 图1电路在100 kSPS更新速率时的 V_{IN} 、 $V+$ 和 $V-$

图3所示电路也采用+5 V单电源供电，并使用电流输出DAC AD5443，其IOUT2引脚接+2.5 V，VREF引脚接地。4.096 V精密基准电压源ADR444和一个分压器网络，用来产生该DAC IOUT2引脚所用的+2.5 V电压以及输出驱动器级所用的+3.75 V共模电压。

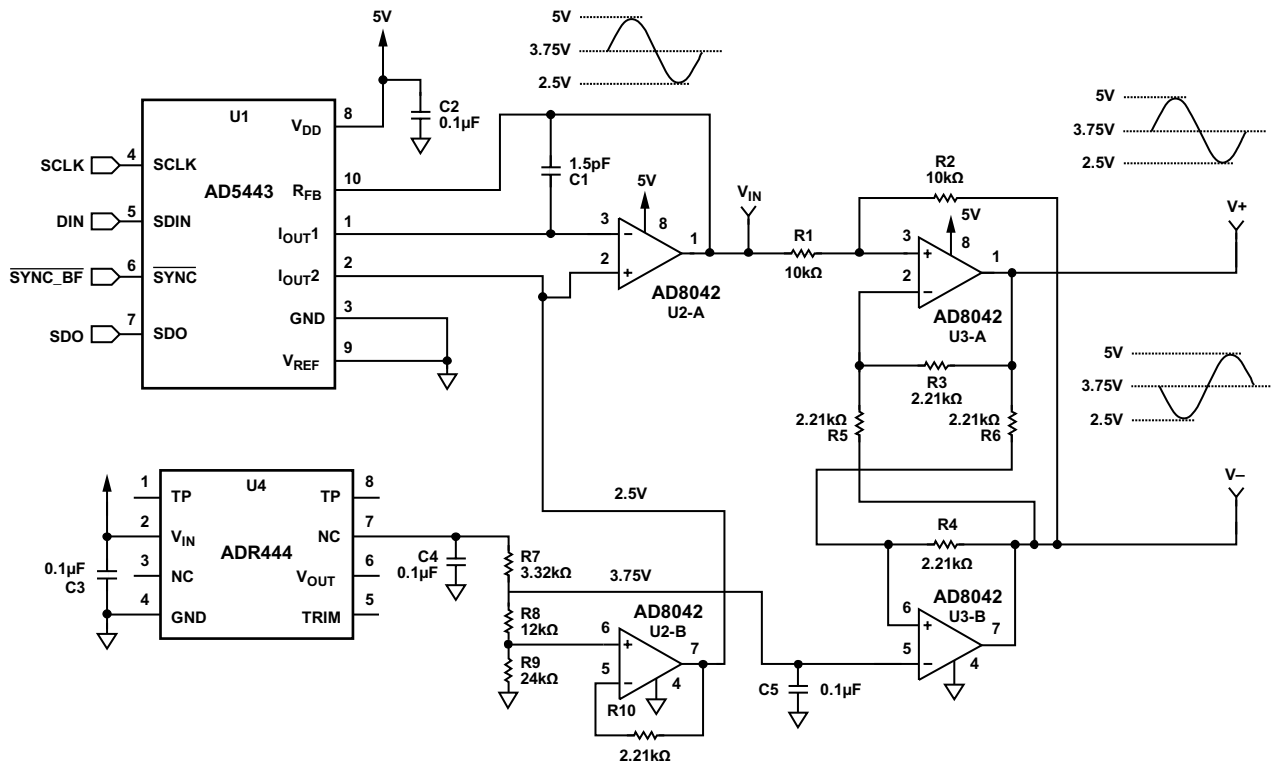


图3. 用于电流输出DAC AD5443的差分驱动器

在这些条件下，U2-A的输出摆幅为+2.5 V至+5 V。该驱动器的差分输出限制在正电源轨的大约30 mV范围内；因此，如果DAC在该区间工作，将会发生一定的削波。图4显示图3的输出驱动器级对应的输入和输出波形。

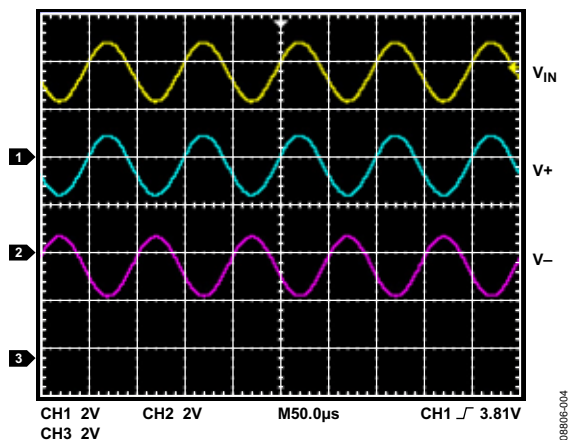


图4. 图3电路在100 kSPS更新速率时的 V_{IN} 、 $V+$ 和 $V-$

该单端差分转换器级的带宽典型值为10 MHz。不过，最大输出频率由DAC更新速率控制，AD5620为125 kSPS，AD5443为2.5 MSPS。根据采样原理，最大输出频率约为最大更新速率的三分之一。

为了使本文所讨论的电路达到理想的性能，必须采用出色的布局、接地和去耦技术(请参考教程MT-031和教程MT-101)。

常见变化

AD5640和AD5660分别是AD5620的14位和16位版本。AD5446是AD5443的14位版本。

了解详情

Kester, Walt. *The Data Conversion Handbook*. Chapter 3, 7. Analog Devices. 2005.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.
Voltage Reference Wizard Design Tool, Analog Devices.

数据手册和评估板

AD5443 Data Sheet

AD5443 Evaluation Board

AD5620 Data Sheet

AD5620 Evaluation Board

AD8042 Data Sheet

ADR444 Data Sheet

修订历史

2014年2月—修订版0至修订版A

更改图1 1

更改图2 2

2010年3月—修订版0：初始版

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