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Regulatory Compliance

The ADSP-BF561 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF561 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC amended by 93/68/EEC and therefore carries the “CE” mark.

The ADSP-BF561 EZ-KIT Lite has been appended to Analog Devices, Inc. Technical File (TCF) referenced ‘DSPTOOLS1’ dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

Technical Certificate No: Z600ANA1.016

Issued by: Technology International (Europe) Limited
60 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.
# CONTENTS

## PREFACE

- Product Overview ............................................................... xi
- Purpose of This Manual ......................................................... xiii
- Intended Audience ................................................................. xiii
- Manual Contents ................................................................. xiv
- What’s New in This Manual ................................................... xiv
- Technical Support ............................................................... xv
- Supported Processors ........................................................... xvi
- Product Information ............................................................ xvi
  - Analog Devices Web Site .................................................... xvi
  - EngineerZone ..................................................................... xvii
- Related Documents ............................................................. xviii
- Notation Conventions ............................................................ xviii

## USING THE ADSP-BF561 EZ-KIT LITE

- Package Contents ............................................................... 1-2
- Default Configuration .......................................................... 1-3
- CCES Install and Session Startup .......................................... 1-4
  - Session Startup ................................................................. 1-6
## Contents

VisualDSP++ Install and Session Startup ........................................... 1-8  
CCES Evaluation License .......................................................... 1-10  
VisualDSP++ Evaluation License ............................................... 1-11  
Memory Map ............................................................................ 1-11  
LEDs and Push Buttons ........................................................... 1-14  
Audio Interface ....................................................................... 1-15  
Video Interface ....................................................................... 1-16  
Board Design Database ............................................................. 1-17  
Example Programs .................................................................... 1-18  
Flash Programming Utility ....................................................... 1-18

### ADSP-BF561 EZ-KIT LITE HARDWARE REFERENCE

System Architecture ................................................................. 2-2  
  External Bus Interface Unit ................................................... 2-3  
  SPORT Audio Interface ....................................................... 2-3  
  SPI Interface ..................................................................... 2-3  
  Programmable Flags .......................................................... 2-4  
  PPI Interfaces .................................................................... 2-5  
    Video Output (PPI1) ....................................................... 2-7  
    Video Input (PPI0) ......................................................... 2-7  
  UART Port ....................................................................... 2-8  
  Expansion Interface ............................................................ 2-8  
  JTAG Emulation Port ........................................................... 2-9
Contents

Jumper and DIP Switch Settings ................................................................. 2-10
  Video Configuration Switch (SW2) .................................................. 2-10
  Boot Mode Switch (SW3) ............................................................... 2-11
  Push Button Enable Switch (SW4) .............................................. 2-12
  PPI Clock Select Switch (SW5) ..................................................... 2-13
  Test DIP Switches (SW10 and SW11) ........................................ 2-13
  Audio Enable Switch (SW12) ....................................................... 2-13
  SPIs1/SpIiS Select (SW13) ............................................................. 2-14
  Video Encoder Clock Select Jumper (JP1) ................................ 2-14
  VDDINT Select Jumpers (JP2 and JP3) ....................................... 2-14
  UART Loop Jumper (P1) ................................................................. 2-15

LEDs and Push Buttons ........................................................................... 2-15
  Reset Push Button (SW1) ............................................................ 2-16
  Programmable Flag Push Buttons (SW6–9) .................................. 2-16
  Power LED (LED1) ...................................................................... 2-16
  Reset LED (LED2) ....................................................................... 2-17
  USB Monitor LED (ZLED3) .......................................................... 2-17
  User LEDs (LED5–12, LED13–20) ............................................. 2-17

Connectors .............................................................................................. 2-18
  Expansion Interface (J1–3) ............................................................ 2-19
  Audio (J4 and J5) ......................................................................... 2-19
  Video (J6) .................................................................................. 2-20
  Power (J7) .................................................................................. 2-20
  RS-232 (P2) ................................................................................ 2-20
Contents

SPORT1 (P3) .......................................................... 2-21
SPI (P5) .......................................................... 2-21
USB Debug Agent Connector (ZJ1) ...................... 2-21
JTAG (ZP4) .................................................. 2-22

ADSP-BF561 EZ-KIT LITE BILL OF MATERIALS
ADSP-BF561 EZ-KIT LITE SCHEMATIC
INDEX
Thank you for purchasing the ADSP-BF561 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a type of embedded processor designed specifically to meet the computational demands and power constraints of today’s embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.
The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test the capabilities of the ADSP-BF561 Blackfin processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF561 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF561 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF561 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-BF561 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.
Product Overview

The board features:

- Analog Devices ADSP-BF561 Blackfin processor
  - 256-pin mini-BGA package
  - 30 MHz CLKIN oscillator
- Synchronous dynamic random access memory (SDRAM)
  - 64 MB (16M x 16 bits x 2 chips)
- Flash memory
  - 8 MB (4M x 16 bits)
- Analog audio interface
  - AD1836 A – Analog Devices 96 kHz audio codec
  - 4 input RCA phono jacks (2 stereo channels)
  - 6 output RCA phono jacks (3 stereo channels)
- Analog video interface
  - ADV7183A video decoder w/ 3 input RCA phono jacks
  - ADV7179 video encoder w/ 3 output RCA phono jacks
- Universal asynchronous receiver/transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - DB9 male connector


**Product Overview**

- **LEDs**
  - 20 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 16 general-purpose (amber), and 1 USB monitor (amber)
- **Push buttons**
  - 5 push buttons with debounce logic: 1 reset, 4 programmable flags
- **Expansion interface**
  - `PPI0`, `PPI1`, `SPI`, `EBIU`, `Timers11-0`, `UART`, programmable flags, `SPORT0`, `SPORT1`
- **Other features**
  - JTAG ICE 14-pin header

The EZ-KIT Lite board holds 8 MB of flash memory, which can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. The board also holds 512-Mb SDRAM, which can be used at runtime. For more information see “Memory Map” on page 1-11.

`SPORT0` interfaces with the AD1836A audio codec, facilitating creation of audio signal processing applications. `SPORT0` also attaches to an off-board connector to allow communication with other serial devices. For information about `SPORT0`, see “SPORT Audio Interface” on page 2-3.

The parallel peripheral interfaces (PPIs) of the processor connect to both a video encoder and video decoder, facilitating creation of video signal processing applications. For information on how the board utilizes the processor’s PPIs, see “PPI Interfaces” on page 2-5.

The UART of the processor connects to an RS-232 line driver and a DB9 male connector, allowing you to interface with a PC or other serial device. For information about the UART, see “UART Port” on page 2-8.
Additionally, the EZ-KIT Lite board provides access to most of the processor’s peripheral ports. Access is provided in the form of a three-connector expansion interface. For information about the expansion interface, see “Expansion Interface” on page 2-8.

**Purpose of This Manual**

The *ADSP-BF561 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF561 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

**Intended Audience**

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see “Related Documents”.

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user’s manuals.
Manual Contents

The manual consists of:

- Chapter 1, “Using the ADSP-BF561 EZ-KIT Lite” on page 1-1
  Describes the EZ-KIT Lite functionality from a programmer’s perspective and provides an easy-to-access memory map

- Chapter 2, “ADSP-BF561 EZ-KIT Lite Hardware Reference” on page 2-1
  Provides information on the EZ-KIT Lite hardware components.

- Appendix A, “ADSP-BF561 EZ-KIT Lite Bill Of Materials” on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.

- Appendix B, “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design. Appendix B is part of the online help.

What’s New in This Manual

This is revision 3.3 of the ADSP-BF561 EZ-KIT Lite Evaluation System Manual. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.
Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  http://ez.analog.com/community/dsp

- Submit your questions to technical support directly at:
  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from CrossCore Embedded Studio or VisualDSP++:
  Choose Help > Email Support. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your CrossCore Embedded Studio or VisualDSP++ version information and license.dat file.

- E-mail your questions about processors and processor applications to:
  processor.support@analog.com or
  processor.china@analog.com (Greater China support)

- In the USA only, call 1-800-ANALOGD (1-800-262-5643)

- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  www.analog.com/adi-sales
Supported Processors

- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF561 Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site


To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information
about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals.

myAnalog provides access to books, application notes, data sheets, code examples, and more.

Visit myAnalog (found on the Analog Devices home page) to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

**EngineerZone**

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.
Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

<table>
<thead>
<tr>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADSP-BF561 Blackfin Embedded Symmetric Multiprocessor Data Sheet</strong></td>
<td>General functional description, pinout, and timing of the processor</td>
</tr>
<tr>
<td><strong>ADSP-BF561 Blackfin Processor Hardware Reference</strong></td>
<td>Description of the internal processor architecture and all register functions</td>
</tr>
<tr>
<td><strong>Blackfin Processor Programming Reference</strong></td>
<td>Description of all allowed processor assembly instructions</td>
</tr>
</tbody>
</table>

Notation Conventions

Text conventions used in this manual are identified and described as follows.

<table>
<thead>
<tr>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Close command (File menu)</td>
<td>Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the Close command appears on the File menu).</td>
</tr>
<tr>
<td>{this</td>
<td>that}</td>
</tr>
<tr>
<td>[this</td>
<td>that]</td>
</tr>
<tr>
<td>[this,...]</td>
<td>Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of this.</td>
</tr>
<tr>
<td>.SECTION</td>
<td>Commands, directives, keywords, and feature names are in text with letter gothic font.</td>
</tr>
</tbody>
</table>
**Preface**

<table>
<thead>
<tr>
<th>Example</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>filename</td>
<td>Non-keyword placeholders appear in text with italic style format.</td>
</tr>
</tbody>
</table>
| ![Note](image) | **Note:** For correct operation, ...  
A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol. |
| ![Caution](image) | **Caution:** Incorrect device operation may result if ...  
**Caution:** Device damage may result if ...  
A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol. |
| ![Warning](image) | **Warning:** Injury to device users may result if ...  
A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol. |
1 USING THE ADSP-BF561 EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF561 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- “Package Contents” on page 1-2
  Lists the items contained in your ADSP-BF561 EZ-KIT Lite package.

- “Default Configuration” on page 1-3
  Shows the default configuration of the ADSP-BF561 EZ-KIT Lite.

- “CCES Install and Session Startup” on page 1-4
  Instructs how to start a new or open an existing ADSP-BF561EZ-KIT Lite session using CCES.

- “VisualDSP++ Install and Session Startup” on page 1-8
  Instructs how to start a new or open an existing ADSP-BF561EZ-KIT Lite session using VisualDSP++.

- “CCES Evaluation License” on page 1-10
  Describes the CCES demo license shipped with the EZ-KIT Lite.

- “VisualDSP++ Evaluation License” on page 1-11
  Describes the VisualDSP++ demo license shipped with the EZ-KIT Lite.

- “Memory Map” on page 1-11
  Defines the ADSP-BF561 EZ-KIT Lite’s external memory map.
Package Contents

Your ADSP-BF561 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF561 EZ-KIT Lite board
- Universal 7V DC power supply
- USB 2.0 cable
If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

**Default Configuration**

The ADSP-BF561 EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF561 EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.
CCES Install and Session Startup

Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-BF561 EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/Blackfin/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.
Using the ADSP-BF561 EZ-KIT Lite

**Step 1:** Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

**Using an Emulator:**

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.

2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

**Using the on-board Debug Agent:**

1. Plug one side of the USB cable into the USB connector of the debug agent ZJ1 (labeled USB).

2. Plug the other side of the cable into a USB port of the PC running CCES.

**Step 2:** Attach the provided cord and appropriate plug to the power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J7 (labeled Power) on the EZ-KIT Lite board.

2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED1) is lit green when power is applied to the board.

3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power is lit green when power is applied.
CCES Install and Session Startup

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3) on the debug agent is on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the Start menu.

Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

If a debug configuration exists already, select the appropriate configuration and click Apply and Debug or Debug. Go to step 8.

To create a debug configuration, do one of the following:

- Click the down arrow next to the little bug icon, select Debug Configurations
- Choose Run > Debug Configurations.

The Debug Configuration dialog box appears.

3. Select CrossCore Embedded Studio Application and click (New launch configuration).

The Select Processor page of the Session Wizard appears.
Using the ADSP-BF561 EZ-KIT Lite


The Select Connection Type page of the Session Wizard appears.

5. Select one of the following:

   • For standalone debug agent connections, EZ-KIT Lite and click Next.
     
   • For emulator connections, Emulator and click Next.

The Select Platform page of the Session Wizard appears.

6. Do one of the following:

   • For standalone debug agent connections, ensure that the selected platform is ADSP-BF561 EZ-KIT Lite via Debug Agent.
   
   • For emulator connections, choose the type of emulator that is connected to the board.

7. Click Finish to close the wizard.

The new debug configuration is created and added to the program(s) to load list.

8. In the Program(s) to load section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.
VisualDSP++ Install and Session Startup

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click ☒ and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run > Terminate**.

To delete a session, choose **Target > Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

**VisualDSP++ Install and Session Startup**

For information about VisualDSP++ and to download the software, go to [www.analog.com/VisualDSP](http://www.analog.com/VisualDSP).

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start > Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.
Using the ADSP-BF561 EZ-KIT Lite

3. To connect to a new EZ-KIT Lite session, start Session Wizard by selecting one of the following.

   - From the Session menu, New Session.
   - From the Session menu, Session List. Then click New Session from the Session List dialog box.
   - From the Session menu, Connect to Target.


5. The Select Connection Type page of the wizard appears on the screen. Select EZ-KIT Lite and click Next.

6. The Select Platform page of the wizard appears on the screen. In the Select your platform list, select ADSP-BF561 EZ-KIT Lite via Debug Agent. In Session name, highlight or specify the session name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and to open a new session.

   Click Next.

7. The Finish page of the wizard appears on the screen. The page displays your selections. If you are satisfied, click Finish. If not, click Back to make changes.
CCES Evaluation License

To disconnect from a session, click the disconnect button or select Session > Disconnect from Target.

To delete a session, select Session > Session List. Select the session name from the list and click Delete. Click OK.

CCES Evaluation License

The ADSP-BF561 EZ-KIT Lite software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF56x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to: http://www.analog.com/buyonline.

- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to: http://www.analog.com/salesdir/continent.asp.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.
VisualDSP++ Evaluation License

The ADSP-BF561 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF561 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.

- The linker restricts a user's program to 41 KB of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

Memory Map

The EZ-KIT Lite board includes two types of external memory, 64-MB SDRAM and 8-MB flash. See the external memory map in Table 1-1. The complete configuration of the ADSP-BF561 processor internal SRAM is detailed in Figure 1-2.

Table 1-1. EZ-KIT Lite External Memory Map

<table>
<thead>
<tr>
<th>Start Address</th>
<th>End Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000</td>
<td>0x3FFFFFF</td>
<td>SDRAM bank 0; see &quot;Memory Map&quot; on page 1-11</td>
</tr>
<tr>
<td>0x20000000</td>
<td>0x207FFFFF</td>
<td>ASYNC memory bank 0; see &quot;Memory Map&quot; on page 1-11.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All other locations Not used</td>
</tr>
</tbody>
</table>
The 8 MB of flash memory is organized as 4M x 16 bit and mapped into an ADSP-BF561 processor’s ASYNC memory bank 0. The memory select signal connects to the output enable pin of flash memory.

The 64 MB of SDRAM is organized as 16M x 32 bits wide. The processor’s memory select pin is configured for SDRAM. Three SDRAM control registers must be initialized in order to access the SDRAM memory.

---

Figure 1-2. ADSP-BF561 Processor Internal Memory Map
When in a CCES or VisualDSP++ session, you can configure the SDRAM registers automatically:

- CCES users, choose Target > Settings > Target Options > Use XML reset values
- VisualDSP++ users, choose Settings > Target Options > Use XML reset values

The EBIU_SDGCTL, EBIU_SDBCTL, and EBIU_SDRRC register values have been set in the ADSP-BF561-proc.xml file found in your System\ArchDef folder. These values can be changed to be more optimal depending on the SCLK frequency.

The values in Table 1-2 are set by default whenever bank 0 is accessed through the debugger (for example, when viewing memory windows or loading a program). The numbers are derived for maximum flexibility and work for a system clock frequency between 60 MHz and 133 MHz.

Table 1-2. EZ-KIT Lite Session SDRAM Default Settings

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>EBIU_SDGCTL</td>
<td>0x0091998D</td>
<td>Calculated with SCLK = 133 MHz</td>
</tr>
<tr>
<td>EBIU_SDBCTL</td>
<td>0x00000013</td>
<td></td>
</tr>
<tr>
<td>EBIU_SDRRC</td>
<td>0x000001CF</td>
<td>Calculated with SCLK = 120 MHz</td>
</tr>
</tbody>
</table>

The EBIU_SDGCTL register can be written once after the processor comes out of reset. Therefore, the user code should not re-initialize the register. Clearing the Use XML reset values check box allows manual configuration of the EBIU registers. For more information, see online help.
LEDs and Push Buttons

Automatic configuration of SDRAM is not optimized for a specific SCLK frequency. Table 1-3 shows the optimized configuration of the SDRAM registers using a 120 MHz SCLK. The frequency of 120 MHz is the maximum SCLK frequency when using a 600 MHz core frequency, the maximum frequency for the EZ-KIT Lite. Only the EBIU_SDRRC register needs to be modified in the user code to achieve maximum performance.

Table 1-3. SDRAM Optimum Settings

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>EBIU_SDGCTL</td>
<td>0x0091998D</td>
</tr>
<tr>
<td>EBIU_SDBCTL</td>
<td>0x00000013</td>
</tr>
<tr>
<td>EBIU_SDRRC</td>
<td>0x000003A0</td>
</tr>
</tbody>
</table>

1 Calculated with SCLK = 120 MHz

For more information, see “External Bus Interface Unit” on page 2-3.

An example program is included in the EZ-KIT installation directory to demonstrate the SDRAM interface setup.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and sixteen LEDs for general-purpose IO.

Sixteen LEDs, labeled LED5 through LED20, are controlled by the processor’s programmable flags PF32 through PF47 (equivalent to PPI0_D15–8 and PPI1_D15–8). These LEDs are accessed through the FLAG 2 registers. First, the direction must be configured to output by setting the bits of the FIO2_DIR register to 1. Then the value of the LEDs are modified using one of the FIO2_FLAG_D, FIO2_FLAG_C, FIO2_FLAG_S, or FIO2_FLAG_T registers.

The four general-purpose push buttons are labeled SW6 through SW9. The buttons connect to the programmable flags PF8–5. A status of each
Using the ADSP-BF561 EZ-KIT Lite

individual button can be read through the \texttt{FI00\_FLAG\_D} register. A switch is being pressed-on when the corresponding bit of the register reads 1. When the switch is released, the bit reads 0. A connection between the push button and PF input is established through the \texttt{SW4} DIP switch.

For information on how to disconnect the switch from the programmable flag and use it for another objective, see “Push Button Enable Switch (SW4)”.

\hspace{1cm} An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

\textbf{Audio Interface}

The AD1836A audio codec provides three channels of stereo audio output and two channels of multichannel 96 kHz input. The \texttt{SPORT0} interface of the processor links with the stereo audio data input and output pins of the AD1836A codec. The processor is capable of transferring data to the audio codec in time-division multiplexed (TDM) or 2-wire serial interface (TWI) mode.

In TWI mode, the codec can operate at a 96 kHz sample rate but restricts the output to two channels. In TDM mode, the codec can operate at a maximum of 48 kHz sample rate but allows simultaneous use of all input and output channels. When using TWI mode, the \texttt{TSCLK0} and \texttt{RSCLK0} pins (as well as the \texttt{TFS0} and \texttt{RFS0} pins of the processor) must be tied together externally to the processor. This is accomplished with the \texttt{SW4} DIP switch. See “Push Button Enable Switch (SW4)” on page 2-12 for more information.

The AD1836A audio codec’s internal configuration registers are configured using the processor’s \texttt{PF4} programmable flag pin, used as the select for the audio device. For more information on how to configure the multichannel codec, go to \url{www.analog.com/AD1836A}. 
Video Interface

The AD1836A codec reset is controlled by the processor’s programmable flag PF15. When PF15 is 0, the reset is asserted. When PF15 is 1, the reset is de-asserted. Note that when PF15 is not driven (configured as input), the AD1836A reset is asserted due to the pull-down resistor. See “Programmable Flags” on page 2-4 for more information.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the AD1836A codec operation.

Video Interface

The board supports video input and output applications. The ADV7179 video encoder provides up to three output channels of analog video, while the ADV7183A video decoder provides up to three input channels of analog video. The video encoder connects to the parallel peripheral interface 1 (PPI1), while the video decoder connects to the parallel peripheral interface 0, (PPI0). Each PPI interface has an individual clock that is configured by the SW5 switch settings. See “PPI Clock Select Switch (SW5)” on page 2-13 for more information.

Both the encoder and the decoder connect to the parallel peripheral interfaces (PPI input clock) of the processor. For additional information on the video interface hardware, refer to “PPI Interfaces” on page 2-5.

For the video interface to be operational, the following basic steps must be performed.

1. Configure the SW2 DIP switch as required by the application. Refer to “Video Configuration Switch (SW2)” on page 2-10 for details.

2. De-assert the video device’s reset by setting high a corresponding programmable flag. PF14 controls the ADV7179 encoder’s reset, while PF13 controls the ADV7183A decoder’s reset.
Using the ADSP-BF561 EZ-KIT Lite

3. If using the ADV7183A decoder:
   - Enable device by driving programmable flag output PF2 to 0.
   - Select PPI0 clock; for details, refer to “PPI Clock Select Switch (SW5)” on page 2-13.

4. Program internal registers of the video device in use. Both video encoder and decoder use a 2-wire serial interface to access internal registers. The PF0 programmable flag functions as a serial clock (SCL), and PF1 functions as a serial data (SDAT).

5. Program the ADSP-BF561 processor’s PPI interfaces (configuration registers, DMA, and so on).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the capabilities of the video interface.

Board Design Database

A .zip file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at:

Example Programs

Example Programs

Example programs are provided with the ADSP-BF561 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the Examples folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

Flash Programming Utility

Flash Programming Utility

The ADSP-BF561 EZ-KIT Lite evaluation system includes a flash programming utility. The utility allows you to program flash memory on the EZ-KIT Lite. The utility installed with VisualDSP++ is called Flash Programmer. The utility installed with CCES is called Device Programmer.

The flash programming driver is core-specific (core A) and must be loaded to core A in order to operate correctly. The flash programming utility relies on the user to set the correct core focus. To set the correct core, select core A in the multiprocessor window before opening the utility interface.

For more information on the flash programming utility, refer to the online help.
2 ADSP-BF561 EZ-KIT LITE
HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF561 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-BF561 EZ-KIT Lite configuration and explains how the board components interface with the processor.

- "Jumper and DIP Switch Settings" on page 2-10
  Shows the locations and describes the configuration jumpers and switches.

- "LEDs and Push Buttons" on page 2-15
  Shows the locations and describes the LEDs and push buttons.

- "Connectors" on page 2-18
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.
This section describes the processor's configuration on the EZ-KIT Lite board.

Figure 2-1. System Architecture

This EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF561 Blackfin processor. The processor has an IO voltage of 3.3V. The core voltage and the core clock rate can be set on the fly by the processor. The input clock is 30 MHz.
External Bus Interface Unit

The external bus interface unit (EBIU) connects external memory to the ADSP-BF561 processor. It includes a 32-bit wide data bus, an address bus (A25–2), and a control bus. All of the 8-bit, 16-bit, and 32-bit accesses are supported. On the EZ-KIT Lite board, the EBI unit connects to SDRAM and flash memory. For more information on using the external memory see “Memory Map” on page 1-11.

All of the address, data, and control signals are available externally via the expansion interface connectors (J1–3). The pinout of these connectors can be found in “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1.

SPORT Audio Interface

The SPORT0 interface connects to the AD1836A audio codec and the expansion interface. The AD1836A codec uses both the primary and secondary data transmit and receive pins to input and output data from the audio input and outputs.

The SPORT1 interface connects to the SPORT connector (P3).

The pinout of the SPORT and expansion interface connectors can be found in “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1.

SPI Interface

The processor’s serial peripheral interface (SPI) connects to the AD1836A audio codec and the expansion interface. The SPI connection to the AD1836A codec is used to access the control registers of the device. The PF4 flag of the processor acts as the device select for the SPI port.

The SPI signals are available on the expansion interface and on the SPI connector (P5). The pinout for the interface can be found in “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1.
**Programmable Flags**

The processor has 48 programmable flag pins (PFs). Many of the flags are multi-functional and depend on the processor’s setup. Table 2-1 shows how the programmable flag pins are used on the EZ-KIT Lite.

Table 2-1. Programmable Flag Connections

<table>
<thead>
<tr>
<th>Processor PF Pin</th>
<th>Processor Function</th>
<th>EZ-KIT Lite Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF0</td>
<td>SPI select 5, timer 0</td>
<td>Serial clock for programming ADV7179 video encoder and ADV7183A video decoder.</td>
</tr>
<tr>
<td>PF1</td>
<td>SPI select 1, timer 1</td>
<td>Serial data for programming ADV7179 video encoder and ADV7183A video decoder.</td>
</tr>
<tr>
<td>PF2</td>
<td>SPI select 2, timer 2</td>
<td>ADV7183A video decoder's OE.</td>
</tr>
<tr>
<td>PF3</td>
<td>SPI select 3, timer 3</td>
<td>ADV7183A FIELD pin. See “Video Configuration Switch (SW2)” on page 2-10.</td>
</tr>
<tr>
<td>PF4</td>
<td>SPI select 4, timer 4</td>
<td>AD1836A audio codec's SPI select.</td>
</tr>
<tr>
<td>PF5</td>
<td>SPI select 5, timer 5</td>
<td>Push button (SW6). See &quot;LEDs and Push Buttons&quot; on page 1-14 and &quot;Push Button Enable Switch (SW4)&quot; on page 2-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF6</td>
<td>SPI select 6, timer 6</td>
<td>Push button (SW7). See &quot;LEDs and Push Buttons&quot; on page 1-14 and &quot;Push Button Enable Switch (SW4)&quot; on page 2-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF7</td>
<td>SPI select 7, timer 7</td>
<td>Push button (SW8). See &quot;LEDs and Push Buttons&quot; on page 1-14 and &quot;Push Button Enable Switch (SW4)&quot; on page 2-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF8</td>
<td></td>
<td>Push button (SW9). See &quot;LEDs and Push Buttons&quot; on page 1-14 and &quot;Push Button Enable Switch (SW4)&quot; on page 2-12 for information on how to disable the push button.</td>
</tr>
<tr>
<td>PF9–12</td>
<td></td>
<td>Not used</td>
</tr>
<tr>
<td>PF13</td>
<td></td>
<td>ADV7183A video decoder's reset</td>
</tr>
</tbody>
</table>
The ADSP-BF561 processor employs two independent parallel peripheral interfaces (PPIs), PPI0 and PPI1. Each PPI interface is a half-duplex, bi-directional bus consisting of 16 bits of data, a dedicated input clock,
System Architecture

and synchronization signals. The ADSP-BF561 EZ-KIT Lite board utilizes the PPI interfaces for video input and video output.

The **PPI0** interface is configured to input video data from the ADV7183A video decoder device: bits 7–0 connect to the video decoder’s data outputs. The **PPI1** interface is configured to output video data to the ADV7179 video encoder device: bits 7–0 connect to the video encoder’s data inputs.

Each PPI interface has a dedicated clock input configured independently by the **SW5** switch. The clock source can be one of the following: 27 MHz crystal oscillator, ADV7183A video decoder’s clock output, or external clock from the expansion interface. See “PPI Clock Select Switch (SW5)” on page 2-13 for more information about the switch.

The **SW2** switch provides a flexible connection between dedicated synchronization IOs (**SYNC1** and **SYNC2** of each PPI interface) and the encoder’s and decoder’s horizontal and vertical synchronization pins. See “Video Configuration Switch (SW2)” on page 2-10 for more information about the switch. For a detailed description of the ADSP-BF561 processor’s PPI interfaces, refer to the *ADSP-BF561 Blackfin Processor Hardware Reference*.

Table 2-2 describes the PPI pins of the EZ-KIT Lite board.

Table 2-2. PPI Connections

<table>
<thead>
<tr>
<th>Processor PPI Pin</th>
<th>Other Processor Function</th>
<th>EZ-KIT Lite Function</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PPI0</strong> bits 7–0</td>
<td>ADV7183A data outputs</td>
<td>P15–8</td>
</tr>
<tr>
<td><strong>PPI1</strong> bits 7–0</td>
<td>ADV7179 data inputs</td>
<td>P7–0</td>
</tr>
<tr>
<td><strong>PPI0</strong> <strong>SYNC1</strong></td>
<td>Timer 8</td>
<td>ADV7179 HSYNC. For more information, see “Video Configuration Switch (SW2)” on page 2-10.</td>
</tr>
<tr>
<td><strong>PPI0</strong> <strong>SYNC2</strong></td>
<td>Timer 9</td>
<td>ADV7179 VSYNC. For more information, see “Video Configuration Switch (SW2)” on page 2-10.</td>
</tr>
<tr>
<td><strong>PPI0 clock</strong></td>
<td>A choice of ADV7183A output clock, a local 27 MHz oscillator, or an external clock from ADSP-BF533/BF561 Blackfin EZ-Extender®.</td>
<td></td>
</tr>
</tbody>
</table>
Video Output (PPI1)

The PPI1 interface is configured as output and connects to the on-board video encoder device, ADV7179. The ADV7179 encoder generates three analog video channels on DAC A, DAC B, and DAC C. The PPI1 bits 7–0 connect to P7–0 of the encoder’s pixel inputs. The encoder’s input clock is fixed and comes from an on-board 27 MHz oscillator.

The encoder’s synchronization signals, HSYNC and VSYNC, can be configured as inputs or outputs. Video blanking control signal is at level 1. The HSYNC and VSYNC signals can connect to SYNC1 and SYNC2 of the processor’s PPI1 interface via the SW2 switch, as described in “Video Configuration Switch (SW2)” on page 2-10.

Video Input (PPI0)

The PPI0 interface is configured as input and connects to the on-board video decoder device, ADV7183A. The ADV7183A decoder receives three analog video channels on AIN1, AIN4, and AIN5 input. The decoder’s pixel data outputs P15–8 drive the PPI0 inputs 8–0. The decoder’s 27 MHz pixel clock output can be selected to drive any of the PPI clocks as shown in Table 2-7 on page 2-13.
System Architecture

Synchronization outputs of the decoder, \texttt{HS/HACTIVE}, \texttt{VS/VACTIVE}, and \texttt{FIELD} can connect to the processor's PPI0\_SYNC1, PPI0\_SYNC2, and PF3 flag via the \texttt{SW2} DIP switch, as described in “Video Configuration Switch (SW2)” on page 2-10.

UART Port

The processor’s universal asynchronous receiver/transmitter (UART) port connects to the ADM3202 RS-232 line driver as well as to the expansion interface. The RS-232 line driver is attached to the DB9 male connector, providing an interface to a personal computer and other serial devices.

Expansion Interface

The expansion interface consists of the three 90-pin connectors, J1–3. Table 2-3 shows the interfaces each connector provides. For the exact pin-out of the connectors, refer to “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1. The mechanical dimensions of the connectors can be obtained from Technical Support.

Table 2-3. Connector Interfaces

<table>
<thead>
<tr>
<th>Connector</th>
<th>Interfaces</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>5V, GND, address, data, PPI0 3–0, PF15–6, PF4</td>
</tr>
<tr>
<td>J2</td>
<td>3.3V, GND, SPI, NMI, PPI0 SYNC3–1, SPORT0, SPORT1, PF15–0, EBU1 control signals</td>
</tr>
<tr>
<td>J3</td>
<td>5V, 3.3V, GND, UART, PPI1 15–0, reset, video control signals</td>
</tr>
</tbody>
</table>
Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry also can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

**JTAG Emulation Port**

The JTAG emulation port allows an emulator to access internal and external memories of the processor through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at ZP4, the USB debugging interface is disabled. See “JTAG (ZP4)” on page 2-22 for more information about the JTAG connector.

To learn more about available emulators, go to [http://www.analog.com/processors/tools/blackfin](http://www.analog.com/processors/tools/blackfin).
Jumper and DIP Switch Settings

This section describes functionality of the jumpers and DIP switches. The jumper and DIP switch locations are shown in Figure 2-2.

![Figure 2-2. DIP Switch Locations](image)

**Video Configuration Switch (SW2)**

The video configuration switch (SW2) determines how some video signals from the ADV7183A video decoder and ADV7179 video encoder are routed to the processor’s PPIs. The switch also determines if the PF2 pin controls the OE signal of the ADV7183A video decoder outputs. See Table 2-4.
Positions 1 through 5 of SW2 determine how and if the \textit{SYNC1}, \textit{SYNC2}, and \textit{FIELD} control signals of the \textit{PPI0} and \textit{PPI1} interfaces are routed to the processor’s PPIs. In standard configuration of the encoder and decoder, this is not necessary because the processor is capable of reading the control information embedded in the data stream.

Position 6 of SW2 determines whether PF2 connects to the \textit{OE} signal of the ADV7183A device. When the switch is \textit{OFF}, PF2 can be used for other operations, and the decoder output enable is held high with a pull-up resistor.

**Boot Mode Switch (SW3)**

Positions 1 and 2 of the SW3 switch set the boot mode of the processor, as described in Table 2-5. Position 3 sets the processor’s PLL on boot—when the position is \textit{ON}, the PLL is in bypass.

<table>
<thead>
<tr>
<th>Switch Position (Default)</th>
<th>Processor Signal</th>
<th>Video Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (OFF)</td>
<td>PPI1 SYN1</td>
<td>ADV7179</td>
</tr>
<tr>
<td>2 (OFF)</td>
<td>PPI0 SYN1</td>
<td>ADV7183A</td>
</tr>
<tr>
<td>3 (OFF)</td>
<td>PPI1 SYN2</td>
<td>ADV7183A</td>
</tr>
<tr>
<td>4 (OFF)</td>
<td>PPI1 SYN2</td>
<td>ADV7179</td>
</tr>
<tr>
<td>5 (OFF)</td>
<td>PF3 (FIELD)</td>
<td>ADV7183A</td>
</tr>
<tr>
<td>6 (ON)</td>
<td>PF2</td>
<td>ADV7183A</td>
</tr>
</tbody>
</table>
Table 2-5. Boot Mode Select Switch (SW3)

<table>
<thead>
<tr>
<th>Position 1 BMODE0</th>
<th>Position 2 BMODE1</th>
<th>Boot Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ON</td>
<td>Execute from 16-bit external memory (Bypass Boot ROM)</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>Boot from 8-bit/16-bit flash (default)</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>Boot from SPI host slave mode</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>Boot from SPI serial EEPROM (16-, 24-bit address range)</td>
</tr>
</tbody>
</table>

Push Button Enable Switch (SW4)

Positions 1 through 4 of the push button enable switch (SW4) allow to disconnect the drivers associated with the push buttons from the PF pins of the processor. Positions 5 and 6 connect the transmit and receive frame syncs and clocks of SPORT0. This is important when the AD1836A audio codec and the processor are communicating in 2-wire interface (TWI) mode. Table 2-6 shows which PF is driven when the switch is ON.

Table 2-6. Push Button Enable Switch (SW4)

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>Default Setting</th>
<th>Pin #</th>
<th>Signal (Side 1)</th>
<th>Pin #</th>
<th>Signal (Side 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ON</td>
<td>1</td>
<td>SW6</td>
<td>12</td>
<td>PF5</td>
</tr>
<tr>
<td>2</td>
<td>ON</td>
<td>2</td>
<td>SW7</td>
<td>11</td>
<td>PF6</td>
</tr>
<tr>
<td>3</td>
<td>ON</td>
<td>3</td>
<td>SW8</td>
<td>10</td>
<td>PF7</td>
</tr>
<tr>
<td>4</td>
<td>ON</td>
<td>4</td>
<td>SW9</td>
<td>9</td>
<td>PF8</td>
</tr>
<tr>
<td>5</td>
<td>OFF</td>
<td>5</td>
<td>TFS0</td>
<td>8</td>
<td>RFS0</td>
</tr>
<tr>
<td>6</td>
<td>OFF</td>
<td>6</td>
<td>RSLCK0</td>
<td>7</td>
<td>TSLCK0</td>
</tr>
</tbody>
</table>
ADSP-BF561 EZ-KIT Lite Hardware Reference

PPI Clock Select Switch (SW5)

The SW5 switch controls a clock selection of the PPI interfaces as described in Table 2-7 and Table 2-8.

Table 2-7. PPICLK1 Clock Source Setup

<table>
<thead>
<tr>
<th>SW5 Position 1</th>
<th>SW5 Position 2</th>
<th>PPIxCLK1 Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI0_CKSEL0</td>
<td>PPI0_CKSEL1</td>
<td>27 MHz oscillator (default)</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>ADV7183 clock out</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>Expansion interface</td>
</tr>
</tbody>
</table>

Table 2-8. PPICLK2 Clock Source Setup

<table>
<thead>
<tr>
<th>SW5 Position 3</th>
<th>SW5 Position 4</th>
<th>PPICLK2 Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPI1_CKSEL0</td>
<td>PPI1_CKSEL1</td>
<td>27 MHz oscillator (default)</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>ADV7183 clock out</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>Expansion interface</td>
</tr>
</tbody>
</table>

Test DIP Switches (SW10 and SW11)

Two DIP switches (SW10 and SW11) are located on the bottom of the board. The switches are used only for testing and should remain in the OFF position.

Audio Enable Switch (SW12)

The audio enable switch (SW12) disconnects the audio signals from the processor. The default is all positions ON.
Jumper and DIP Switch Settings

**SPIS1/SPISS Select (SW13)**

The SPIS1/SPISS select switch (SW13) disconnects the SPIS1 and SPISS signals from the board, making them available on the SPI connector (P5). The default is the ON position.

**Video Encoder Clock Select Jumper (JP1)**

The video encoder clock select jumper (JP1) determines the source of the ADV7179 video encoder’s clock. The jumper setting is shown in Table 2-9.

Table 2-9. Video Encoder Clock Select Jumper (JP1)

<table>
<thead>
<tr>
<th>JP1 Position</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 and 2</td>
<td>Input clock for encoder is generated from 27 MHz oscillator (default)</td>
</tr>
<tr>
<td>2 and 3</td>
<td>Input clock for encoder is generated from output clock of decoder. This is used when synchronizing the encoder and decoder clock is required.</td>
</tr>
</tbody>
</table>

**VDDINT Select Jumpers (JP2 and JP3)**

The processor internal voltage (VDDINT) select jumpers (JP2–3) determine the source of the processor’s internal voltage. For the core clock set at 533 MHz and higher, select the on-board external regulator for VDDINT. The jumper settings are shown in Table 2-10.

Table 2-10. Processor Internal Voltage Select Jumpers (JP2 and JP3)

<table>
<thead>
<tr>
<th>JP2</th>
<th>JP3</th>
<th>VDDINT Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not populated</td>
<td>1 and 2 ON</td>
<td>Provided by the on-board external regulator</td>
</tr>
<tr>
<td>Populated</td>
<td>2 and 3 ON</td>
<td>Provided by the processor through the VROUT pins (internal regulator)</td>
</tr>
</tbody>
</table>
UART Loop Jumper (P1)

The UART loop jumper (P1) is for looping the transmit and receive signals. The default is the OFF position.

LEDs and Push Buttons

This section describes functionality of the LEDs and push buttons. Figure 2-3 shows the locations of the LEDs and push buttons.

Figure 2-3. LED and Push Button Locations
LEDs and Push Buttons

Reset Push Button (SW1)

The \texttt{RESET} push button resets all of the ICs on the board. One exception is the USB interface chip (\texttt{U34}). The chip is not being reset when the push button is pressed after the USB cable has been plugged in and communication with the PC has been initialized correctly. Once communication is initialized, the only way to reset the USB is by powering down the board.

Programmable Flag Push Buttons (SW6–9)

Four push buttons, \texttt{SW6–9}, are provided for general-purpose user input. The buttons connect to the programmable flag pins of the processor (\texttt{PF5–8}). The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to “LEDs and Push Buttons” on page 1-14 for more information on how to use PFs when programming the processor. The push button enable switch (\texttt{SW4}) is capable of disconnecting the push buttons from its associated PF (refer to “Push Button Enable Switch (SW4)” on page 2-12). The programmable flag pins and corresponding switches are shown in Table 2-11.

Table 2-11. Programmable Flag Switches

<table>
<thead>
<tr>
<th>Processor Programmable Flag Pin</th>
<th>Push Button Reference Designator</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF5</td>
<td>SW6</td>
</tr>
<tr>
<td>PF6</td>
<td>SW7</td>
</tr>
<tr>
<td>PF7</td>
<td>SW8</td>
</tr>
<tr>
<td>PF8</td>
<td>SW9</td>
</tr>
</tbody>
</table>

Power LED (LED1)

When \texttt{LED1} is lit (green), it indicates that power is being supplied to the board properly.
Reset LED (LED2)

When LED2 is lit, it indicates that the master reset of all major ICs is active.

USB Monitor LED (ZLED3)

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully and you can connect to the processor using an EZ-KIT Lite session. This takes approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver.

When the development software is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

User LEDs (LED5–12, LED13–20)

Sixteen LEDs connect to the processor’s programmable flags. Eight LEDs labeled LED5 through LED12 are controlled by programmable flags PF40 through PF47 (equivalent to PPI0_D15–8). Eight LEDs labeled LED13 through LED20 are controlled by programmable flags PF32 through PF39 (equivalent to PPI1_D15–8). To learn how to use the LEDs, refer to “LEDs and Push Buttons” on page 1-14.

Table 2-12. User LEDs

<table>
<thead>
<tr>
<th>LED Reference Designator</th>
<th>Flag Port Name</th>
<th>LED Reference Designator</th>
<th>Flag Port Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED5</td>
<td>PB40</td>
<td>LED13</td>
<td>PB32</td>
</tr>
<tr>
<td>LED6</td>
<td>PB41</td>
<td>LED14</td>
<td>PB33</td>
</tr>
<tr>
<td>LED7</td>
<td>PB42</td>
<td>LED15</td>
<td>PB34</td>
</tr>
<tr>
<td>LED8</td>
<td>PB43</td>
<td>LED16</td>
<td>PB35</td>
</tr>
<tr>
<td>LED9</td>
<td>PB44</td>
<td>LED17</td>
<td>PB36</td>
</tr>
</tbody>
</table>
Connectors

Table 2-12. User LEDs (Cont’d)

<table>
<thead>
<tr>
<th>LED Reference Designator</th>
<th>Flag Port Name</th>
<th>LED Reference Designator</th>
<th>Flag Port Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED10</td>
<td>PB45</td>
<td>LED18</td>
<td>PB37</td>
</tr>
<tr>
<td>LED11</td>
<td>PB46</td>
<td>LED19</td>
<td>PB38</td>
</tr>
<tr>
<td>LED12</td>
<td>PB47</td>
<td>LED20</td>
<td>PB39</td>
</tr>
</tbody>
</table>

Connectors

This section describes the connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-4.

Figure 2-4. Connector Locations
Expansion Interface (J1–3)

Three board-to-board connector footprints provide signals for most of the processor’s peripheral interfaces. The connectors are located at the bottom of the board. For more information about the interface, see “Expansion Interface” on page 2-8. For the availability and pricing of the J1, J2, and J3 connectors, contact Samtec.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>90-position 0.05” spacing, SMT (J1, J2, J3)</td>
<td>SAMTEC</td>
<td>SFC-145-T2-F-D-A</td>
</tr>
</tbody>
</table>

Mating Connector

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>90-position 0.05” spacing (through hole)</td>
<td>SAMTEC</td>
<td>TFM-145-x1 series</td>
</tr>
<tr>
<td>90-position 0.05” spacing (surface mount)</td>
<td>SAMTEC</td>
<td>TFM-145-x2 series</td>
</tr>
<tr>
<td>90-position 0.05” spacing (low cost)</td>
<td>SAMTEC</td>
<td>TFC-145 series</td>
</tr>
</tbody>
</table>

Audio (J4 and J5)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x2 RCA jacks (J4)</td>
<td>SWITCHCRAFT</td>
<td>PJRSA2X2S01X</td>
</tr>
<tr>
<td>3x2 RCA jacks (J5)</td>
<td>SWITCHCRAFT</td>
<td>PJRSA3X2S01X</td>
</tr>
</tbody>
</table>

Mating Connector

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two channel RCA interconnect cable</td>
<td>MONSTER CABLE</td>
<td>B1100-1M</td>
</tr>
</tbody>
</table>
Connectors

Video (J6)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>3x2 RCA jacks (J6)</td>
<td>SWITCHCRAFT</td>
<td>PJRAS3X2S01X</td>
</tr>
</tbody>
</table>

Power (J7)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 mm power jack (J7)</td>
<td>SWITCHCRAFT</td>
<td>RAPC712X</td>
</tr>
<tr>
<td><strong>Mating Power Supply</strong> (shipped with EZ-KIT Lite)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7V power supply</td>
<td>CUI INC.</td>
<td>DMS070214-P6P-SZ</td>
</tr>
</tbody>
</table>

The power connector supplies DC power to the EZ-KIT Lite board.

RS-232 (P2)

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB9, male, right angle (P2)</td>
<td>TYCO</td>
<td>5747250-4</td>
</tr>
<tr>
<td><strong>Mating Assembly</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2m female-to-female cable</td>
<td>DIGI-KEY</td>
<td>AE1016-ND</td>
</tr>
</tbody>
</table>
SPORT1 (P3)

The SPORT1 connector is linked to a 20-pin connector. The connector’s pinout can be found in “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDC header</td>
<td>FCI</td>
<td>68737-420HLF</td>
</tr>
</tbody>
</table>

SPI (P5)

The SPI connector is linked to a 12-pin connector. The connector’s pinout can be found in “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDC header</td>
<td>SULLINS</td>
<td>GEC06DAAN</td>
</tr>
</tbody>
</table>

USB Debug Agent Connector (ZJ1)

The USB debug agent connector is the connecting point for the JTAG USB debug agent interface. The JTAG header (ZJ4) should not be used whenever ZJ1 and its mating cable are used to communicate to the processor via CCES or VisualDSP++.

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDC socket</td>
<td>DIGI-KEY</td>
<td>S4207-ND</td>
</tr>
</tbody>
</table>
Connectors

JTAG (ZP4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

- Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

- When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.
A ADSP-BF561 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to “ADSP-BF561 EZ-KIT Lite Schematic” on page B-1.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Qty.</th>
<th>Description</th>
<th>Reference Designator</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>74LVC14A SOIC14</td>
<td>U47</td>
<td>TI</td>
<td>74LVC14AD</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>IDT74FCT3244 APY SSOP20</td>
<td>U13, U30</td>
<td>IDT</td>
<td>IDT74FCT3244APYG</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>12,288MHZ OSC003</td>
<td>U16</td>
<td>EPSON</td>
<td>SG-8002CA MP</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>NDS8434A SO-8</td>
<td>U29</td>
<td>FAIRCHILD</td>
<td>NDS8434A</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>MT48LC16M16 A2TG-75 TSOP54</td>
<td>U32-33</td>
<td>MICRON</td>
<td>MT48LC16M16A2P-75</td>
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<td>6</td>
<td>1</td>
<td>27MHZ OSC005</td>
<td>U17</td>
<td>EPSON</td>
<td>SG-8002CA MP</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>IDT2305-1DC SOIC8</td>
<td>U19-20</td>
<td>INTEGRATED SYS</td>
<td>ICS9112AM-16LFT</td>
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<td>8</td>
<td>1</td>
<td>SN74LVC1G32 SOT23-5</td>
<td>U10</td>
<td>TI</td>
<td>SN74LVC1G32DBVR</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>30MHZ OSC003</td>
<td>U14</td>
<td>EPSON</td>
<td>SG-8002CA MP</td>
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<td>BF561 M29W640D &quot;U27&quot;</td>
<td>U27</td>
<td>ST MICRO</td>
<td>M29W640DT 90N6E</td>
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<tr>
<td>11</td>
<td>2</td>
<td>FDC658P SOT23-6</td>
<td>U28, U49</td>
<td>FAIRCHILD</td>
<td>FDC658P</td>
</tr>
<tr>
<td>Ref.</td>
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<td>Description</td>
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<td>Manufacturer</td>
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<td>1</td>
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<td>U46</td>
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<tr>
<td></td>
<td></td>
<td>SOIC8</td>
<td></td>
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<td>1</td>
<td>ADP3338AKCZ-33 SOT-223</td>
<td>VR3</td>
<td>ANALOG DEVICES</td>
<td>ADP3338AKCZ-3.3-RL</td>
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<tr>
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<td>1</td>
<td>ADP3339AKCZ-5 SOT-223</td>
<td>VR1</td>
<td>ANALOG DEVICES</td>
<td>ADP3339AKCZ-5-R7</td>
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<tr>
<td>15</td>
<td>1</td>
<td>ADP3336ARMZ MSOP8</td>
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<td>ANALOG DEVICES</td>
<td>ADP3336ARMZ-REEL7</td>
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<td>1</td>
<td>10MA AD1580BRTZ SOT23D</td>
<td>D1</td>
<td>ANALOG DEVICES</td>
<td>AD1580BRTZ-REEL7</td>
</tr>
<tr>
<td>17</td>
<td>4</td>
<td>ADG752BRTZ SOT23-6</td>
<td>U22-23,U25-26</td>
<td>ANALOG DEVICES</td>
<td>ADG752BRTZ-REEL</td>
</tr>
<tr>
<td>18</td>
<td>3</td>
<td>AD8061ARTZ SOT23-5</td>
<td>U1-3</td>
<td>ANALOG DEVICES</td>
<td>AD8061ARTZ-R2</td>
</tr>
<tr>
<td>19</td>
<td>1</td>
<td>ADM3202ARNZ SOIC16</td>
<td>U21</td>
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<td>ADM3202ARNZ</td>
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<tr>
<td>20</td>
<td>8</td>
<td>AD8606ARZ SOIC8</td>
<td>U5-7,U9,U11-12, U18,U24</td>
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<td>AD8606ARZ</td>
</tr>
<tr>
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<td>1</td>
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<td>U15</td>
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<td>AD1836AASZ</td>
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<td>ADV7179KCPZ</td>
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<td>ADV7183BKSTZ</td>
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<td>ADP1864AUJZ SOT23-6</td>
<td>VR5-6</td>
<td>ANALOG DEVICES</td>
<td>ADP1864AUJZ-R7</td>
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<tr>
<td>26</td>
<td>5</td>
<td>RUBBER FOOT</td>
<td>M1-5</td>
<td>MOUSER</td>
<td>517-SJ-5018BK</td>
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</tbody>
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## ADSP-BF561 EZ-KIT Lite Bill Of Materials

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Qty.</th>
<th>Description</th>
<th>Reference Designator</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>1</td>
<td>PWR 2.5MM_JACK CON005</td>
<td>J7</td>
<td>SWITCH-CRAFT</td>
<td>RAPC712X</td>
</tr>
<tr>
<td>28</td>
<td>1</td>
<td>RCA 2X2 CON013</td>
<td>J4</td>
<td>SWITCH-CRAFT</td>
<td>PJRAS2X2S01X</td>
</tr>
<tr>
<td>29</td>
<td>5</td>
<td>MOMENTARY SWT013</td>
<td>SW1,SW6-9</td>
<td>PANASONIC</td>
<td>EVQ-PAD04M</td>
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<td>3</td>
<td>.05 45X2 CON019</td>
<td>J1-3</td>
<td>SAMTEC</td>
<td>SFC-145-T2-F-D-A</td>
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<td>3</td>
<td>DIP6 SWT017 SW2,SW4,SW10</td>
<td>SW13</td>
<td>CTS</td>
<td>218-6LPST</td>
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<td>J5-6</td>
<td>SWITCH-CRAFT</td>
<td>PJRAS3X2S01X</td>
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<td>4</td>
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<tr>
<td>35</td>
<td>1</td>
<td>IDC 2X1 IDC2X1</td>
<td>P1</td>
<td>FCI</td>
<td>90726-402HLF</td>
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<tr>
<td>36</td>
<td>1</td>
<td>IDC 2X1 IDC2X1</td>
<td>JP2</td>
<td>FCI</td>
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<td>2</td>
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<td>JP1,JP3</td>
<td>FCI</td>
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<tr>
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<td>1</td>
<td>IDC 10X2 IDC10X2</td>
<td>P3</td>
<td>BURG-FCI</td>
<td>54102-T08-10LF</td>
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<td>4</td>
<td>IDC 2PIN_JUMPER_SHORT</td>
<td>SJ1-4</td>
<td>DIGI-KEY</td>
<td>S9001-ND</td>
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<td>DB9 9PIN DB9M</td>
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<tr>
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<td>5A RESETABLE FUS005</td>
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</tr>
<tr>
<td>43</td>
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## ADSP-BF561 EZ-KIT Lite Bill Of Materials

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## ADSP-BF561 EZ-KIT Lite Bill Of Materials

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ADSP-BF561 EZ-KIT Lite Schematic
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com.

All USB interface circuitry is considered proprietary and has been omitted from this schematic.
(WHITE) OUT (RED) IN

<table>
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<th>AVIN4</th>
<th>AVIN5</th>
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| Composite Video | Component 
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S Video
Differential Component Video
Composite Video

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<tr>
<th>Node</th>
<th>Description</th>
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<tr>
<td>CON024</td>
<td>J6</td>
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Note: Signal Names in brackets refer to ADV7183KST

SW2: Video Sync Signals and Encoder Enable Select
Default = OFF, OFF, OFF, OFF, OFF, ON

Position | Function
--- | ---
1-5 | Connect video sync signals to DSP
6 | OFF = Encoder digital interface always disabled
**Title:** ADS-PF561 EZ-KIT LITE

**Reset, Push-Button Switches, UART**

**Position:**

- **1-4:** Connects the push buttons to the Programmable Flags of the DSP. Useful if using the PFs for another purpose.
- **5-6:** OFF, OFF = AD1836A -> TDM Mode
  - ON, ON = AD1836A -> I2S Mode

**NOTE:** Remove R192 when populating R191 and R184.
I  INDEX

Numerics
2-wire interface (TWI) mode, 1-15, 1-17, 2-12

A
A25-2 address bus pins, 2-3
AD1836A audio codecs, 1-15, 2-3, 2-4, 2-12
ADV7179 video encoders
  video interface, 1-16
  clock select jumper (JP1), 2-14
  configuration switch (SW2), 2-10
  PPI1 interface, 2-6, 2-7
  programmable flags, 2-4
  reset, 1-16
ADV7183A video decoders
  video interface, 1-16
  clock select switch (SW5), 2-13
  configuration switch (SW2), 2-10
  PPI0 interface, 2-6, 2-7
  programmable flags, 2-4
  reset, 1-16
AIN1/4/5 analog video channels, 2-7
AMS0 memory select pins, 1-12
analog
  audio interface, See SPORT0
  video interface, See video interface architecture, of this EZ-KIT Lite, 2-2
ASYNC (asynchronous memory control) banks, 1-11

audio
  codecs, See AD1836A
  connectors (J4-5), 2-19
  enable switch (SW12), 2-13
  interface, See SPORT

B
bill of materials, A-1
BMODE1-0 (boot mode select) pins, 2-12
board design database, 1-17
board schematic (ADSP-BF561), B-1
boot mode select switch (SW3), 2-11

C
clock select switch, of PPIs (SW5), 2-13
codecs, See AD1836A
configuration, of this EZ-KIT Lite, 1-3
connectors
  diagram of locations, 2-18
  DB9 (UART), xii, 2-8
  J1-3 (expansion), 2-8, 2-19
  J4-5 (audio), 2-19
  J6 (video), 2-20
  J7 (power), 2-20
  P2 (RS-232), xi, 2-20
  P3 (SPORT1), 2-3, 2-21
  P5 (SPI), 2-3, 2-14, 2-21
  P9 (SPORT0), 2-21
  ZJ1 (USB), 1-5, 2-21
  ZP4 (JTAG), 2-22
contents, of this EZ-KIT Lite package, 1-2
Index

core
  clock rate, 2-2, 2-14
  frequency, 1-14
  voltage, 2-2

D
DAC A/B/C analog audio channels, 2-7
DB9 (UART) connector, xii, 2-8, 2-20
default configuration, of this EZ-KIT Lite, 1-3
DIP switches
diagram of locations, 1-3, 2-10
SW10-11 (test), 2-13
SW2 (video config), 1-16, 2-8
SW4 (push button enable), 1-15, 2-12, 2-16

E
EBIU
  address bus (A25-2) pins, 2-3
  control signals, 2-3, 2-8
  EBIU_SDBCTL register, 1-13, 1-14
  EBIU_SDGCTL register, 1-13, 1-14
  EBIU_SDRRC register, 1-13, 1-14
evaluation license
  CCES, 1-10
  example programs, 1-18
  expansion interface, 2-3, 2-8, 2-19
  external bus interface unit, See EBIU
  external memory
  See also flash memory, SDRAM
  memory map, 1-11
  via JTAG, 2-9
EZ-KIT Extender boards, 2-6

F
features, of this EZ-KIT Lite, xi
FIELD (ADV7183A) control signal, 2-4, 2-8, 2-11
FIO0_FLAG_D registers, 1-15
FIO2_DIR register, 1-14
FIO2_FLAG_C/D/S/T registers, 1-14
flag pins, See programmable flags (PFs)
  flash memory, 2-3
  ports (PB47-32), 2-17
  frequency, 1-13, 1-14

G
general-purpose IO pins, 1-14, 2-4, 2-12, 2-16
GND signals, 2-8

H
HSYNC signals, 2-6, 2-7

I
input clocks, 1-16, 2-2, 2-5, 2-7
installation, of this EZ-KIT Lite, 1-8
  CCES, 1-4
  interfaces, See video, SPORT0, SPI, expansion
  internal memory
  See also SRAM
  map of the processor, 1-12
  internal voltage (VDDINT), 2-14
  IO voltage, 2-2
J

JTAG
connector (ZP4), 2-9, 2-22
emulation port, 2-9

jumpers
JP1 (ADV7179 clock select), 2-14
JP2-3 (VDDINT source select), 2-14
P1 (UART loop), 2-15

L

LEDs
diagram of locations, 1-3, 2-15
LED13-20 (PF39-32), 1-14, 2-5, 2-17
LED1 (power), 2-16
LED2 (chip reset), 2-17
LED5-12 (PF47-40), 1-14, 2-5, 2-17
ZLED3 (USB monitor), 1-8, 2-17

M

Media Instruction Set Computing (MISC), ix
memory
map, of this EZ-KIT Lite, 1-11
select pins, See AMS2-0, SMS0
Micro Signal Architecture (MSA), ix

N

notation conventions, xviii

O

\overline{OE} (ADV7183A) signal, 2-4, 2-10
oscillators, 2-6, 2-7, 2-13

P

P3 (SPORT0) connector, 2-3
package contents, 1-2

parallel peripheral interfaces (PPIs), 1-17, 2-5, 2-10, 2-19
See also PPI0, PPI1
PB47-32 flash ports, 2-17
power
connector (J7), 2-20
LED (LED1), 2-16
PPI0_D15-8 bits, 1-14, 2-5
PPI0 interface
to ADV7183A decoder, 1-16, 2-7
clock select pin, 2-6, 2-7
D15-8 bits, 2-17
D7-0 bits, 2-6
SYNC2-1 signals, 2-6, 2-8, 2-11
PPI0_SYNC2-1 synchronization signals, 2-8, 2-11
PPI1_D15-8 bits, 1-14, 2-5
PPI1 interface
to ADV7179 video encoder, 1-16, 2-7
clock select pin, 2-7
D15-8 bits, 2-17
D7-0 bits, 2-6, 2-7
HSYNC signals, 2-7
SYNC2-1 signals, 2-7, 2-11
PPI clock select switch (SW5), 1-16, 2-13
PPIxCLK signals, 2-13
product information, xvi
programmable flags (PFs)
connections, 2-4
PF0 (video serial clock), 1-17, 2-4
PF1 (video serial data), 1-17, 2-4
PF2 (DV7183A enable), 1-17, 2-4, 2-10, 2-11
PF3 (DV7183A field pin), 2-4, 2-8, 2-11
PF4 (AD1836A SPI select), 1-15, 2-3, 2-4
PF13 (DV7183A reset), 1-16, 2-4
PF14 (DV7179 reset), 1-16, 2-5
PF15 (AD1836A reset), 1-16, 2-5
## Index

**programmable flags (PFs) (continued)**
- PF16-20 (SPORT0), 2-5
- PF21-25 (SPORT1), 2-5
- PF26-27 (UART), 2-5
- PF28-29 (SPORT0 serial clock), 2-5
- PF30-31 (SPORT1 serial clock), 2-5
- PF39-40 (LED13-20), 2-5
- PF47-48 (LED5-12), 1-14, 2-5
- PF5-8 (general-purpose IO), 1-14, 2-4, 2-12, 2-16
- pull-down resistors, 1-16
- pull-up resistors, 2-11
- push buttons
  - See also switches by name (SWx), 1-14
  - diagram of locations, 2-15
  - enable switch (SW4), 2-12

**S**
- schematic, of ADSP-BF561 EZ-KIT Lite, B-1
- SDRAM memory
  - connections, 2-3
  - control registers, 1-12
  - core MMRs, 1-12
  - data bank B SRAM, 1-12
  - data banks A, B SRAM, 1-12
  - default settings, 1-13
  - instruction SRAM, 1-12
  - instruction SRAM/CACHE, 1-12
  - optimum settings, 1-14
  - reserved, 1-12
  - scratch pad SRAM, 1-12
  - system MMRs, 1-12
- serial
  - clock pin (SCL), 1-17, 2-4
  - data pin (SDAT), 1-17
  - video data, 2-4
  - serial peripheral interface (SPI), 2-3, 2-4, 2-14
  - setup, of this EZ-KIT Lite, 1-4
  - SMS0 memory select pins, 1-12
  - SPIS1/SPISS signals, 2-14
- SPORT
  - audio interface, 2-3
  - SPORT0
    - audio interface, xii, 1-15
    - connector (P3), 2-21
    - receive data secondary pin (PF20), 2-5
    - receive frame sync pin (PF19), 2-5
    - receive serial clock pin (PF28), 2-5
    - transmit data primary pin (PF18), 2-5
    - transmit data secondary pin (PF17), 2-5
    - transmit frame sync pin (PF16), 2-5
    - transmit serial clock pin (PF29), 2-5
  - SPORT1
    - receive data secondary pin (PF25), 2-5
    - receive frame sync pin (PF24), 2-5
    - receive serial clock pin (PF29), 2-5
    - transmit data primary pin (PF23), 2-5
    - transmit data secondary pin (PF22), 2-5
    - transmit frame pin (PF21), 2-5
    - transmit serial clock pin (PF31), 2-5

---

ADSP-BF561 EZ-KIT Lite Evaluation System Manual
Index

SRAM data bank A, 1-12
startup, of this EZ-KIT Lite, 1-8
   CCES, 1-4
SW10-11 (test) DIP switches, 2-13
SW12 (audio enable) switch, 2-13
SW13 (SPIS1/SPISS select) switch, 2-14
SW1 (reset) push button, 2-16
SW2 (video config) DIP switch, 1-16, 2-6, 2-7, 2-8, 2-11
SW3 (boot mode) switch, 2-11
SW4 (push button enable) DIP switch, 1-15, 2-12, 2-16
SW5 (PPI clock select) switch, 1-16, 2-6, 2-13
SW6-9 (general input) push buttons, 1-14, 2-4, 2-12, 2-16
synchronous dynamic random access memory, See SDRAM system
architecture, of EZ-KIT Lite, 2-2
clock (SCLK), 1-13

T
technical support, xv
test DIP switches (SW10-11), 2-13
TFS0 signal, 1-15, 2-12
time-division multiplexed (TDM) mode, 1-15
timers11-8, 2-6
timers7-0, 2-4
TSCLK0 signal, 1-15, 2-12

U
UART
   loop jumper (P1), 2-15
   port, xii, 2-8
   transmit/receive pins (PF26-27), 2-5
universal asynchronous
   receiver/transmitter, See UART port

USB
cable, 1-2
default agent connector (ZJ1), 2-21
interface, 2-9, 2-16, 2-22
monitor LED (ZLED3), 2-17
user LEDs (LED5-12, LED13-20), 2-17

V
VDDINT signal, 2-14
very-long instruction word (VLIW), ix
video
   channels, 2-7
   configuration switch (SW2), 2-10
   connector (J6), 2-20
   control signals, 2-7, 2-8
   decoders, See ADV7183A
   encoders, See ADV7179
   input (PPI0), 2-7
   interface, 1-16
   output (PPI1), 2-7
VisualDSP++
   environment, 1-8
   VROUT pins, 2-14
   VSYNC signals, 2-6, 2-7