Solving Power-Management Problems with a Single Chip that Handles up to 7 Channels of Sequencing, Monitoring, and Supervision

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The design of systems with multiple supply voltages is commonplace today. In such systems as Internet routers, digital subscriber-line access multiplexers (DSLAMs), base stations, and servers, the sequencing and supervision of their multiple supplies has grown in importance. The ADM1060 *supervisor/sequencer* from Analog Devices greatly simplifies this task by providing multiple supply supervisors, sequencing logic, and multiple-output drivers, in a single 28-lead TSSOP device—ideal for applications where board space is at a premium. The configuration of these multiple functions is easily programmed using an intuitive *graphical user interface* (GUI), also provided by Analog Devices.

The increasing number of user demands on designers of the backplanes, line-cards, and blades used in infrastructure and server systems is making the design task increasingly difficult. Customers want more channels at higher data rates for less money. They also require a much higher level of reliability than before: An uptime of 99.999%, commonly known as "*five*-9's *reliability*" (analogous to two minutes of down time per year), is now a basic requirement. Yet these more complex, more reliable boards must still fit in the same central-office and server form factors as before. Power budgets for these systems have not necessarily increased either, so greater attention must now be paid to power consumption.

The additional bandwidth, expressed in both channel count and speed, has resulted in a proliferation of many new-generation microprocessors, DSP devices, FPGAs, and CPLDs. The cores of these devices run at much lower voltages than the traditional 3.3 V or 5 V (for example, 1.2 V, 1.5 V, 1.8 V, and 2.5 V are common core-supply levels). Yet I/O protocols dictate that 3.3-V and 5-V supplies still be provided. In fact, some designs may require a 12-V supply; others need termination voltages as low as 0.75 V; and there are even cases where *negative* supplies are required for op amp rails.

It is not uncommon for many, if not all, of these supplies to be needed on a single board. The requirement could easily be for six, seven, or more supplies. The sequence in which the supplies turn on can be critical to the reliable operation of the system. A good rule of thumb might be to start with the highest supply first and work downwards; but this is not always the case. For instance, some DSP manufacturers recommend that the core of their device be powered up before the I/O, while others recommend the *opposite*. Given the complexity of the PCBs being designed, the truth is that it may be difficult to determine what the optimal power-up sequence is without first designing, building, and testing the board. This "trial-and-error" approach can prove costly, both in terms of manufacturing costs (multiple board-design cycles, or *spins*) and in time to market.

The current discrete approach to supply sequencing, using reset generators, FET drivers, and RC time constants (a typical implementation is shown in Figure 1)—while adequate for a system requiring two or three supplies, becomes very cumbersome when the number rises to six or seven. Another problem is that accurate reset generators have fixed threshold voltages. If—as can be the case with ASIC designs—a supply voltage must be tweaked to a nonstandard value in order to provide maximum performance, a reset generator with the revised threshold may not exist. Also, designs of this nature require the power designer's best guess (albeit an educated one) as to the sequence required. If the guess proves wrong, it is difficult to rectify the issue without a board spin. Further, as the population density of PCBs increases, real estate becomes an issue and a multi-component discrete solution becomes unattractive. Finally, it is not easy to design a power-down sequence, using the same simple reset generators with fixed timeouts and open-drain outputs.

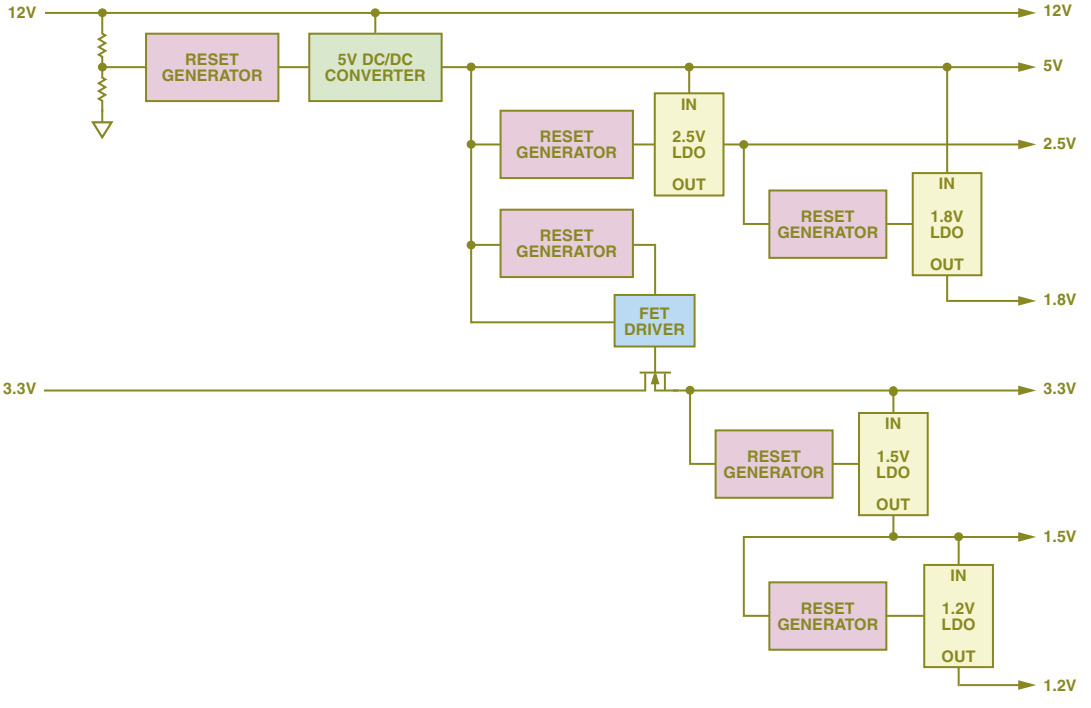

Figure 1. Discrete implementation for sequencing seven supplies.

The solution to be described here is a *single IC*, which provides a total voltage-management solution and encompasses all of the functionality of the discrete design shown in Figure 1. The device needs to—and does—go further, however, in providing the flexibility to change its configuration easily as required. If the alteration of a reset threshold, the power-up sequence, the power-down sequence, and the watchdog timeout on a processor clock can be altered without laying out the hardware again, the power designer's task is made infinitely easier. Naturally, a single IC (with minimal external components) also addresses the key issue of board real estate. Reduced design time also means reduced time-to-market, since the power designer can implement a design more quickly—with confidence that, if necessary, it can be altered later without a change in hardware.

The Analog Devices ADM1060 *multi-supply supervisory circuit* is such a device. It is a total voltage-management solution in a single small 28-lead TSSOP package. It requires as few as two external components (two decoupling capacitors), making it ideal for applications where board space is at a premium.

The ADM1060 can supervise up to seven supplies. All of the supervisors on the chip use window comparators, so that both overvoltage and undervoltage supply faults can be detected on each of the supply fault input pins. One of the supply fault detectors can supervise a supply up to 14.4 V (analogous to a 12-V supply being overranged by +20%). Four of the supervisors can detect faults from 0.6 V to 6 V (analogous to a 5-V supply being overranged by +20%). The other two supervisors can be used to monitor negative supplies down to –6 V. If supervision of a negative supply is not required, these two pins can be used to monitor supplies up to +6 V. Any threshold voltage within the above ranges can be programmed with 8-bit resolution. Thus, if an ASIC runs optimally with a nonstandard voltage—i.e., not 1.2 V, 1.5 V, 1.8 V, etc., the ADM1060 can be programmed around the modified supply voltage with an accurate fault-detection window. The hysteresis of these comparators is programmable digitally, allowing the user to control the level of noise immunity required.

The ADM1060 does not need a dedicated power pin. The device uses an arbitration scheme to power itself from any one of five of the supply-fault input pins (the negative supply input pins are not used here). Whichever supply is highest is used to power the device. If the highest supply should fail, the ADM1060 seamlessly switches over to the next highest supply to power itself. Thus, even in a failing system, the device continues to be powered, allowing it to maintain supervision of the supplies for as long as possible. For example, it could cause a controlled power-down sequence to be initiated. The ADM1060 requires a minimum of 3.0 V (on one of the supply input pins) to power the device.

The ADM1060 also provides four *general-purpose inputs* (GPI's). These are logic inputs (TTL- or CMOS-compatible) that enable the user to apply control signals, such as POWER_OK, RESET, or MANUAL RESET, and use these to control the sequence in which the supplies turn on. Note that these inputs can also be used to take signals from external supervisory chips, if more than seven supplies need to be supervised and included in the sequencing. A watchdog timer is also included. This circuit is used to ensure that a processor clock continues to toggle (transition from low to high or high to low).

The logical core of the device is the *programmable logic-block array* (PLBA), combined with the *programmable delay block* (PDB). These blocks enable the ADM1060 to sequence the turn-on of the supplies' programmable time delays in the chosen order. A set of different time delays can be programmed for a power-down sequence. For instance, a supply may be required to power up 100 ms after the previous supply—but to turn off instantly if a fault occurs.

The ADM1060 makes available nine output drivers. These *programmable driver outputs* (PDOs) can be used as logic-control signals, such as chip-enable, LDO- (dc/dc brick-)output enable, or simply as status signals, such as POWER_GOOD, or RESET. The output pins all have an open-drain configuration, allowing the user to connect an external resistor to pull the pin up to the desired voltage. However, it is likely that the pull-up voltage is one that is being supervised at one of the inputs of the device and is available on-chip. Therefore, the ADM1060 features a bank of internal pull-up resistors, which can be connected to the pull-up voltage without external components. This is of course significant where minimal board space is available. Four of the output drivers can also provide a high-voltage gate drive to turn on an NMOS FET, which may be placed in a supply path. In this option, a 12-V charge-pump voltage is provided at the output pin.

Communication with the ADM1060 is via an industry-standard 2-wire interface (SMBus). The user can set up the features described using the intuitive GUI provided by Analog Devices. This programming can be done offline, using the Evaluation Kit, or in-system, using a 3-pin header cable (data, clock, and GND). Both are available from Analog Devices. Once satisfied with the configuration, the user can store this in nonvolatile memory, so that each time the device is subsequently powered up, the same configuration is downloaded and set up in the device. An example window from the GUI is shown in Figure 2.

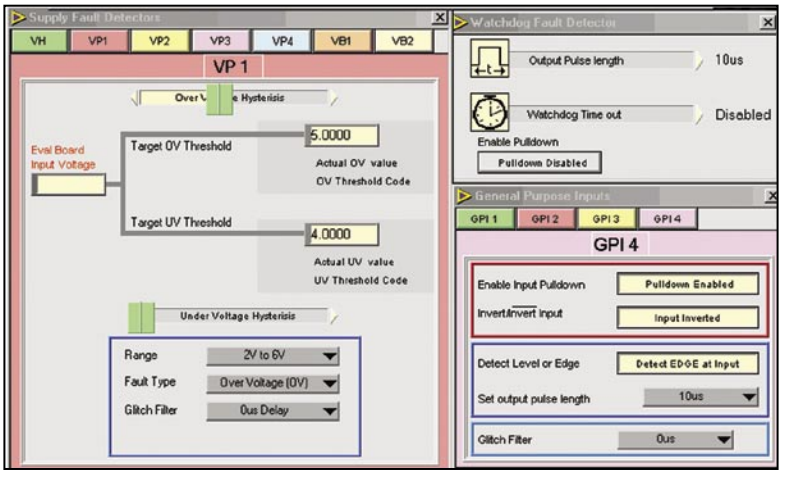

Figure 2. ADM1060 graphical user interface (GUI).

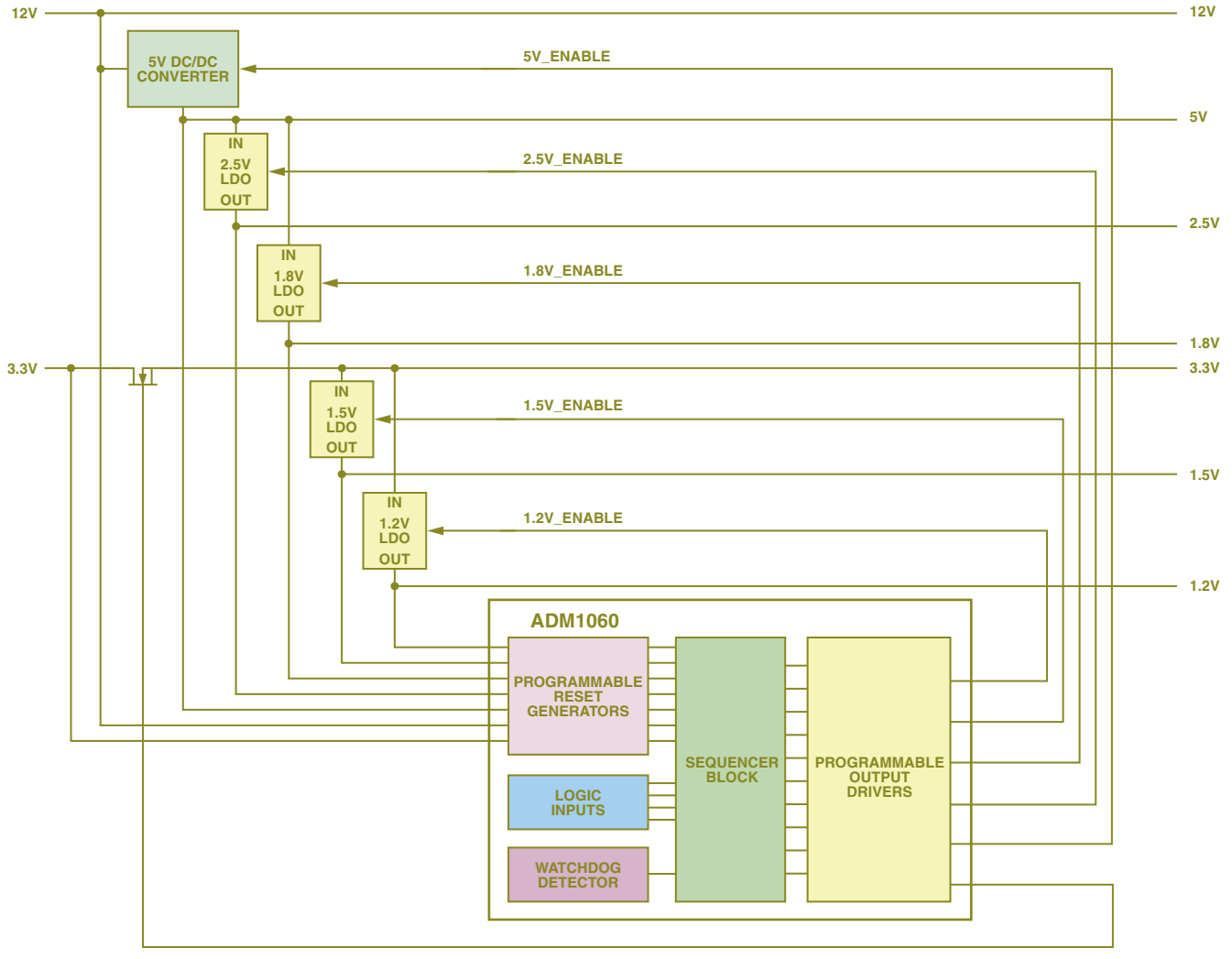

Figure 3. Sequencing the same seven supplies using a single ADM1060.

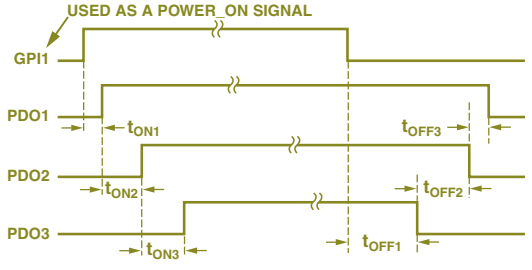

Figure 4. Controlled power on/off sequence using the ADM1060.

Providing the same seven supplies outlined in the discrete design of Figure 1, a sequence could be implemented using a single ADM1060 as shown in Figure 3.

Another very powerful feature of the ADM1060, not easily replicated in a discrete design, is the ability to configure a controlled power-down sequence. Again, using the software provided, a sequence like that shown in Figure 4 can be configured.

CONCLUSION

The requirement for multiple voltages on a single PCB has resulted in a difficult supply sequencing problem for power designers. With six, seven, or more voltages required, discrete solutions are unwieldy and impractical. The ADM1060 from Analog Devices provides a powerful and flexible solution, making the configuration of supply thresholds, logic inputs, and supply sequencing a straightforward *software* design—rather than a costly and error-prone hardware design.