

**DS28E30****1-Wire ECDSA Secure Authenticator****General Description**

The DS28E30 provides a highly secure and easily deployed turnkey authentication solution based on the FIPS-186 ECDSA standard. The secure authenticator combines ECDSA challenge and response authentication with secured EEPROM for the storage of the keys and user data.

The device provides a core set of cryptographic tools derived from integrated blocks including an asymmetric hardware engine, a true random number generator (TRNG), 3Kb of secure EEPROM, a decrement-only counter, and a unique 64-bit ROM identification number (ROM ID). The ECC public/private key capabilities operate from the NIST-defined P-256 curve to provide a FIPS 186-compliant ECDSA signature generation function to support a bidirectional asymmetric key authentication model. The unique ROM ID is used as a fundamental input parameter for cryptographic operations and serves as an electronic serial number within the application. In addition, authenticity of the chip can be verified with a Maxim-provided public key certificate. The device communicates over the single-contact 1-Wire® bus at overdrive speed. The communication follows the 1-Wire protocol with the ROM ID acting as a node address in the case of a multidevice 1-Wire network.

**Applications**

- Battery Authentication and Charge Cycle Tracking
- Medical Tools/Accessories Authentication and Calibration
- Accessory and Peripheral Secure Authentication

**Benefits and Features**

- Robust Countermeasures Protect Against Security Attacks
  - All Stored Data Cryptographically Protected from Discovery
- ECC P-256 Secure Compute Engine
  - Preprogrammed and Write-Protected ECC P-256 Key Pair
  - FIPS 186-4 Compliant ECDSA for Strong Challenge/Response Authentication
  - ECDSA Authenticated R/W of Configurable Memory
- TRNG Used for Secure ECDSA Nonces
- Supplemental Features Enable Easy Integration into End Applications
  - 17-Bit, One-Time Settable, Nonvolatile Decrement-Only Counter with Authenticated Read
  - 3Kb of Secure EEPROM for User Data, Keys, Certificate, and Secure Counter
  - Unique and Unalterable Factory-Programmed, 64-Bit Identification Number (ROM ID)
  - Authenticity Verification with ECDSA Using Preprogrammed Maxim Certificate
  - Advanced 1-Wire Protocol Minimizes Interface to Single Contact
  - Full-Time Overdrive Communication Speed
  - Operating Range: -40°C to +85°C, 1.62V to 5V
  - 4-Bump WLP and 6-Pin TSOC Packages
  - 3.5µA (typ) Input Load Current
  - High ESD Immunity of 1-Wire Pin: ±8kV Human Body Model (HBM), typ

**Request DS28E30  
Security User Guide**

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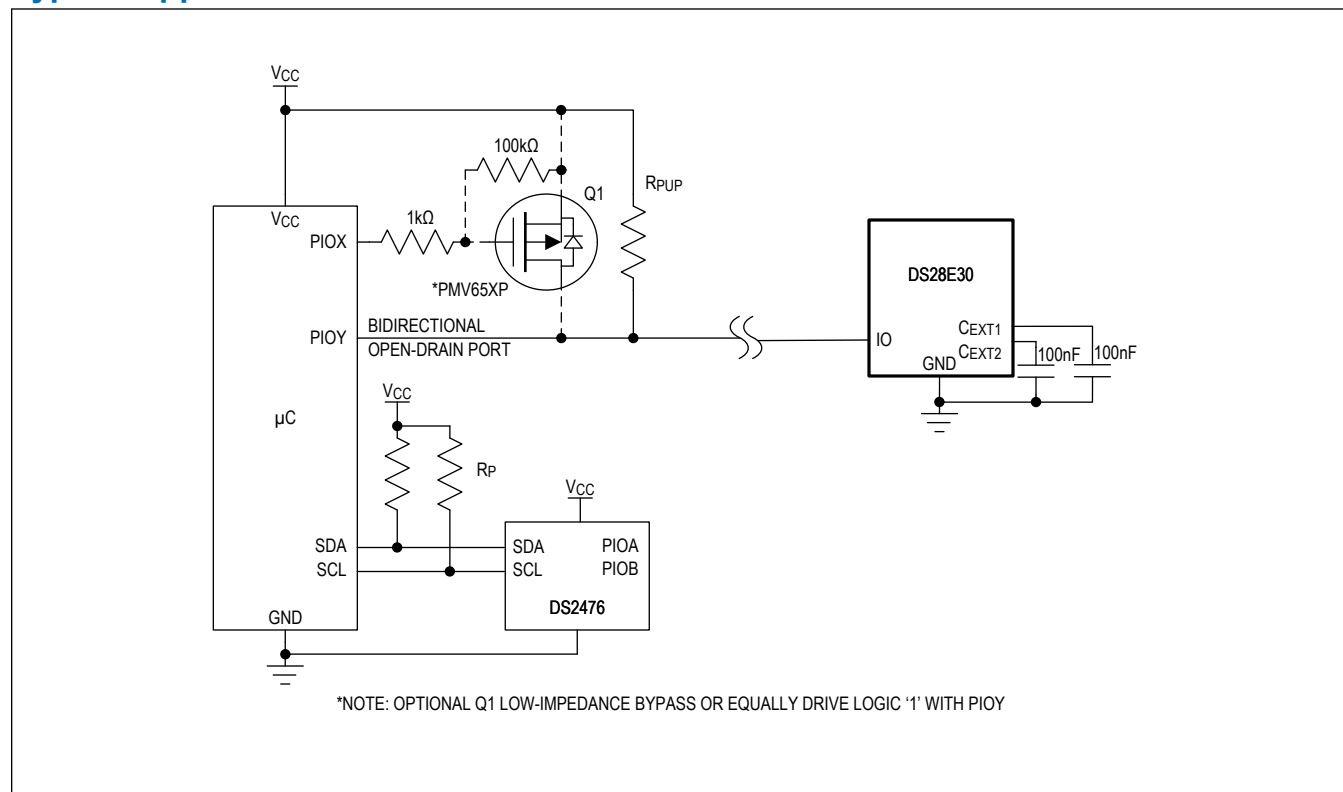
[Ordering Information](#) appears at end of data sheet.

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## Typical Application Circuit



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## Absolute Maximum Ratings

V <sub>DD</sub> to GND.....	-0.5V to 5.5V	Junction Temperature .....	+150°C
Any Pin to GND except V <sub>DD</sub> (Any Pin to GND except V <sub>DD</sub> ) -0.3V to V <sub>DD</sub> + 0.3V		Storage Temperature Range .....	-40°C to +125°C
Operating Temperature Range .....	-40°C to +85°C	Lead Temperature (soldering, 10s).....	+300°C
		Soldering Temperature (reflow) .....	+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 4 WLP

Package Code	Z41A1+1
Outline Number	<a href="#">21-100548</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	95.15°C/W
Junction to Case ( $\theta_{JC}$ )	N/A

### 6 TSOC

Package Code	D6+1
Outline Number	<a href="#">21-0382</a>
Land Pattern Number	<a href="#">90-0321</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	166°C/W
Junction to Case ( $\theta_{JC}$ )	37°C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	126.7°C/W
Junction to Case ( $\theta_{JC}$ )	37°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

(Limits are 100% tested at T<sub>A</sub> = +25°C and T<sub>A</sub> = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>IO PIN: GENERAL DATA</b>						
1-Wire Pullup Voltage	V <sub>PUP</sub>	System requirement	1.62		5.25	V
1-Wire Pullup Resistance	R <sub>PUP</sub>	V <sub>PUP</sub> = 1.62V to 2.7V ( <a href="#">Note 1</a> )	300		750	$\Omega$
		V <sub>PUP</sub> = 2.7V to 5.25V ( <a href="#">Note 1</a> )	300		2200	
Input Capacitance	C <sub>IO</sub>	( <a href="#">Note 1</a> , <a href="#">Note 2</a> )		0.1 + C <sub>CEXT1</sub>		nF
Capacitor External 1	C <sub>EXT1</sub>		100			nF

## Electrical Characteristics (continued)

(Limits are 100% tested at  $T_A = +25^{\circ}\text{C}$  and  $T_A = +85^{\circ}\text{C}$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitor External 2	$C_{EXT2}$		100			nF
Input Load Current	$I_L$	IO pin at $V_{PUP}$		3.5	11	$\mu\text{A}$
High-to-Low Switching Threshold	$V_{TL}$	( <a href="#">Note 3</a> , <a href="#">Note 4</a> )		$0.65 \times V_{PUP}$		V
Input Low Voltage	$V_{IL}$	( <a href="#">Note 5</a> )			$0.18 \times V_{PUP}$	mV
Low-to-High Switching Threshold	$V_{TH}$	( <a href="#">Note 3</a> , <a href="#">Note 6</a> )		$0.75 \times V_{PUP}$		V
Switching Hysteresis	$V_{HY}$	( <a href="#">Note 3</a> , <a href="#">Note 7</a> )		0.3		V
Output Low Voltage	$V_{OL}$	$I_{OL} = 4\text{mA}$ ( <a href="#">Note 8</a> )			0.4	V
<b>IO PIN: 1-Wire INTERFACE</b>						
Recovery Time ( <a href="#">Note 9</a> )	$t_{REC}$		5			$\mu\text{s}$
Time Slot Duration ( <a href="#">Note 10</a> )	$t_{SLOT}$		11			$\mu\text{s}$
<b>IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE</b>						
Reset Low Time	$t_{RSTL}$	System requirement	48		80	$\mu\text{s}$
Reset High Time ( <a href="#">Note 11</a> )	$t_{RSTH}$		48			$\mu\text{s}$
Presence-Detect Sample Time ( <a href="#">Note 12</a> )	$t_{MSP}$		7		10	$\mu\text{s}$
<b>IO PIN: 1-Wire WRITE</b>						
Write-Zero Low Time ( <a href="#">Note 13</a> )	$t_{W0L}$		6		16	$\mu\text{s}$
Write-One Low Time ( <a href="#">Note 13</a> )	$t_{W1L}$		0.25		2	$\mu\text{s}$
<b>IO PIN: 1-Wire READ</b>						
Read Low Time ( <a href="#">Note 14</a> )	$t_{RL}$		0.25		$2 - \delta$	$\mu\text{s}$
Read Sample Time ( <a href="#">Note 14</a> )	$t_{MSR}$		$t_{RL} + \delta$		2	$\mu\text{s}$
<b>Strong Pullup Operation</b>						
Strong Pullup Current	$I_{SPU}$	( <a href="#">Note 15</a> )			6	mA
Strong Pullup Voltage	$V_{SPU}$	( <a href="#">Note 15</a> )	1.62			V
Read Memory Time	$t_{RM}$	( <a href="#">Note 16</a> )		75		ms
Write Memory Time	$t_{WM}$	( <a href="#">Note 16</a> )		100		ms
Generate ECDSA Signature	$t_{GES}$	( <a href="#">Note 16</a> )		205		ms
Verify ECDSA Signature	$t_{VES}$	( <a href="#">Note 16</a> )		250		ms
<b>EEPROM</b>						
Write/Erase Cycles (Endurance)	$N_{CY}$	( <a href="#">Note 17</a> )	100k			

## Electrical Characteristics (continued)

(Limits are 100% tested at  $T_A = +25^{\circ}\text{C}$  and  $T_A = +85^{\circ}\text{C}$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention	$t_{\text{DR}}$	$T_A = +85^{\circ}\text{C}$ ( <a href="#">Note 18</a> )	10			years
<b>POWER-UP</b>						
Power-Up Time	$t_{\text{OSCWUP}}$	System requirement ( <a href="#">Note 19</a> )			10	ms

**Note 1:** System requirement. Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.

**Note 2:** Value represents the typical parasite capacitance when  $V_{\text{PUP}}$  is first applied. Once the parasite capacitance is charged, it does not affect normal communication.

**Note 3:**  $V_{\text{TL}}$ ,  $V_{\text{TH}}$ , and  $V_{\text{HY}}$  are a function of the internal supply voltage, which is a function of  $V_{\text{PUP}}$ ,  $R_{\text{PUP}}$ , 1-Wire timing, and capacitive loading on IO. Lower  $V_{\text{PUP}}$ , higher  $R_{\text{PUP}}$ , shorter  $t_{\text{REC}}$ , and heavier capacitive loading all lead to lower values of  $V_{\text{TL}}$ ,  $V_{\text{TH}}$ , and  $V_{\text{HY}}$ .

**Note 4:** Voltage below which, during a falling edge on IO, a logic-zero is detected.

**Note 5:** The voltage on IO must be less than or equal to  $V_{\text{ILMAX}}$  at all times the controller is driving IO to a logic-zero level.

**Note 6:** Voltage above which, during a rising edge on IO, a logic-one is detected.

**Note 7:** After  $V_{\text{TH}}$  is crossed during a rising edge on IO, the voltage on IO must drop by at least  $V_{\text{HY}}$  to be detected as logic-zero.

**Note 8:** The I-V characteristic is linear for voltages less than 1V.

**Note 9:** System requirement. Applies to a single device attached to a 1-Wire line.

**Note 10:** Defines maximum possible bit rate. Equal to  $1/(t_{\text{WOLMIN}} + t_{\text{RECMIN}})$ .

**Note 11:** An additional reset or communication sequence cannot begin until the reset high time has expired.

**Note 12:** System requirement. Interval after  $t_{\text{RSTL}}$  during which a bus controller can read a logic 0 on IO if there is a device present. The power-up presence detect pulse could be outside this interval, but completes within 2ms after power-up.

**Note 13:** System requirement.  $\epsilon$  in [Figure 3](#) represents the time required for the pullup circuitry to pull the voltage on IO up from  $V_{\text{IL}}$  to  $V_{\text{TH}}$ . The actual maximum duration for the controller to pull the line low is  $t_{\text{W1LMAX}} + t_{\text{F}} - \epsilon$  and  $t_{\text{W0LMAX}} + t_{\text{F}} - \epsilon$ , respectively.

**Note 14:** System requirement.  $\delta$  in [Figure 3](#) represents the time required for the pullup circuitry to pull the voltage on IO up from  $V_{\text{IL}}$  to the input-high threshold of the bus controller. The actual maximum duration for the controller to pull the line low is  $t_{\text{RLMAX}} + t_{\text{F}}$ .

**Note 15:** Current drawn from IO during a SPU operation interval. The pullup circuit on IO during the SPU operation interval should be such that the voltage at IO is greater than or equal to  $V_{\text{SPUMIN}}$ . A low-impedance bypass of  $R_{\text{PUP}}$  activated during the SPU operation is the recommended way to meet this requirement.

**Note 16:** Guaranteed by design and/or characterization only. Not production tested.

**Note 17:** Write-cycle endurance is tested in compliance with JESD47H.

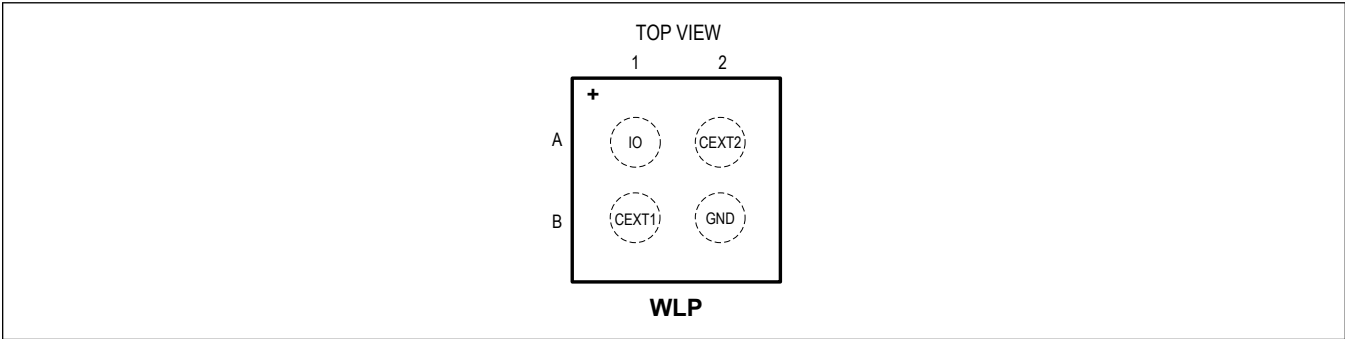
**Note 18:** Data retention is tested in compliance with JESD47H.

**Note 19:** 1-Wire communication should not take place for at least  $t_{\text{OSCWUP}}$  after  $V_{\text{PUP}}$  reaches  $V_{\text{PUP}}(\text{min})$ .

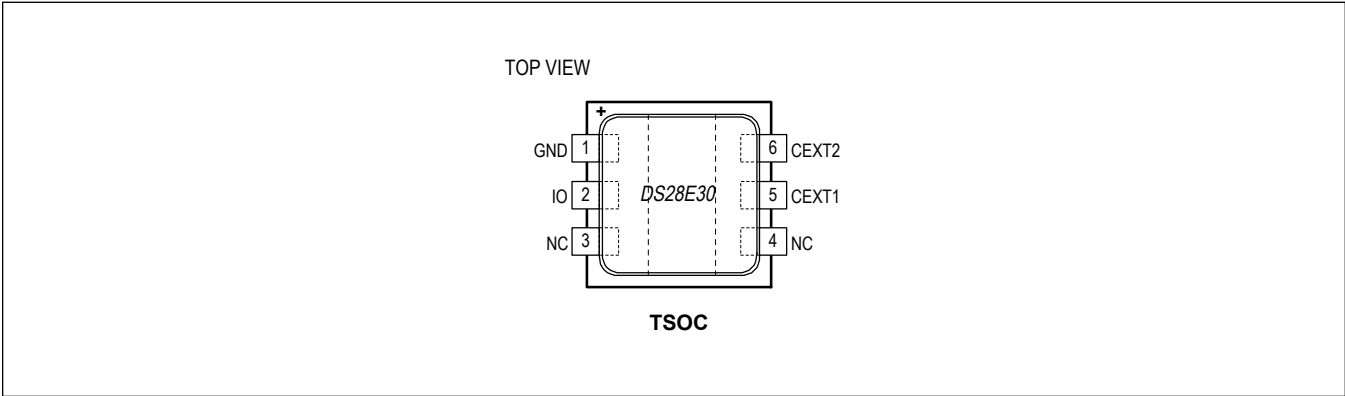


Pin Configurations

4 WLP



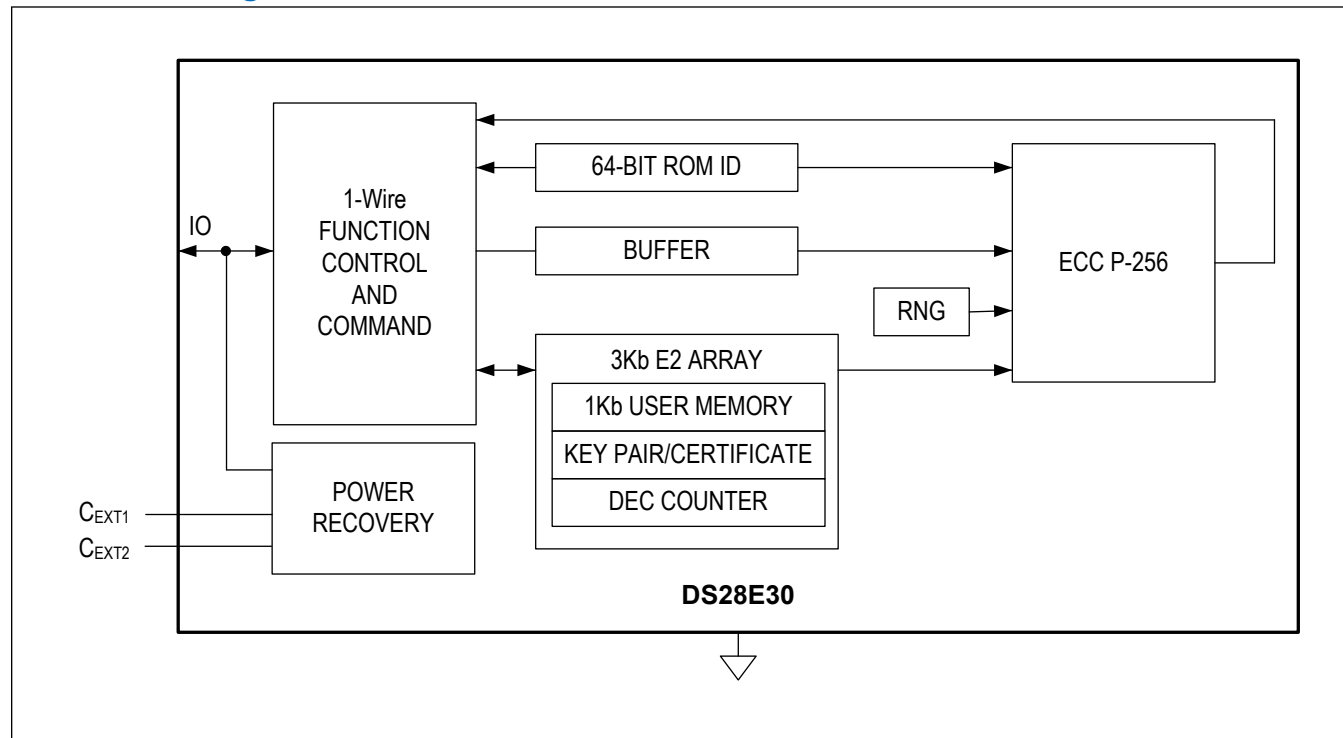
6 TSOC



Pin Description

PIN		NAME	FUNCTION
4 WLP	6 TSOC		
—	3,4	NC	Not Connected
A1	2	IO	1-Wire I/O
B2	1	GND	Ground Reference. Connect directly to the ground plane.
B1	5	CEXT1	Input for External Capacitor
A2	6	CEXT2	Input for External Capacitor

## Functional Diagram



## Detailed Description

The DS28E30 integrates Analog Devices-proprietary techniques to protect all device stored data from invasive or noninvasive discovery. The circuit design combined with cryptographic methods, both inherited from Maxim's financial terminal security experience, protect against die-level data extraction attacks.

In addition to the secure ECDSA engine for signatures, the device integrates a high-quality TRNG, a SHA-256 engine, 1Kb EEPROM for user memory, plus additional EEPROM space for one ECDSA P-256 private key, one ECDSA P-256 public key certificate, one 17-bit decrement counter, and control registers. The device operates from a 1-Wire interface with a parasitic supply by way of an external capacitor (CEXT1) and an additional capacitor (CEXT2) for the internal voltage regulator. The [Functional Diagram](#) shows the relationships between the circuit elements of the DS28E30.

## 1-Wire Bus System

The 1-Wire bus is a system that has a single bus controller and one or more peripherals. In all instances, the DS28E30 is a peripheral device. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus controller.

## Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus can drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E30 is open drain with an internal circuit equivalent.

A multidrop bus consists of a 1-Wire bus with multiple peripherals attached. The DS28E30 supports overdrive communication speed of 90.9kpbs (max). The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E30 requires a pullup resistor of 750Ω (max).

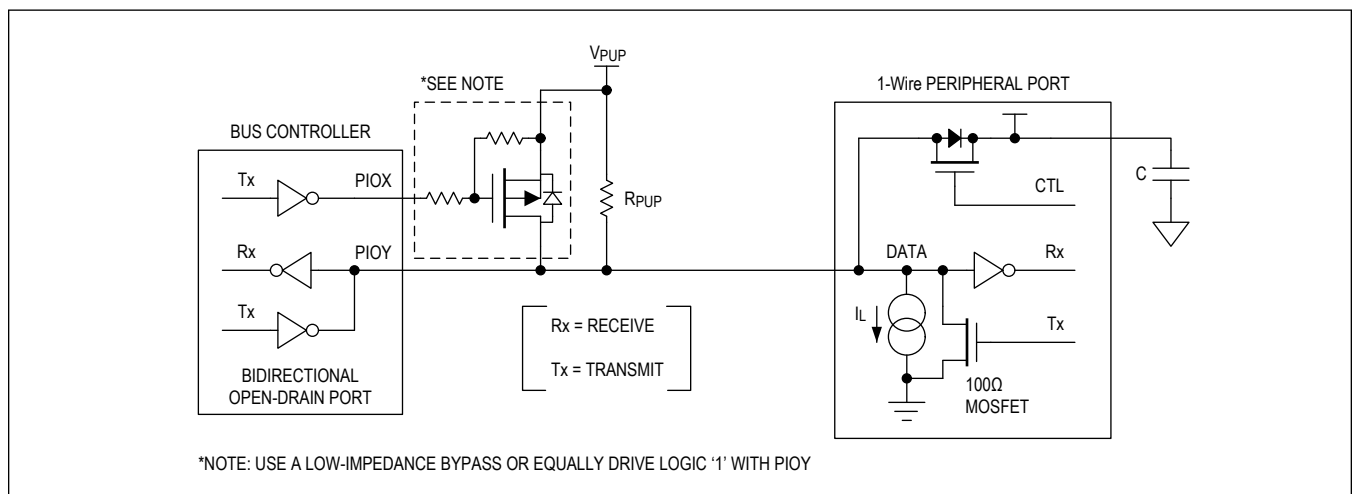


Figure 1. Hardware Configuration

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16μs, one or more devices on the bus could be reset.

## Transaction Sequence

The protocol for accessing the DS28E30 through the 1-Wire port is as follows:

- Initialization
- ROM function command

- Device function command
- Transaction/data

### Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus controller followed by presence pulse(s) transmitted by the peripheral(s). The presence pulse lets the bus controller know that the DS28E30 is on the bus and is ready to operate. For more details, see the [1-Wire Signaling and Timing](#) section.

### 1-Wire Signaling and Timing

The DS28E30 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus controller initiates all falling edges.

To get from idle to active, the voltage on the 1-Wire line needs to fall from  $V_{PUP}$  below the threshold  $V_{TL}$ . To get from active to idle, the voltage needs to rise from  $V_{ILMAX}$  past the threshold  $V_{TH}$ . The time it takes for the voltage to make this rise is seen in [Figure 2](#) as  $\epsilon$ , and its duration depends on the pullup resistor ( $R_{PUP}$ ) used and the capacitance of the 1-Wire network attached. The voltage  $V_{ILMAX}$  is relevant for the DS28E30 when determining a logical level, not when triggering any events.

[Figure 2](#) shows the initialization sequence required to begin any communication with the DS28E30. A reset pulse followed by a presence pulse indicates that the DS28E30 is ready to receive data, given the correct ROM and device function command. If the bus controller uses slew-rate control on the falling edge, it must pull down the line for  $t_{RSTL} + t_F$  to compensate for the edge.

After the bus controller has released the line, it goes into receive mode. Now, the 1-Wire bus is pulled to  $V_{PUP}$  through the pullup resistor or, in the case of a special driver chip, through the active circuitry. When the threshold  $V_{TH}$  is crossed, the DS28E30 waits and then transmits a presence pulse by pulling the line low. To detect a presence pulse, the controller must test the logical state of the 1-Wire line at  $t_{MSP}$ .

Immediately after  $t_{RSTH}$  has expired, the DS28E30 is ready for data communication.

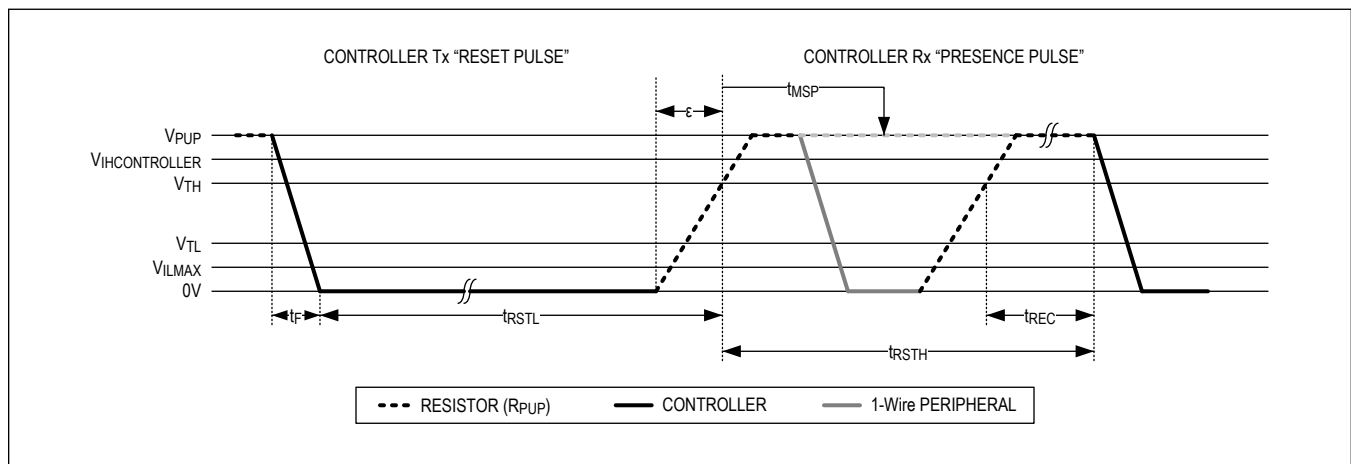


Figure 2. Initialization Procedure: Reset and Presence Pulse

### Read/Write Time Slots

Data communication with the DS28E30 takes place in time slots that carry a single bit each. Write time slots transport data from the bus controller to the peripheral. Read time slots transfer data from the peripheral to the controller. [Figure 3](#) illustrates the definitions of the write and read time slots.

All communication begins with the controller pulling the data line low. As the voltage on the 1-Wire line falls below the threshold  $V_{TL}$ , the DS28E30 starts its internal timing generator that determines when the data line is sampled during a

write time slot and how long data is valid during a read time slot.

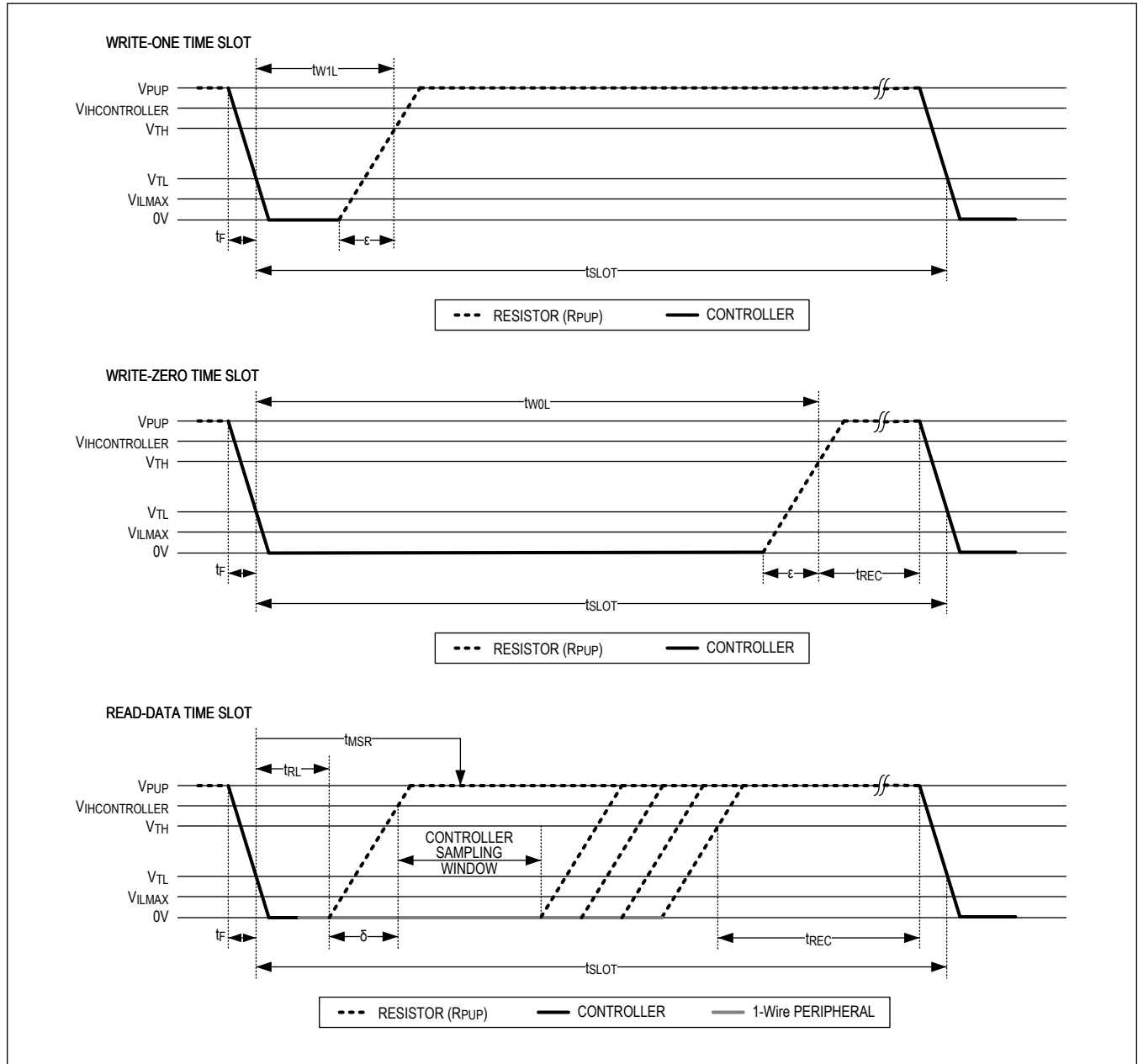


Figure 3. Read/Write Timing Diagrams

### Controller to Peripheral

For a write-one time slot, the voltage on the data line must have crossed the  $V_{TH}$  threshold before the write-one low time  $t_{W1LMAX}$  is expired. For a write-zero time slot, the voltage on the data line must stay below the  $V_{TH}$  threshold until the write-zero low time  $t_{W0LMAX}$  is expired. For the most reliable communication, the voltage on the data line should not exceed  $V_{ILMAX}$  during the entire  $t_{W0L}$  or  $t_{W1L}$  window. After the  $V_{TH}$  threshold has been crossed, the DS28E30 needs recovery time  $t_{REC}$  before it is ready for the next time slot.

### Peripheral to Controller

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below  $V_{TL}$  until the read low time  $t_{RL}$  is expired. During the  $t_{RL}$  window, when responding with a 0, the DS28E30 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E30 does not hold the data line low at all, and the voltage starts rising as soon as  $t_{RL}$  is over.

The sum of  $t_{RL} + \delta$  (rise time) on one side and the internal timing generator of the DS28E30 on the other side define the controller sampling window ( $t_{MSRMIN}$  to  $t_{MSRMAX}$ ), in which the controller must perform a read from the data line. For the most reliable communication,  $t_{RL}$  should be as short as permissible, and the controller should read close to, but no later than  $t_{MSRMAX}$ . After reading from the data line, the controller must wait until  $t_{SLOT}$  is expired. This guarantees sufficient recovery time  $t_{REC}$  for the DS28E30 to get ready for the next time slot. Note that  $t_{REC}$  specified herein applies only to a single DS28E30 attached to a 1-Wire line. For multidevice configurations,  $t_{REC}$  must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the special 1-Wire line drivers can be used.

### 1-Wire ROM Commands

Once the bus controller has detected a presence, it can issue one of the five ROM function commands that the DS28E30 supports. All ROM function commands are 8 bits long. For operational details, see [Figure 4](#). A descriptive list of these ROM function commands follows in the subsequent sections, and the commands are summarized in [Table 1](#).

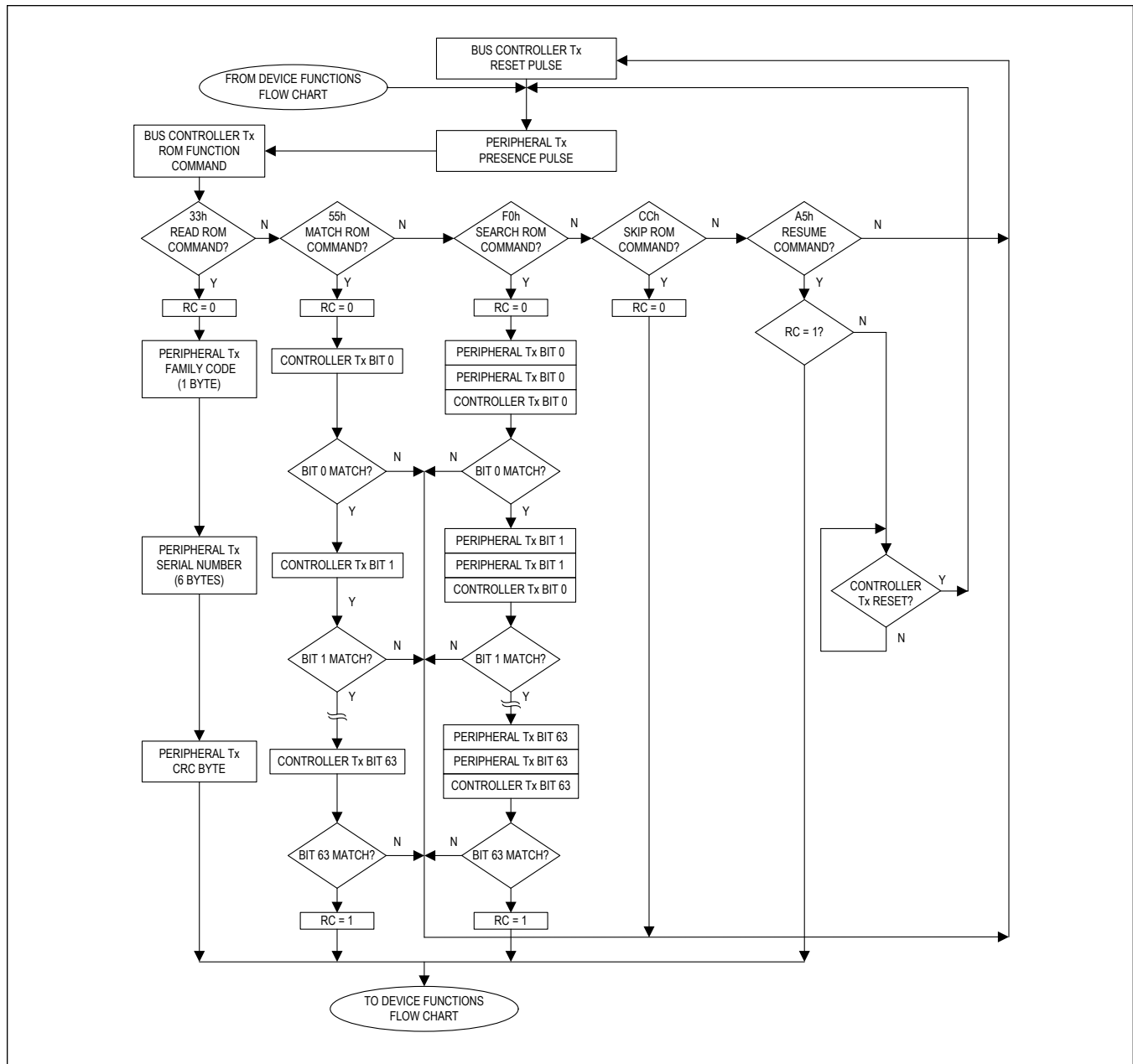


Figure 4. ROM Function Flow

Table 1. 1-Wire ROM Commands Summary

ROM FUNCTION COMMAND	CODE	DESCRIPTION
Search ROM	F0h	Search for a device
Read ROM	33h	Read ROM from device (single drop)
Match ROM	55h	Select a device by ROM number
Skip ROM	CCh	Select only device on 1-Wire
Resume	A5h	Selected device with RC bit set

### Search ROM [F0h]

When a system is initially brought up, the bus controller might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the controller can use a process of elimination to identify the ID of all peripheral devices. For each bit in the ID number, starting with the least significant bit, the bus controller issues a triplet of time slots. On the first slot, each peripheral device participating in the search outputs the true value of its ID number bit. On the second slot, each peripheral device participating in the search outputs the complemented value of its ID number bit. On the third slot, the controller writes the true value of the bit to be selected. All peripheral devices that do not match the bit written by the controller stop participating in the search. If both of the read bits are zero, the controller knows that peripheral devices exist with both states of the bit. By choosing which state to write, the bus controller branches in the search tree. After one complete pass, the bus controller knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to [Application Note 187: 1-Wire Search Algorithm](#) for a detailed discussion, including an example.

### Read ROM [33h]

The Read ROM command allows the bus controller to read the DS28E30's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single peripheral on the bus. If more than one peripheral is present on the bus, a data collision occurs when all peripherals try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

### Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus controller to address a specific DS28E30 on a multidrop bus. Only the DS28E30 that exactly matches the 64-bit ROM sequence responds to the subsequent device function command. All other peripherals wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

### Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus controller to access the device functions without providing the 64-bit ROM ID. If more than one peripheral is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple peripherals transmit simultaneously (open-drain pulldowns produce a wired-AND result).

### Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the device function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM or Search ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

### Improved Network Behavior (Switch-Point Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus controller (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a peripheral device to lose synchronization with the controller and, consequently, result in a command error or command abort. For better performance in network applications, the DS28E30 uses a 1-Wire front-end with built-in hysteresis. If a negative glitch crosses  $V_{TH}$ , but does not go below  $V_{TH} - V_{HY}$ , it is not recognized. See [Figure 5](#).



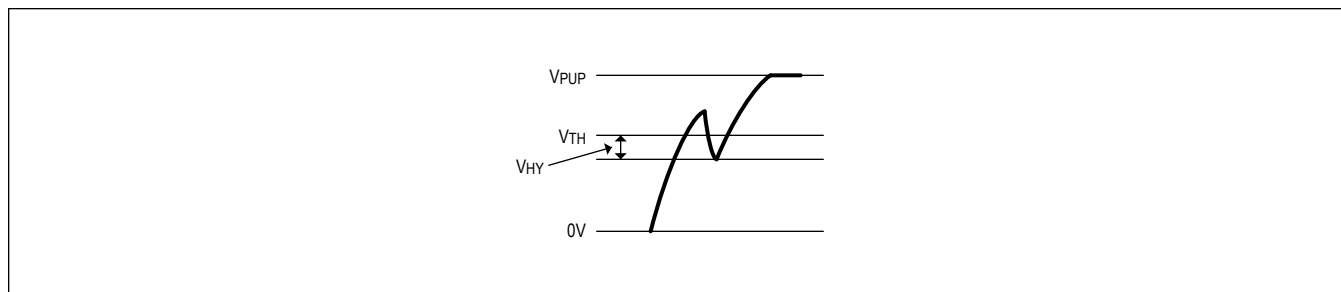


Figure 5. Noise Suppression Scheme

### Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
DS28E30X+T	-40°C to +85°C	4 WLP
DS28E30P+T	-40°C to +85°C	6 TSOC
DS28E30P+	-40°C to +85°C	6 TSOC

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Initial release	—
1	2/22	Updated <i>Electrical Characteristics</i> ( $V_{PUP, max}$ ), <i>Detailed Description</i> , and <i>Ordering Information</i> tables	3, 10, 17
2	9/22	Added TSOC package	1, 3, 6, 9, 18
3	5/23	Updated <i>Electrical Characteristics</i> ( $R_{PUP, max} = 2.2k$ above 2.7V)	6