

Nonreflective, Silicon SP4T Switch, 100 MHz to 20 GHz

FEATURES

- ▶ Wideband frequency range: 100 MHz to 20 GHz
- ▶ Nonreflective design with on-chip 50 Ω terminations
- ▶ Low insertion loss
 - ▶ 0.9 dB typical to 6 GHz
 - ▶ 1.0 dB typical to 12 GHz
 - ▶ 1.2 dB typical to 20 GHz
- ▶ High isolation
 - ▶ 54 dB typical to 6 GHz
 - ▶ 50 dB typical to 12 GHz
 - ▶ 47 dB typical to 20 GHz
- ▶ High linearity
 - ▶ Input P0.1dB: 34 dBm typical
 - ▶ Input IP3: 55 dBm typical
- ▶ High RF power handling
 - ▶ Through path: 33 dBm up to 20 GHz
 - ▶ Terminated path: 18 dBm up to 20 GHz
- ▶ Switching on and off time: 55 ns
- ▶ 0.1 dB settling time: 80 ns
- ▶ All off state control
- ▶ Logic select control
- ▶ Single-supply operation with derated power handling
- ▶ No low frequency spurs, no internal voltage generation
- ▶ 24-terminal, 3 mm \times 3 mm, land grid array (LGA) package
- ▶ Pin compatible with the [ADRF5042](#) and [ADRF5043](#)

APPLICATIONS

- ▶ Test instrumentation
- ▶ Military radios, radars, and electronic counter measures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

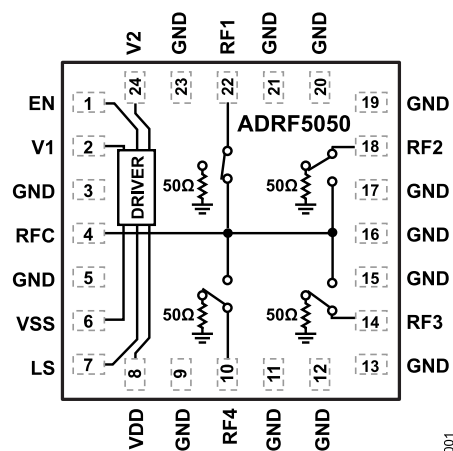


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5050 is a nonreflective SP4T switch manufactured in a silicon on insulator (SOI) process.

The ADRF5050 operates from 100 MHz to 20 GHz with insertion loss less than 1.2 dB and isolation higher than 47 dB. The device has RF input power handling capability of 33 dBm for through paths, 18 dBm for terminated path, and 30 dBm hot switching at the RF common (RFC) port.

The ADRF5050 operates with a dual-supply voltage +3.3 V and -3.3 V. The device can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply pin (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated, see [Table 2](#).

The ADRF5050 employs complimentary metal-oxide semiconductor (CMOS)- and low voltage transistor to transistor logic (LVTTL)-compatible controls.

The device has enable (EN) and logic select (LS) controls. Pulling EN pin to high activates all-off state while pulling LS pin high inverts the throw port selection logic, allowing ease of use for back-to-back applications. Please see the [Theory of Operation](#) section, [Table 7](#) and the [Back-to-Back Application](#) section.

The ADRF5050 is pin compatible with the [ADRF5042](#) and [ADRF5043](#).

The ADRF5050 comes in a 24-terminal, 3 mm \times 3 mm, RoHS compliant, land grid array (LGA) package and can operate from -40°C to +105°C.

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REVISION HISTORY**10/2025—Rev. B to Rev. C**

Changes to Features Section.....	1
Changes to General Description Section.....	1
Changes to Table 1.....	3
Changes to Table 2.....	4
Added Note 1 to Note 3, Table 2.....	4
Changes to Table 3.....	6
Change to Table 4.....	6
Changes to Figure 5 and Figure 6.....	9
Added Figure 7; Renumbered Sequentially.....	9
Changes to Insertion Loss, Return Loss, and Isolation Section, Figure 12 Caption to Figure 22 Caption....	10
Changes to Input Power Compression and Third-Order Intercept Section.....	13
Changes to Theory of Operation Section.....	14
Moved Table 7.....	14
Changes to RF Input and Output Section.....	15
Changes to Recommendations for Printed Circuit Board Design Section, Figure 29, and Figure 30.....	16
Added Back-to-Back Application Section, Figure 31, and Table 8; Renumbered Sequentially.....	16

11/2024—Rev. A to Rev. B

Updated Outline Dimensions.....	18
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8/2023—Rev. 0 to Rev. A

Updated Outline Dimensions	18
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2/2023—Revision 0: Initial Version

SPECIFICATIONS

Positive supply voltage (V_{DD}) = 3.3 V, negative supply voltage (V_{SS}) = -3.3 V, Control Input 1 voltage (V_1) and Control Input 2 voltage (V_2) = 0 V or V_{DD} , T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. V_{CTRL} is the voltages of the digital control inputs, V_1 and V_2 . RFx refers to RF1, RF2, RF3, and RF4.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		100		20,000	MHz
INSERTION LOSS						
Between RFC and RFx (On)		100 MHz to 6 GHz		0.9		dB
		6 GHz to 12 GHz		1.0		dB
		12 GHz to 20 GHz		1.2		dB
ISOLATION						
Between RFC and RFx (Off)		100 MHz to 6 GHz		56		dB
		6 GHz to 12 GHz		54		dB
		12 GHz to 20 GHz		47		dB
Between RFx and RFx		100 MHz to 6 GHz		54		dB
		6 GHz to 12 GHz		50		dB
		12 GHz to 20 GHz		47		dB
RETURN LOSS						
RFC		100 MHz to 6 GHz		26		dB
		6 GHz to 12 GHz		22		dB
		12 GHz to 20 GHz		22		dB
RFx (On)		100 MHz to 6 GHz		24		dB
		6 GHz to 12 GHz		19		dB
		12 GHz to 20 GHz		18		dB
RFx (Off)		100 MHz to 6 GHz		20		dB
		6 GHz to 12 GHz		15		dB
		12 GHz to 20 GHz		12		dB
SWITCHING						
Rise and Fall Time	t_{RISE} , t_{FALL}	10% to 90% of RF output (RF_{OUT})		12		ns
On and Off Time	t_{ON} , t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		55		ns
0.1 dB Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		80		ns
INPUT LINEARITY ¹						
0.1 dB Power Compression	P0.1dB	f = 100 MHz to 20 GHz		34		dBm
Third-Order Intercept	IP3	Two-tone input power = 15 dBm each tone, f = 100 MHz to 20 GHz, Δf = 1 MHz		55		dBm
Second-Order Intercept	IP2	Two-tone input power = 15 dBm each tone, f = 8 GHz, Δf = 1 MHz		110		dBm
VIDEO FEEDTHROUGH ²				30		mV p-p
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			155		μA
Negative Supply Current	I_{SS}			530		μA
DIGITAL CONTROL INPUTS		V1, V2, EN, and LS pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		μA
High	I_{INH}	V1 and V2 pins		3		μA
		EN pin		40		μA
		LS pin		37		μA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		-3.45		-3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Power Handling ³		$f = 100 \text{ MHz to } 20 \text{ GHz}$, $T_{CASE} = 85^{\circ}\text{C}$ ⁴				
Through Path		RF signal is applied to RFC or through connected RF throw port (selected RFx)			33	dBm
Terminated Path		RF signal is applied to any unselected RF throw port (unselected RFx)			18	dBm
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports			30	dBm
Hot Switching (RFx)		RF signal is applied to a RFx port while switching to or from another RFx port			18	dBm
Case Temperature	T_{CASE}		-40		+105	$^{\circ}\text{C}$

¹ For input linearity performance over frequency, see Figure 23 to Figure 26.

² Video feedthrough is the peak transient measured at the RF ports in a 50 Ω test setup, without an RF signal present while switching the control voltage.

³ For RF power handling derating over extended frequency range, see Figure 2.

⁴ For $T_{CASE} = 105^{\circ}\text{C}$ operation, the RF power handling derates from the $T_{CASE} = 85^{\circ}\text{C}$ specification by 3 dB.

SINGLE-SUPPLY OPERATION SPECIFICATIONS

$V_{DD} = 3.3 \text{ V}$, $V_{SS} = 0 \text{ V}$, V_1 and $V_2 = 0 \text{ V}$ or V_{DD} , $T_{CASE} = 25^{\circ}\text{C}$, and 50 Ω system, unless otherwise noted.

The small signal and bias specifications are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		20,000	MHz
SWITCHING						
Rise and Fall Time	t_{RISE} , t_{FALL}	10% to 90% of RF_{OUT}		85		ns
On and Off Time	t_{ON} , t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		175		ns
0.1 dB Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		200		ns
INPUT LINEARITY ¹						
0.1 dB Power Compression	P0.1dB	$f = 100 \text{ MHz to } 20 \text{ GHz}$		17		dBm
Third-Order Intercept	IP3	Two-tone input power = 15 dBm each tone, $f = 100 \text{ MHz to } 20 \text{ GHz}$, $\Delta f = 1 \text{ MHz}$		42		dBm
Second-Order Intercept	IP2	Two-tone input power = 15 dBm each tone, $f = 8 \text{ GHz}$, $\Delta f = 1 \text{ MHz}$		86		dBm
SUPPLY CURRENT						
Positive Supply Current	I_{DD}			36		μA
RECOMMENDED OPERATING CONDITIONS						
RF Power Handling ²		$f = 100 \text{ MHz to } 20 \text{ GHz}$, $T_{CASE} = 85^{\circ}\text{C}$ ³				
Through Path		RF signal is applied to RFC or through connected RF throw port (selected RFx)			22	dBm
Terminated Path		RF signal is applied to any unselected RF throw port (unselected RFx)			18	dBm
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports			21	dBm

SPECIFICATIONS

Table 2. Single-Supply Operation Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hot Switching (RFx)		RF signal is applied to a RFx port while switching to or from another RFx port			18	dBm
Case Temperature	T _{CASE}		-40		+105	°C

¹ For input linearity performance over frequency, see [Figure 23](#) to [Figure 26](#).

² For RF power handling derating over extended frequency range, see [Figure 2](#).

³ For T_{CASE}=105°C operation, the RF power handling derates from the T_{CASE}= 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
V_{DD}	-0.3 V to +3.6 V
V_{SS}	-3.6 V to +0.3 V
Digital Control Inputs ¹	
Voltage	-0.3 V to $V_{DD} + 0.3$ V
Current	3 mA
RF Input Power ²	
Dual Supply ($V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, frequency = 100 MHz to 20 GHz, $T_{CASE} = 85^{\circ}\text{C}$ ³)	
Through Path	33.5 dBm
Terminated Path	18.5 dBm
Hot Switching (RFC)	30.5 dBm
Hot Switching (RFx)	18.5 dBm
Single Supply ($V_{DD} = 3.3$ V, $V_{SS} = 0$ V, frequency = 100 MHz to 20 GHz, $T_{CASE} = 85^{\circ}\text{C}$ ³)	
Through Path	22.5 dBm
Terminated Path	18.5 dBm
Hot Switching (RFC)	21.5 dBm
Hot Switching (RFx)	18.5 dBm
Unbiased ($V_{DD} = 0$ V, $V_{SS} = 0$ V)	
RFC	30 dBm
RFx	27 dBm
Temperature	
Junction, T_J	135°C
Storage Range	-65°C to +150°C
Reflow	260°C

¹ Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

² For RF power handling derating over extended frequency range, see Figure 2.

³ For $T_{CASE} = 105^{\circ}\text{C}$ operation, the power handling degrades from the $T_{CASE} = 85^{\circ}\text{C}$ specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC} ¹	Unit
CC-24-16		
Through Path	110	°C/W
Terminated Path	800	°C/W

¹ θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

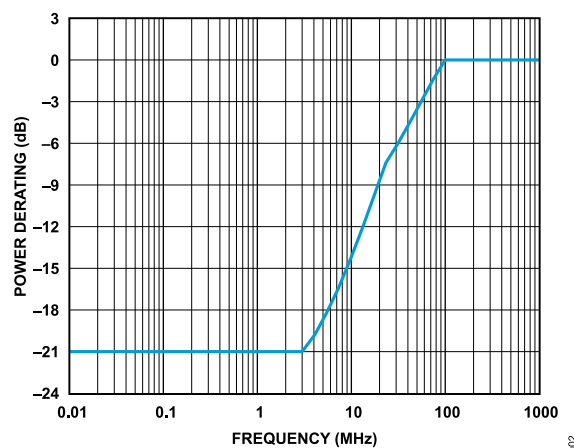


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE} = 85^{\circ}\text{C}$

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5050

Table 5. ADRF5050, 24-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
RFx and RFC Pins	1000	1C
Supply and Control Pins	2000	2
CDM	500	C2A

ABSOLUTE MAXIMUM RATINGS**ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

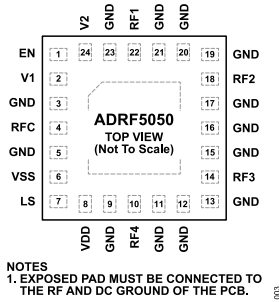


Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. See Table 7 for the truth table and Figure 6 for the interface schematic.
2	V1	Control Input 1. See Table 7 for the truth table and Figure 5 for the interface schematic.
3, 5, 9, 11 to 13, 15 to 17, 19 to 21, 23	GND	Ground. The GND pins must be connected to the RF and dc ground of the PCB.
4	RFC	RF Common Port. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
6	VSS	Negative Supply Voltage.
7	LS	Logic Select Input. See Table 7 for the truth table and Figure 7 for the interface schematic.
8	VDD	Positive Supply Voltage.
10	RF4	RF Throw Port 4. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
14	RF3	RF Throw Port 3. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
18	RF2	RF Throw Port 2. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
22	RF1	RF Throw Port 1. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
24	V2	Control Input 2. See Table 7 for the truth table and Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

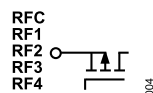


Figure 4. RFC and RF1 to RF4 Pin Interface Schematic

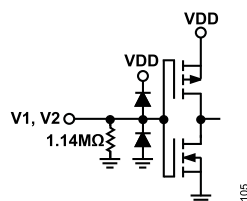


Figure 5. V1 and V2 Pin Interface Schematic

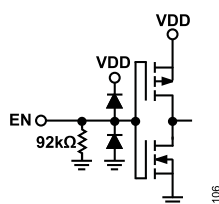


Figure 6. EN Pin Interface Schematic

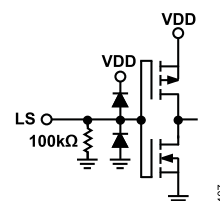


Figure 7. LS Pin Interface Schematic

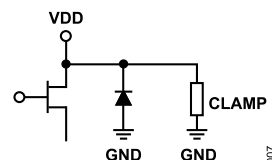


Figure 8. VDD Pin Interface Schematic

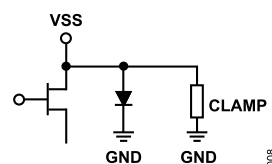


Figure 9. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, LS and EN = 0V, V_1 , or $V_2 = 0\text{ V}$ or V_{DD} , and $T_{CASE} = 25^\circ\text{C}$ on a $50\ \Omega$ system, unless otherwise noted.

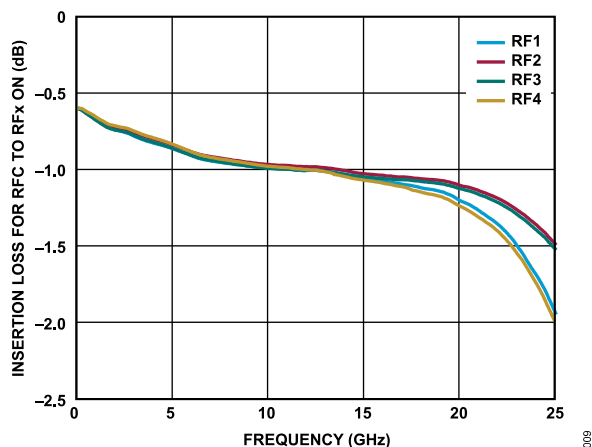


Figure 10. Insertion Loss for RFC to RFx (On) vs. Frequency

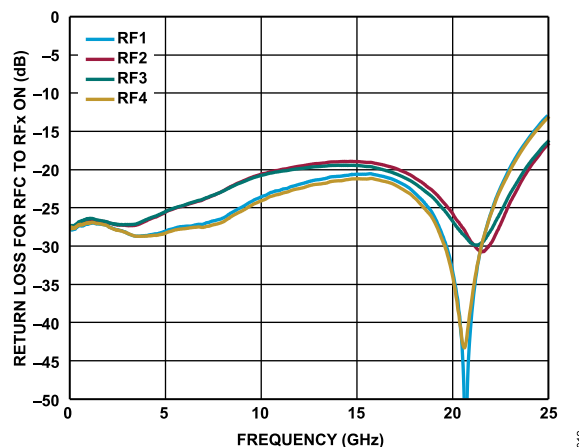


Figure 13. Return Loss for RFx (On) vs. Frequency

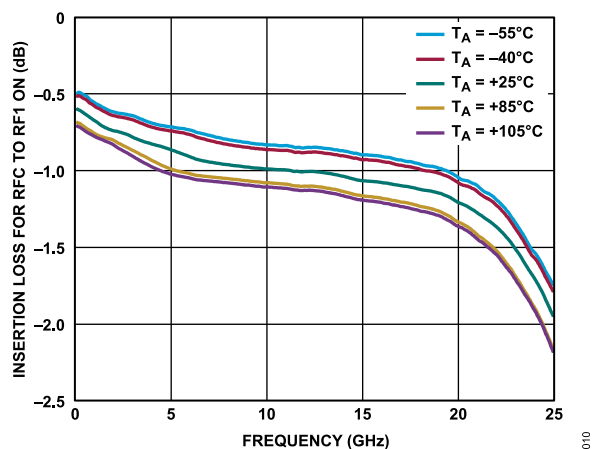


Figure 11. Insertion Loss for RFC to RF1 (On) vs. Frequency over Temperature

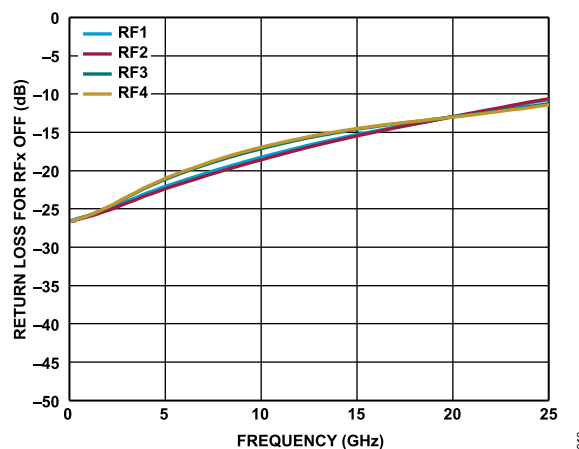


Figure 14. Return Loss for RFx (Off) vs. Frequency

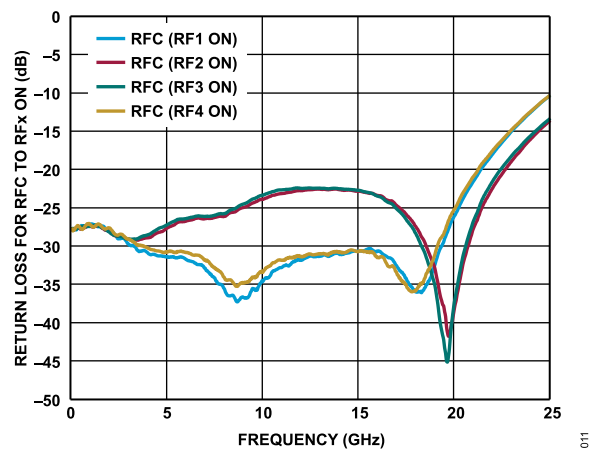


Figure 12. Return Loss for RFC vs. Frequency

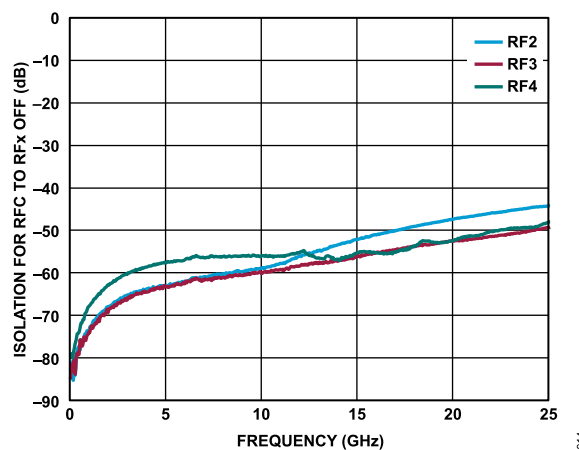


Figure 15. Isolation for RFC to RFx (Off) vs. Frequency, RF1 (On)

TYPICAL PERFORMANCE CHARACTERISTICS

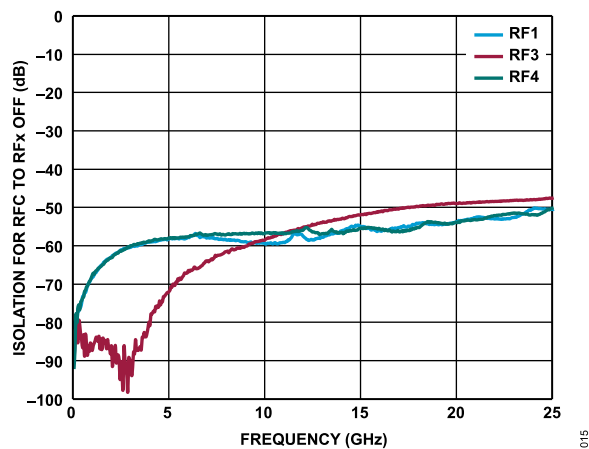


Figure 16. Isolation for RFC to RFx (Off) vs. Frequency, RF2 (On)

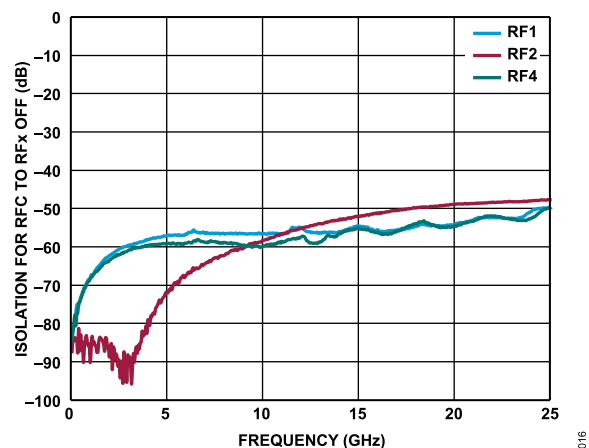


Figure 17. Isolation for RFC to RFx (Off) vs. Frequency, RF3 (On)

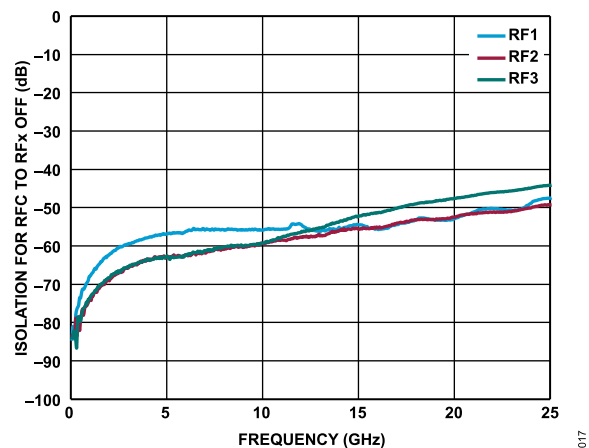


Figure 18. Isolation for RFC to RFx (Off) vs. Frequency, RF4 (On)

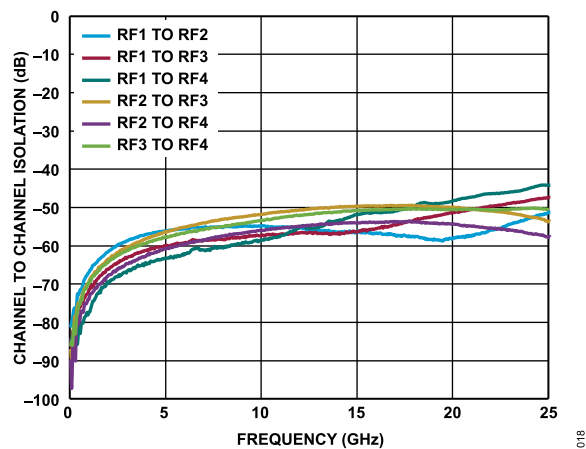


Figure 19. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF1 (On)

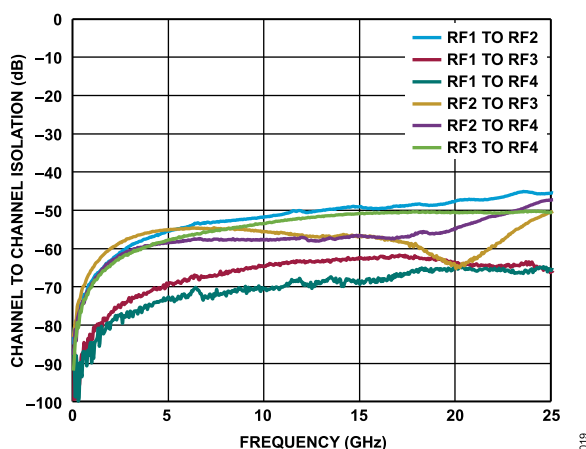


Figure 20. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF2 (On)

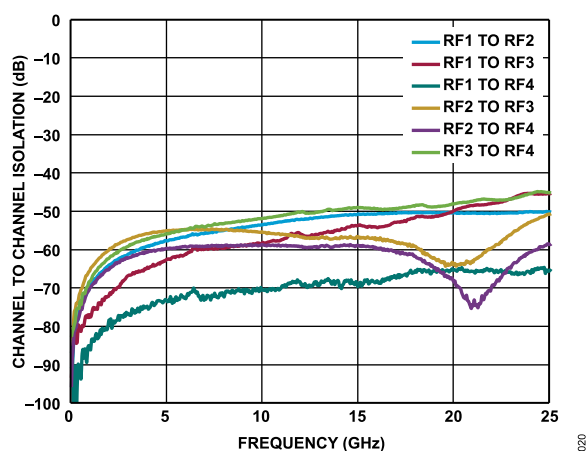


Figure 21. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF3 (On)

TYPICAL PERFORMANCE CHARACTERISTICS

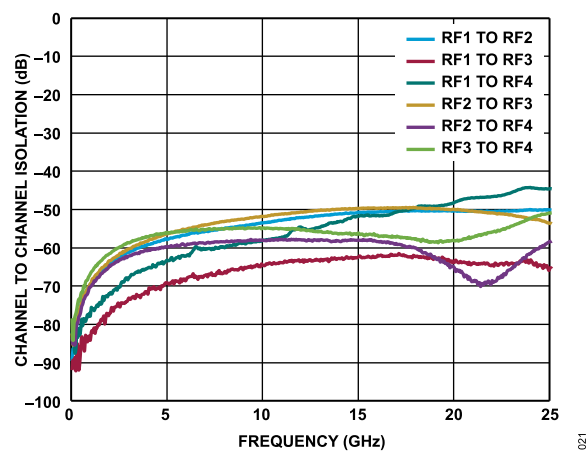


Figure 22. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF4 (On)

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, LS and EN = 0 V, V_1 , or $V_2 = 0\text{ V}$ or V_{DD} , and $T_{CASE} = 25^\circ\text{C}$ on a $50\ \Omega$ system, unless otherwise noted.

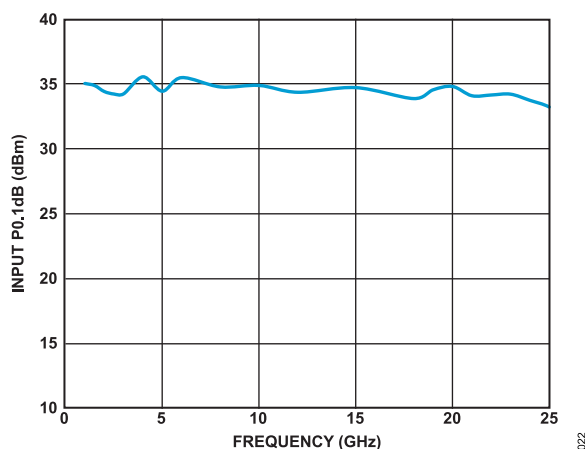


Figure 23. Input P0.1dB vs. Frequency

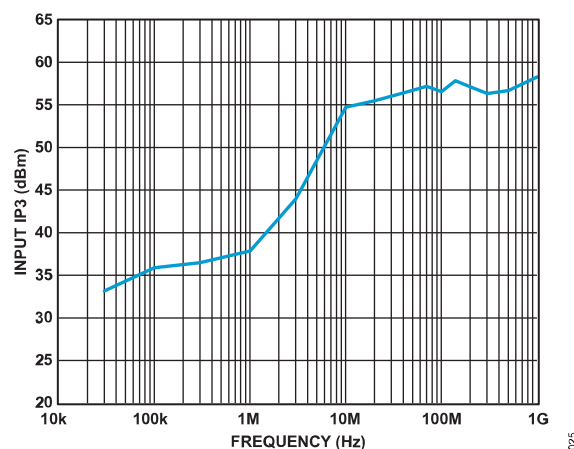


Figure 26. Input IP3 vs. Frequency, Low Frequency Detail

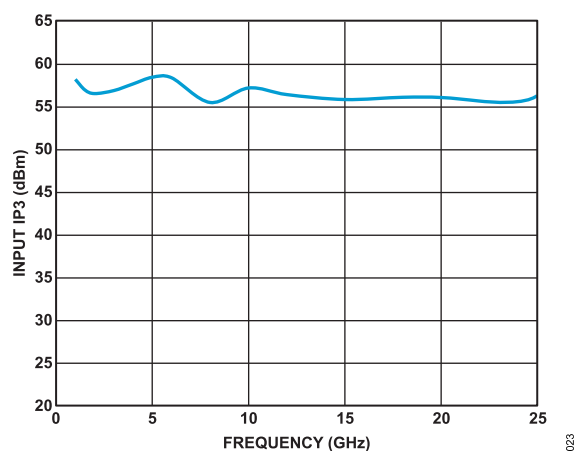


Figure 24. Input IP3 vs. Frequency

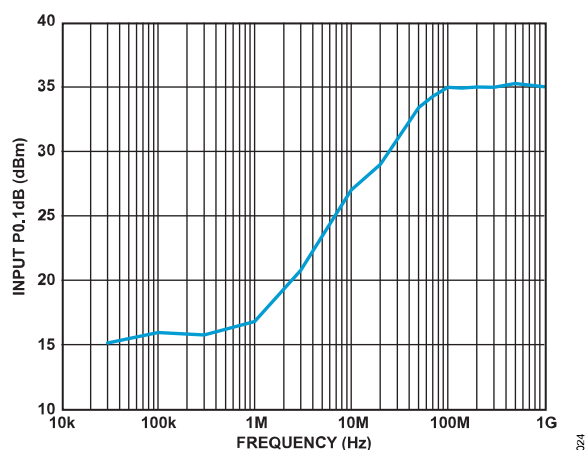


Figure 25. Input P0.1dB vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5050 integrates a CMOS-/LVTTTL-compatible control interface. The digital control input pins (EN, LS, V1, and V2) control the state of the RF paths (see [Table 7](#)).

The logic levels applied to the V1 and V2 pins determine which RF throw (RFx) port is in the insertion loss state (selected or on). The remaining three RFx ports are in the isolation state (unselected or off).

Table 7. Control Voltage Truth Table

Digital Control Inputs				RFx Paths			
EN	LS	V1	V2	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
Low	Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low or high	Low or high	Low or high	Isolation (off)	Isolation (off)	Isolation (off)	Isolation (off)

The LS pin allows the user to invert the RFx port selection logic (see the truth table for V1 and V2, [Table 7](#)). See the application example of this feature in the [Back-to-Back Application](#) section.

When the EN pin is logic high, all four RF paths are in an isolation state regardless of the logic state of the LS, V1, and V2 pins. The RFx ports are terminated to internal 50Ω resistors, and RFC becomes reflective.

THEORY OF OPERATION

RF INPUT AND OUTPUT

All of the RF ports (RFC and RF1 to RF4) are biased to ground potential, and a DC blocking capacitor is not required at the RF ports when the RF line potential is equal to ground. The RF ports are internally matched to 50 Ω . Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. All unselected RF throw ports have high isolation from RFC and the remaining RF throw ports.

POWER SUPPLY

The ADRF5050 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Powering up VSS after VDD avoids current transients on VDD during ramp up.

3. Apply a control voltage to the digital control inputs (EN, LS, V1, and V2). Applying a control voltage to the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. Use a series 1 k Ω resistor to limit the current flowing into the control pin in such cases. If the control pins are not driven to a valid logic state (that is, the controller output is in a high impedance state) after VDD is powered up, it is recommended to use a pull-up or pull-down resistor.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

SINGLE-SUPPLY OPERATION

The ADRF5050 can operate with a single positive supply voltage applied to the VDD pin and VSS pin connected to ground. In single-supply operation, the switching characteristics, linearity, and power handling performance are derated, see [Table 2](#) for additional information.

APPLICATIONS INFORMATION

The ADRF5050 has two power supply pins (VDD and VSS) and four control pins (LS, EN, V1, and V2). [Figure 27](#) shows the external components and connections for the supply and control pins. The supply and control pins are decoupled with 100 pF multilayer ceramic capacitor. Place the decoupling capacitors as close as possible to the ADRF5050. The device pinout allows the placement of the decoupling capacitors close to the ADRF5050. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. Refer to [Pin Configuration and Function Descriptions](#) section for additional information.

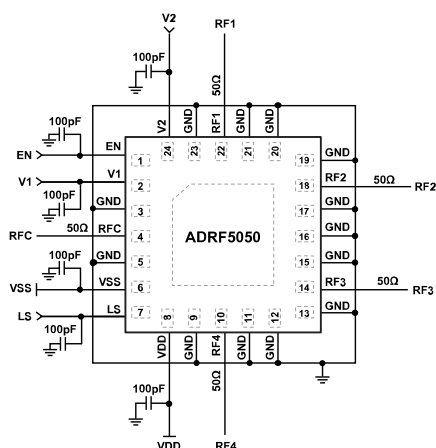


Figure 27. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50 Ω characteristic impedance on the PCB. [Figure 28](#) shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

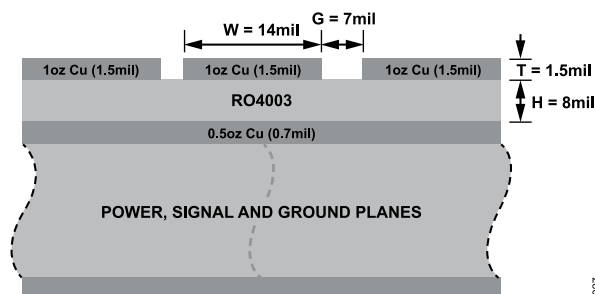


Figure 28. Example PCB Stack Up

[Figure 29](#) shows the routing of the RF traces, supply, and control signals from the ADRF5050. The ground planes are connected with as many filled, through vias as allowed for optimal RF and thermal

performance. The primary thermal path for the device is the bottom side.

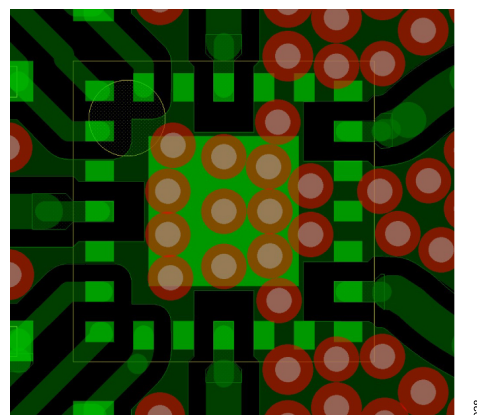


Figure 29. PCB Routings

[Figure 30](#) shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended to the device edge and tapered to RF trace with 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

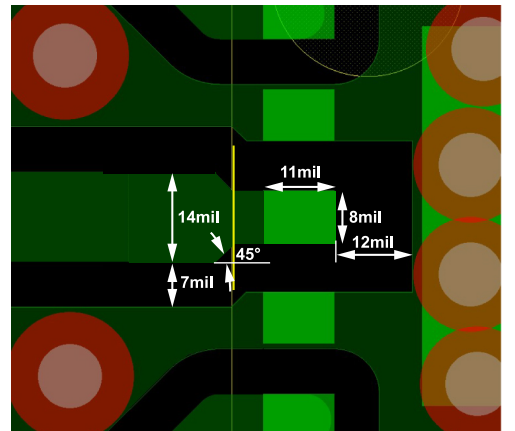


Figure 30. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact [Analog Devices, Inc., Technical Support Request](#) for further recommendations.

BACK-TO-BACK APPLICATION

The switch control input pins, V1 and V2, can be connected together in a back-to-back application by hardwiring the LS pin of one device to GND and of one device to VDD as shown in [Figure 31](#).

APPLICATIONS INFORMATION

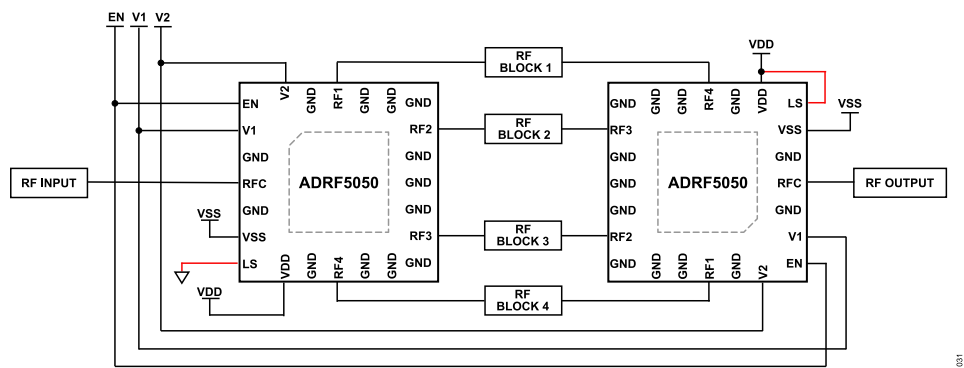


Figure 31. Back-to-Back Application Block Diagram

Table 8. Back-to-Back Application Truth Table

EN	V1	V2	Selected Path
Low	Low	Low	RF Block 1
Low	High	Low	RF Block 2
Low	Low	High	RF Block 3
Low	High	High	RF Block 4
High	Low or high	Low or high	Isolation (off)

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CC-24-16	LGA	24-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
ADRF5050BCCZN	-40°C to +105°C	24-Terminal Land Grid Array [LGA]	Tape, 500	CC-24-16	5050
ADRF5050BCCZN-R7	-40°C to +105°C	24-Terminal Land Grid Array [LGA]	Reel, 500	CC-24-16	5050

¹ Z = RoHS Compliant Part.

EVALUATION BOARDS

Model ¹	Description
ADRF5050-EVALZ	Evaluation Board

¹ Z = RoHS Compliant Part.