

Silicon SPST Switch, Nonreflective, 100 MHz to 55 GHz

FEATURES

- ▶ Ultra-wideband frequency range: 0.1 GHz to 55 GHz
- ▶ Nonreflective ports, high-power terminated path
- ▶ Symmetrical ports
- ▶ Low insertion loss
 - ▶ 1.0 dB typical to 20 GHz
 - ▶ 1.5 dB typical to 40 GHz
 - ▶ 2.0 dB typical to 55 GHz
- ▶ Isolation
 - ▶ 30 dB typical to 50 GHz
 - ▶ 28 dB typical to 55 GHz
- ▶ High input linearity
 - ▶ P0.1dB: >33 dBm typical
 - ▶ Input IP3 >60 dBm typical
- ▶ High power handling $T_{CASE} = 85^\circ\text{C}$
 - ▶ Through path
 - ▶ Peak: 36 dBm
 - ▶ Pulse: 33 dBm
 - ▶ CW: 30 dBm
 - ▶ Terminated path
 - ▶ Peak: 33 dBm
 - ▶ Pulse 33 dBm
 - ▶ CW: 30 dBm
 - ▶ Hot switching
 - ▶ Peak: 33 dBm
 - ▶ Pulse: 33 dBm
 - ▶ CW: 30 dBm
- ▶ Complementary metal-oxide semiconductor (CMOS)-/low voltage transistor-transistor logic (LVTTL)-compatible controls
- ▶ Radio frequency (RF) switching time: 30 ns
- ▶ RF settling time (0.1 dB final RF output): 50 ns
- ▶ Dual-supply operation: $\pm 3.3\text{ V}$
- ▶ **14-lead, 2.25 mm x 2.25 mm, LGA package**

APPLICATIONS

- ▶ Test and instrumentation
- ▶ Cellular infrastructure: 5G mmWave
- ▶ Military radios, radars, electronic countermeasures
- ▶ Microwave radios and very small aperture terminals
- ▶ Industrial scanners

FUNCTIONAL BLOCK DIAGRAM

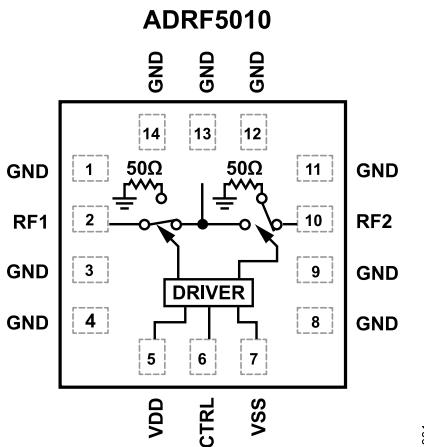


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5010 is a nonreflective, single-pole single-throw (SPST) switch manufactured in the silicon process.

The ADRF5010 operates from 0.1 GHz to 55 GHz with insertion loss of lower than 2 dB and isolation of higher than 28 dB. The device has an RF input power handling capability of 30 dBm for through path and 30 dBm for hot switching.

The ADRF5010 requires dual-supply voltages of $\pm 3.3\text{ V}$. The device employs CMOS- and LVTTL-compatible controls.

The ADRF5010 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. See [Table 2](#) for more details.

The ADRF5010 comes in a **14-lead, 2.25 mm x 2.25 mm, land grid array (LGA)** package and can operate from -40°C to $+105^\circ\text{C}$.

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REVISION HISTORY**9/2024—Revision 0: Initial Version**

SPECIFICATIONS

$V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, $V_{CTRL} = 0$ V or V_{DD} , $T_{CASE} = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted. RFx refers to RF1 or RF2.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1	55		GHz
INSERTION LOSS						
Between RFx and RFx (On)		0.1 GHz to 20 GHz 20 GHz to 40 GHz 40 GHz to 55 GHz		1.0 1.5 2.0		dB
ISOLATION						
Between RFx and RFx		0.1 GHz to 20 GHz 20 GHz to 40 GHz 40 GHz to 55 GHz		31 30 28		dB
RETURN LOSS						
RFx (Through path)		0.1 GHz to 20 GHz 20 GHz to 40 GHz 40 GHz to 55 GHz		20 19 21		dB
RFx (Terminated)		0.1 GHz to 55 GHz		22		dB
SWITCHING						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		27		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		30		ns
RF Settling Time (0.1dB)		50% V_{CTRL} to 0.1 dB of final RF output		50		ns
INPUT LINEARITY ¹						
Input Compression	$P_{0.1\text{dB}}$	$f = 0.1$ GHz to 55 GHz		33		dBm
Third-Order Intercept	IP3	Two-tone input power = 14 dBm each tone, $\Delta f = 1$ MHz		62		dBm
SUPPLY CURRENT						
Positive Supply Current	I_{DD}	V_{DD} and V_{SS} pins		140		μA
Negative Supply Current	I_{SS}			500		μA
DIGITAL CONTROL INPUTS		CTRL				
Voltage						
Low	V_{INL}		0	0.8		V
High	V_{INH}		1.2	3.3		V
Current						
Low	I_{INL} ,			<1		μA
High	I_{INH}			<1		μA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage						
Positive Supply Voltage	V_{DD}		3.15	3.45		V
Negative Supply Voltage	V_{SS}		-3.45	-3.15		V
Digital Control Inputs Voltage	V_{CTRL}		0	VDD		V
RF INPUT POWER ²		$f = 0.1$ GHz to 55 GHz, $T_{CASE} = 85^\circ\text{C}$				
Through Path	P_{IN} Peak ³ Pulse ⁴ CW Peak	RF signal is applied to RFx at Insertion Loss state		36 33 30 33		dBm
Terminated Path	Pulse CW Peak	RF signal is applied to RFx at Isolation state		33 30 33		dBm
Hot Switching	Pulse	RF signal is applied to RFx while switching in between Insertion Loss and Isolation states		33		dBm

SPECIFICATIONS**Table 1. Electrical Specifications (Continued)**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Case Temperature	CW T_{CASE}		-40	30 +85	30 +85	dBm °C

¹ For input linearity performance over frequency, see Figure 12 to Figure 15.

² For power derating over frequency, see Figure 2.

³ Peak: (≤ 100 ns pulse duration, 5% duty cycle).

⁴ Pulse: (> 100 ns pulse duration, 15% duty cycle).

SINGLE-SUPPLY OPERATION

$V_{DD} = 3.3$ V, $V_{SS} = 0$ V, $V_{CTRL} = 0$ V or V_{DD} , $T_{CASE} = 25^\circ\text{C}$ for $50\ \Omega$ system, unless otherwise noted. RFx refers to RF1 or RF2

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1	55		GHz
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		50		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		85		ns
Settling Time (0.1 dB)		50% V_{CTRL} to 0.1 dB of final RF output		120		ns
INPUT LINEARITY		$f = 0.1$ GHz to 55 GHz				
Input Compression	$P_{0.1\text{dB}}$			18		dBm
Third-Order Intercept	IP3	Two-tone input power = 6 dBm each tone, $f = 0.1$ GHz to 55 GHz, $\Delta f = 1$ MHz		53		dBm
RECOMMENDED OPERATING CONDITIONS						
RF Input Power	P_{IN}	$f = 0.1$ GHz to 55 GHz, $T_{CASE} = 85^\circ\text{C}$				
Through Path		RF signal is applied to RFx at Insertion Loss state			18	dBm
Terminated Path		RF signal is applied to RFx at Isolation state			18	dBm
Hot Switching		RF signal is applied to RFx while switching in between Insertion Loss and Isolation states			18	dBm

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see [Table 1](#).

Table 3. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	-0.3 V to +3.6 V
Negative Supply Voltage	-3.6 V to +0.3 V
Digital Control Input ¹	
Voltage	-0.3 V to $V_{DD} + 0.3$ V
Current	3 mA
RF Input Power, Dual Supply ² ($V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, $f = 0.1$ GHz to 55 GHz, $T_{CASE} = 85^\circ\text{C}$ ³)	
Through Path	37 dBm
Terminated Path	33.5 dBm
Hot Switching (RF1/2 to Termination)	33.5 dBm
RF Input Power, Single Supply ($V_{DD} = 3.3$ V, $V_{SS} = 0$ V, $f = 0.1$ GHz to 55 GHz, $T_{CASE} = 85^\circ\text{C}$ ³)	
Through Path	20 dBm
Terminated Path	20 dBm
Hot Switching (RF1/2 to Termination)	20 dBm
RF Input Power, Unbiased ($V_{DD}, V_{SS} = 0$ V)	30 dBm
Temperature	
Junction, T_J	135°C
Storage	-65°C to +150°C
Reflow	260°C

¹ Overvoltages at the digital control input are clamped by internal diodes. Current must be limited to the maximum rating given.

² For power derating over frequency, see [Figure 2](#).

³ For 105°C operation, the power handling degrades from the $T_{CASE} = 85^\circ\text{C}$ specification by 3 dB for dual supply.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at a time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction-to-case bottom (channel-to-package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC} ¹	Unit
CC-14-5	135	°C/W
	50	°C/W

¹ θ_{JC} was determined by simulation under the following conditions: The heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

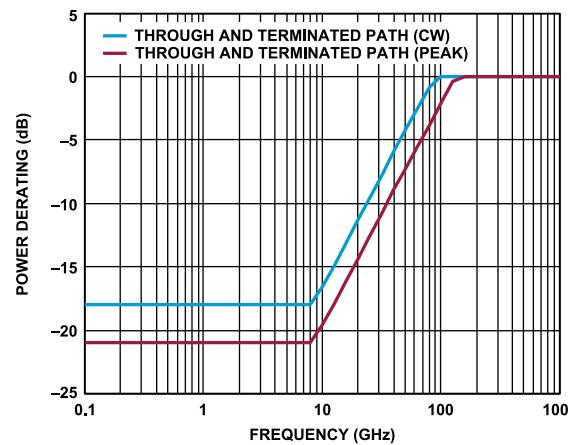


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE} = 85^\circ\text{C}$

ABSOLUTE MAXIMUM RATINGS**ELECTROSTATIC DISCHARGE (ESD) RATINGS**

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

Table 5. ADRF5010, 14-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	750 for RF pins	1B
	750 for supply and digital control pins	1B
CDM	500 for all pins	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

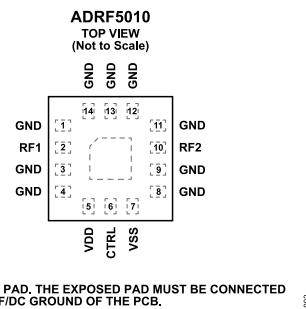


Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 8, 9, 11, 12, 13, 14	GND	Ground. These pins must be connected to the RF/DC ground of the PCB.
2	RF1	RF Port 1. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. For the interface schematic, see Figure 4.
5	V _{DD}	Positive Supply Voltage. For the interface schematic, see Figure 6.
6	CTRL	Control Input Voltage. For the interface schematic, see Figure 5.
7	V _{SS}	Negative Supply Voltage. For the interface schematic, see Figure 7.
10	RF2	RF Port 2. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. For the interface schematic, see Figure 4.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/DC ground of the PCB.

INTERFACE SCHEMATICS

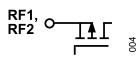


Figure 4. RF1, RF2 Pins Interface Schematic

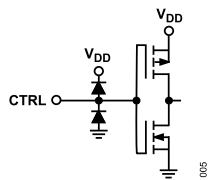
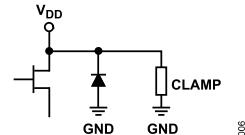
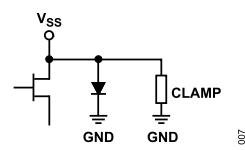


Figure 5. CTRL Pin Interface Schematic

Figure 6. V_{DD} Interface SchematicFigure 7. V_{SS} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, $V_{CTRL} = 0$ V or V_{DD} , $T_{CASE} = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted.

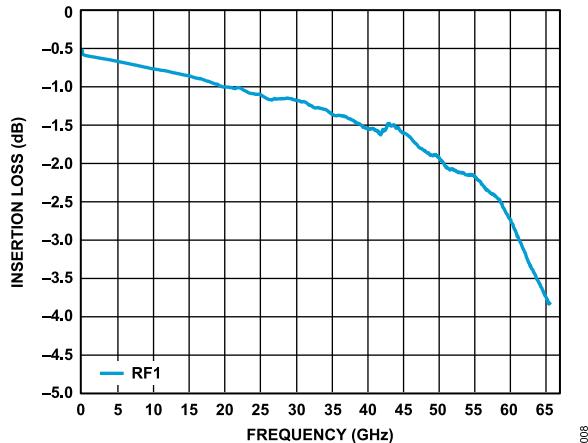


Figure 8. Insertion Loss vs. Frequency

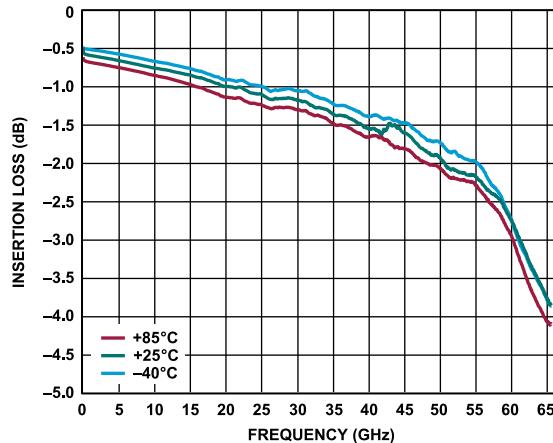


Figure 11. Insertion Loss vs. Frequency over Temperature

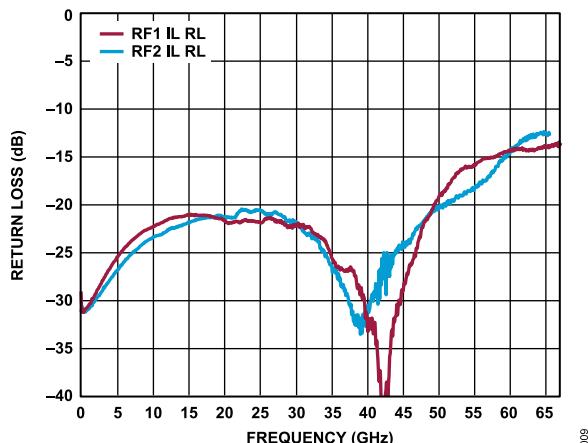


Figure 9. Return Loss vs. Frequency, Insertion Loss

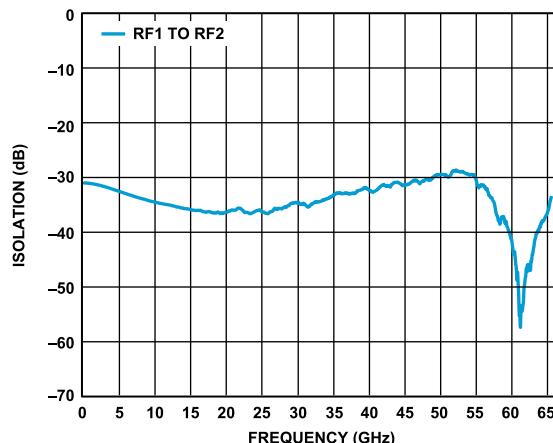


Figure 12. Isolation Loss vs. Frequency

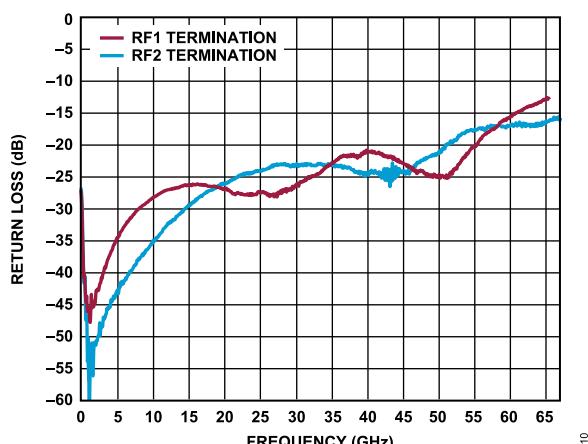
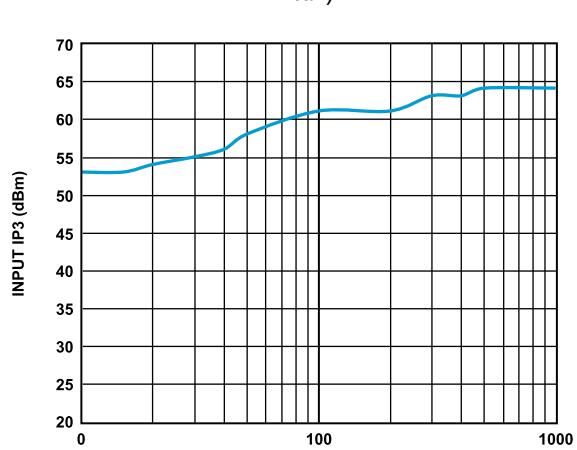
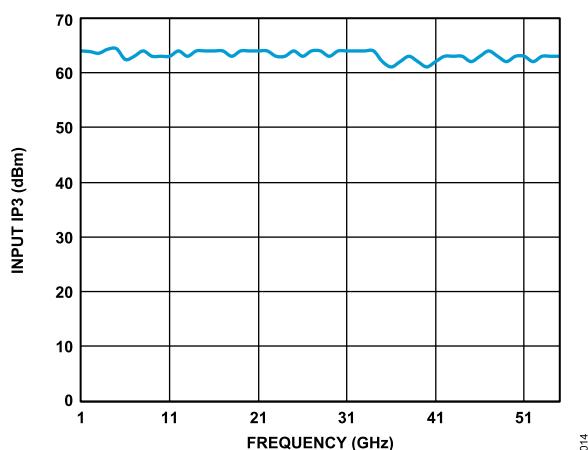
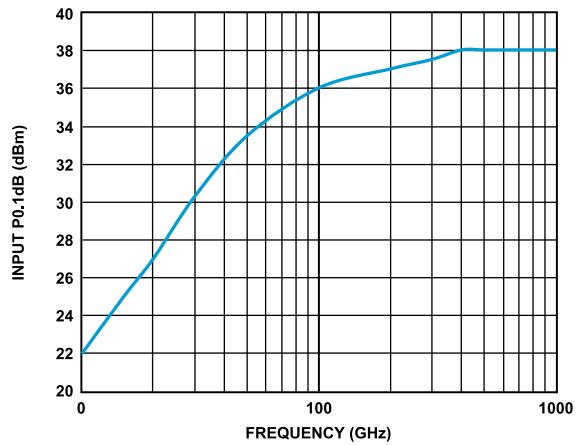
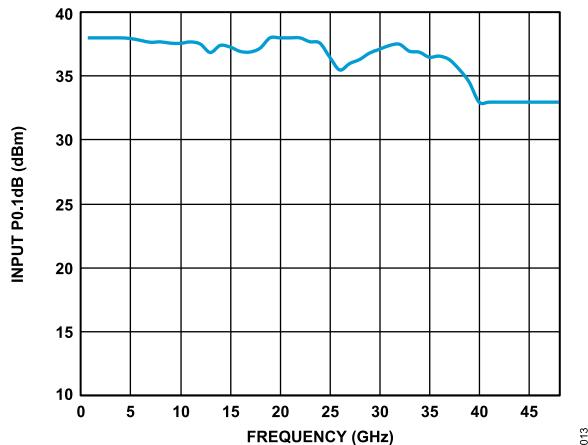


Figure 10. Return Loss vs. Frequency, Termination

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTRL} = 0\text{ V}$ or V_{DD} , $T_{CASE} = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted.



THEORY OF OPERATION

The ADRF5010 can interface CMOS-/LVTTL-compatible control interfaces directly.

CTRL determines which RF ports are in the insertion loss state and in the isolation state. For the control voltage truth table, see [Table 7](#).

RF INPUT AND OUTPUT

The RF ports (RF1 and RF2) are DC-coupled to 0 V and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to $50\ \Omega$. However, impedance matching on transmission lines can be used to improve insertion loss and return loss performances at high frequencies.

The ADRF5010 is bidirectional with equal power handling capabilities.

The insertion loss path conducts the RF signal between the RF1 and RF2 ports. The isolation path provides high loss between RF1 and RF2 ports which are $50\ \Omega$ terminated.

Table 7. Control Voltage Truth Table

Digital Control Input	RFx Paths
CTRL	RF1 to RF2
Low	Insertion loss (on)
High	Isolation (off)

The power handling of the ADRF5010 derates with frequency below 0.1 GHz. For derating of the RF power toward lower frequencies, see [Figure 2](#).

The ADRF5010 requires a positive supply voltage applied to the V_{DD} pin and a negative supply voltage applied to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up V_{DD} and V_{SS} . Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp-up.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply signals to the RF input ports.

APPLICATIONS INFORMATION

EVALUATION BOARD

The ADRF5010 has two power supply pins (V_{DD} and V_{SS}) and one control pin (CTRL). Figure 17 shows the external components and connections for the supply pin. The V_{DD} and V_{SS} pins are decoupled with a 100 pF multilayer ceramic capacitor. The device pin-out allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. For more details, see the [Pin Configuration and Function Description](#) section.

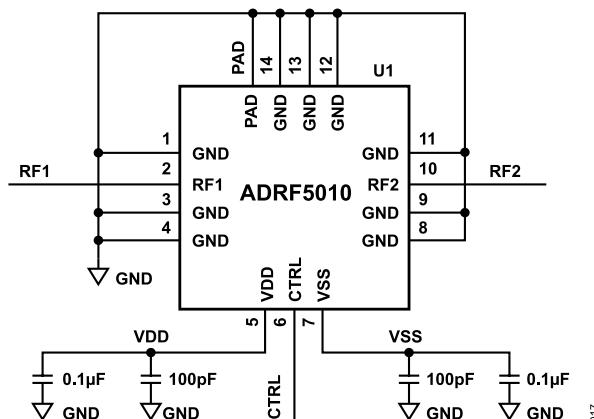


Figure 17. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 18 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003C dielectric material. The RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

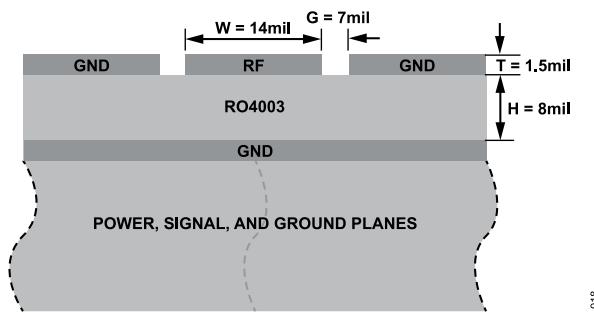


Figure 18. Example PCB Stack-Up

Figure 19 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

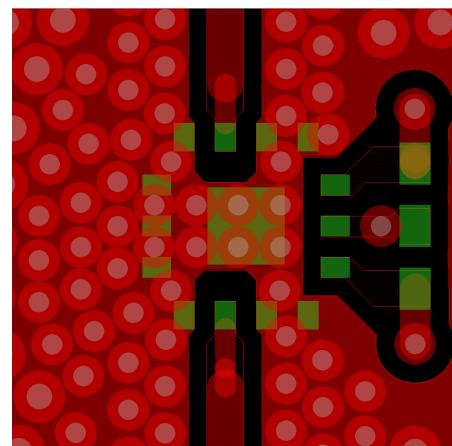


Figure 19. PCB Routing

Figure 20 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn soldermask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width until the package edge and tapered to RF trace. The paste mask is designed to match the device pads without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

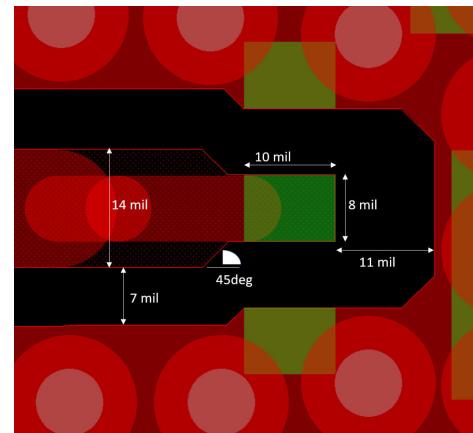


Figure 20. Recommended RF Pin Transition

For alternate PCB stack-ups with different dielectric thickness and RF trace design, and for further recommendations, contact [Technical Support](#).

OUTLINE DIMENSIONS

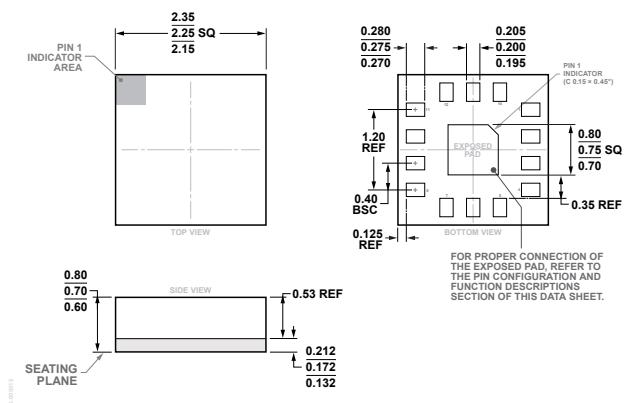


Figure 21. 14-Terminal Land Grid Array (LGA)
2.25 mm x 2.25 mm Body and 0.70 mm Package Height
(CC-14-5)
Dimensions Shown in Millimeters

Updated: September 04, 2024

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5010BCCZN	-40°C to +105°C	14-Terminal LGA (2.25 mm x 2.25 mm x 0.70 mm)		CC-14-5
ADRF5010BCCZN-R7	-40°C to +105°C	14-Terminal LGA (2.25 mm x 2.25 mm x 0.70 mm)	REEL, 1500	CC-14-5

¹ Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model ¹	Description
ADRF5010-EVALZ	Evaluation Board

¹ Z = RoHS-Compliant Part.