10 MHz to 26.5 GHz Amplifier with Bypass Switches

FEATURES

- Wideband amplifier with multiple bypass modes
- Broad operation from 10 MHz to 26.5 GHz
- Integrated power supply decoupling
- Four pin-selectable operating modes
  - Internal amplifier mode
  - Internal bypass mode
  - Two external bypass modes
- Reflective bypass switches
- Amplifier gain: 13.5 dB typical from 8 GHz to 14 GHz
- Amplifier OP1dB: 14.5 dBm typical from 8 GHz to 14 GHz
- Amplifier OIP3: 25.5 dBm typical from 8 GHz to 14 GHz
- Amplifier noise figure: 4 dB typical from 8 GHz to 14 GHz
- Bypass mode insertion loss: 3.4 dB typical from 8 GHz to 14 GHz
- Operating temperature range: −40°C to +85°C
- RoHS compliant, 6 mm × 6 mm, 28-terminal LGA

APPLICATIONS

- Electronic test and measurement equipment
- Electronic warfare
- Wireless receivers

FUNCTIONAL BLOCK DIAGRAM

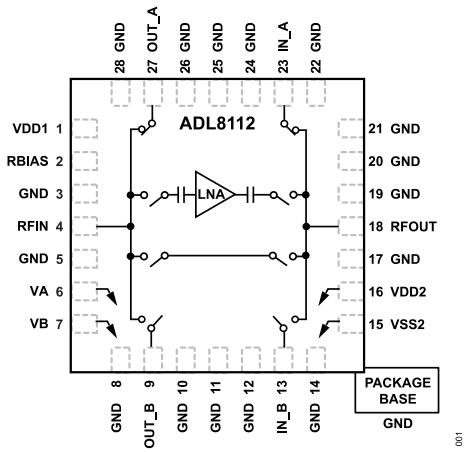

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADL8112 is a low noise amplifier (LNA) with bypass switches that provides broadband operation from 10 MHz to 26.5 GHz. The ADL8112 provides a low noise figure of 4 dB and an output third-order intercept point (OIP3) of 25.5 dBm. The ADL8112 provides a gain of 13.5 dB that is stable over frequency, temperature, power supply, and from device to device.

The integration of an amplifier and two single-pole, four-throw (SP4T) reflective switches allow multiple paths through the device. The addition of switches also offers a high third order input intercept (IIP3) path when large input signals are present. With the integration of power supply decoupling capacitors, minimal external power supply decoupling is required.

The ADL8112 is fully specified for operation across a temperature range of −40°C to +85°C. The ADL8112 is offered in a 6 mm x 6 mm, 28-terminal land grid array (LGA) package.

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Changes to Output 1 dB Compression (OP1dB) Parameter and Output Third-Order Intercept (OIP3) Parameter, Table 3 ... 3
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8/2024—Rev. 0 to Rev. A

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5/2023—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Power Supplies

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE				
Drain Bias Voltage (V_{DD1})	7.5	8.5	9.5	V
Positive Bias Voltage (V_{DD2})	3.0	3.3	3.6	V
Negative Bias Voltage (V_{SS2})	−3.6	−3.3	−3.0	V
SUPPLY CURRENT				
Total Current (I_{DD1}) at 8.5 V		90		mA
Amplifier Current (I_{DQ_AMP})		83		mA
RBIAS Current (I_{RBIAS})		7		mA
Positive Bias Current for the Switch (I_{DD2})		3		µA
Negative Bias Current for the Switch (I_{SS2})		-110		µA

Table 2. Logic Control Voltage (VA, VB)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL CONTROL INPUTS					
Low	<1 µA typical current	0		0.8	V
High	<35 µA typical current	1.2		V_{DD2}	V

0.01 GHZ TO 8 GHZ FREQUENCY RANGE

V_{DD1} = +8.5 V, quiescent drain supply current (I_{DQ}) = 90 mA, V_{SS2} = −3.3 V, V_{DD2} = +3.3 V, and T_A = 25°C, unless otherwise noted.

Table 3. 0.01 GHz to 8 GHz Frequency Range Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		0.01		8	GHz
INTERNAL AMPLIFIER MODE					
Small Signal Gain		12	14.5		dB
Gain Flatness			±0.5		dB
Input Return Loss			22		dB
Output Return Loss			14		dB
Output 1 dB Compression (OP1dB)		8.5	15.5		dBm
Output Third-Order Intercept (OIP3)			26.5		dBm
Noise Figure			4		dB
Switching Characteristics					
Rise (t_{RISE}) and Fall Time (t_{FALL})	10% to 90% of RF output		4		ns
On (t_{ON}) and Off Time (t_{OFF})	50% control voltage (VA or VB) to 90% of RF output		16		ns
RF Settling Time					
0.1 dB	50% VA or VB to 0.1 dB of final RF output		50		ns
0.05 dB	50% VA or VB to 0.05 dB of final RF output		60		ns
INTERNAL BYPASS SWITCH MODE					
Insertion Loss			2.7		dB
Input Return Loss			22		dB
Output Return Loss			22		dB
Input P1dB Compression (IP1dB)			28		dBm
Input P0.1dB Compression (IP0.1dB)			27.5		dBm
Input Third-Order Intercept (IIP3)			50		dBm
RF Settling Time					

SPECIFICATIONS

Table 3. 0.01 GHz to 8 GHz Frequency Range Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
0.1 dB	50% VA or VB to 0.1 dB of final RF output		50		ns
0.05 dB	50% VA or VB to 0.05 dB of final RF output		60		ns
Switching Characteristics					
Rise (t_{RISE}) and Fall Time (t_{FALL})	10% to 90% of RF output		4		ns
On (t_{ON}) and Off Time (t_{OFF})	50% control voltage (VA or VB) to 90% of RF output		16		ns
EXTERNAL BYPASS A AND EXTERNAL BYPASS B MODES					
Insertion Loss			1.4		dB
Input Return Loss On Mode			21		dB
Input Return Loss Off Mode			2		dB
Output Return Loss On Mode			22		dB
Output Return Loss Off Mode			2		dB
IP1dB			28		dBm
IP0.1dB			27.5		dBm
IIP3			50		dBm
Switching Characteristics					
Rise (t_{RISE}) and Fall Time (t_{FALL})	10% to 90% of RF output		3		ns
On (t_{ON}) and Off Time (t_{OFF})	50% VA or VB to 90% of RF output		16		ns
RF Settling Time					
0.1 dB	50% VA or VB to 0.1 dB of final RF output		50		ns
0.05 dB	50% VA or VB to 0.05 dB of final RF output		60		ns

8 GHZ TO 14 GHZ FREQUENCY RANGE

V_{DD1} = +8.5 V, I_{DQ} = 90 mA, V_{SS2} = −3.3 V, V_{DD2} = +3.3 V, and T_A = 25°C, unless otherwise noted.

Table 4. 8 GHz to 14 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit
OVERALL FUNCTION				
Frequency Range	8		14	GHz
INTERNAL AMPLIFIER MODE				
Small Signal Gain	11.5	13.5		dB
Gain Flatness		±0.5		dB
Input Return Loss		17		dB
Output Return Loss		16		dB
OP1dB	7.5	14.5		dBm
OIP3		25.5		dBm
Noise Figure		4		dB
INTERNAL BYPASS SWITCH MODE				
Insertion Loss		3.4		dB
Input Return Loss		17		dB
Output Return Loss		18		dB
IIP3		50		dBm
IP0.1dB		27.5		dBm
IP1dB		28		dBm
EXTERNAL BYPASS A AND EXTERNAL BYPASS B MODES				
Insertion Loss		2.0		dB
Input Return Loss On Mode		21		dB

SPECIFICATIONS

Table 4. 8 GHz to 14 GHz Frequency Range Specifications (Continued)

Parameter	Min	Typ	Max	Unit
Input Return Loss Off Mode		3		dB
Output Return Loss On Mode		20		dB
Output Return Loss Off Mode		3		dB
IIP3		50		dBm
IP0.1dB		27.5		dBm
IP1dB		28		dBm

14 GHZ TO 20 GHZ FREQUENCY RANGE

V_{DD1} = +8.5 V, I_{DQ} = 90 mA, V_{SS2} = −3.3 V, V_{DD2} = +3.3 V, and T_A = 25°C, unless otherwise noted.

Table 5. 14 GHz to 20 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit
OVERALL FUNCTION				
Frequency Range	14		20	GHz
INTERNAL AMPLIFIER MODE				
Small Signal Gain	11	13.5		dB
Gain Flatness		±0.4		dB
Input Return Loss		22		dB
Output Return Loss		15		dB
OP1dB	5.75	13		dBm
OIP3		23.5		dBm
Noise Figure		5.5		dB
INTERNAL BYPASS SWITCH MODE				
Insertion Loss		3.8		dB
Input Return Loss		21		dB
Output Return Loss		22		dB
IP1dB		28		dBm
IP0.1dB		27.5		dBm
IIP3		50		dBm
EXTERNAL BYPASS A AND EXTERNAL BYPASS B MODES				
Insertion Loss		2.3		dB
Input Return Loss On Mode		16		dB
Input Return Loss Off Mode		4		dB
Output Return Loss On Mode		18		dB
Output Return Loss Off Mode		4		dB
IP1dB		28		dBm
Input 0.5 dB Compression (IP0.5dB)		27.5		dBm
IIP3		50		dBm

20 GHZ TO 24 GHZ FREQUENCY RANGE

V_{DD1} = 8.5 V, I_{DQ} = 90 mA, V_{SS2} = −3.3 V, V_{DD2} = +3.3 V, and T_A = 25°C, unless otherwise noted.

Table 6. 20 GHz to 24 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit
OVERALL FUNCTION				
Frequency Range	20		24	GHz
INTERNAL AMPLIFIER MODE				

SPECIFICATIONS

Table 6. 20 GHz to 24 GHz Frequency Range Specifications (Continued)

Parameter	Min	Typ	Max	Unit
Small Signal Gain	9.5	13.4		dB
Gain Flatness		±0.6		dB
Input Return Loss		18		dB
Output Return Loss		18		dB
OP1dB	4	11		dBm
OIP3		20.5		dBm
Noise Figure		6.5		dB
INTERNAL BYPASS SWITCH MODE				
Insertion Loss		4.25		dB
Input Return Loss		23		dB
Output Return Loss		21		dB
IP1dB		28		dBm
IP0.1dB		27.5		dBm
IIP3		50		dBm
EXTERNAL BYPASS A AND EXTERNAL BYPASS B MODES				
Insertion Loss		2.5		dB
Input Return Loss On Mode		23		dB
Input Return Loss Off Mode		4		dB
Output Return Loss On Mode		18		dB
Output Return Loss Off Mode		4		dB
IP1dB		28		dBm
IP0.1dB		27.5		dBm
IIP3		50		dBm

24 GHZ TO 26.5 GHZ FREQUENCY RANGE

V_{DD1} = 8.5 V, I_{DQ} = 90 mA, V_{SS2} = −3.3 V, V_{DD2} = +3.3 V, and T_A = 25°C, unless otherwise noted.

Table 7. 24 GHz to 26.5 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit
OVERALL FUNCTION				
Frequency Range	24		26.5	GHz
INTERNAL AMPLIFIER MODE				
Small Signal Gain		11.8		dB
Gain Flatness		±1.0		dB
Input Return Loss		17		dB
Output Return Loss		17		dB
OP1dB	4	9		dBm
OIP3		17.5		dBm
Noise Figure		8.0		dB
V_{DD1}	7.5	8.5	9.5	V
INTERNAL BYPASS SWITCH MODE				
Insertion Loss		4.8		dB
Input Return Loss		23		dB
Output Return Loss		17		dB
IP1dB		28		dBm
IP0.1dB		27		dBm
IIP3		50		dBm

SPECIFICATIONS

Table 7. 24 GHz to 26.5 GHz Frequency Range Specifications (Continued)

Parameter	Min	Typ	Max	Unit
EXTERNAL BYPASS A AND EXTERNAL BYPASS B MODES				
Insertion Loss		3.0		dB
Input Return Loss On Mode		17		dB
Input Return Loss Off Mode		4		dB
Output Return Loss On Mode		17		dB
Output Return Loss Off Mode		4		dB
IP1dB		28		dBm
IP0.1dB		27.5		dBm
IIP3		50		dBm

ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
V_{DD1}	11.5 V
V_{DD2}	−0.3 V to +3.6 V
V_{SS2}	−3.6 V to +0.3 V
Control Voltage (VA, VB) Range	±0.3 V to VDD2
RF Input Power (RFIN) (Derate at Lower Frequencies, According to Figure 2)	
Internal Amplifier Mode	23 dBm
Internal/External Bypass Mode	27.5 dBm
Hot Switch Power Level	22 dBm
Internal Amplifier Mode	
External/Internal Switch Mode	27.5 dBm
Continuous Power Dissipation (P_{DISS})	0.98 W
Temperature	
Channel	175°C
Storage Range	−40°C to +125°C
Operating Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 9. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-28-4	92	°C/W

RF INPUT POWER DERATING CURVE

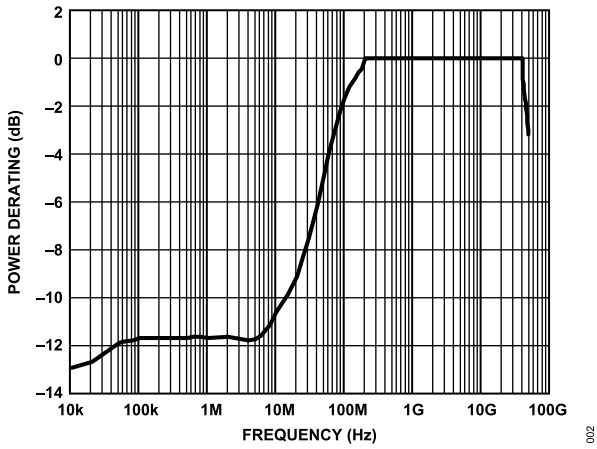

Figure 2. RF Input Power Derating Curve

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8112

Table 10. ADL8112, 28-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

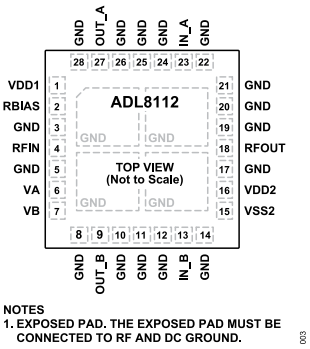

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD1	Drain Bias Voltage. See Figure 5 for the interface schematic.
2	RBIAS	Current Mirror Bias Resistor Pin. Use this pin to set the current to the internal resistor by the external resistor. See Figure 10 for the interface schematic.
3, 5, 8, 10 to 12, 14, 17, 19 to 22, 24 to 26, 28	GND	RF and DC Ground. See Figure 4 for the interface schematic.
4	RFIN	RF Input. This pin is DC-coupled and matched to 50 Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0 V DC. See Figure 11 for the interface schematic.
6, 7	VA , VB	Control Input. See Figure 8 and Figure 9 for the interface schematics.
9, 13	OUT_B, IN_B	External Bypass Path B. These pins are DC-coupled and matched to 50 Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0 V DC. See Figure 11 for the interface schematic.
15	VSS2	Negative Bias Voltage for the Switch.
16	VDD2	Positive Bias Voltage for the Switch.
18	RFOUT	RF Output. This pin is DC-coupled and matched to 50 Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0 V DC. See Figure 11 for the interface schematic
23, 27	IN_A, OUT_A	External Bypass Path A. These pins are DC-coupled and matched to 50 Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0 V DC. See Figure 11 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and DC ground.

INTERFACE SCHEMATICS

Figure 4. GND Interface Schematic

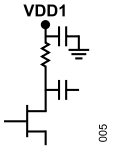

Figure 5. VDD1 Interface Schematic

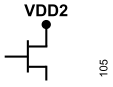

Figure 6. VDD2 Interface Schematic

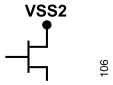

Figure 7. VSS2 Interface Schematic

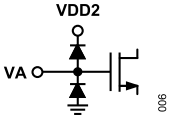

Figure 8. VA Interface Schematic

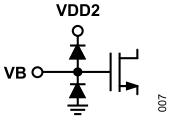

Figure 9. VB Interface Schematic

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

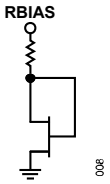

Figure 10. RBIAS Interface Schematic

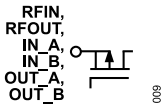

Figure 11. RFIN, RFOUT, IN_A, IN_B, OUT_A and OUT_B Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INTERNAL AMPLIFIER MODE

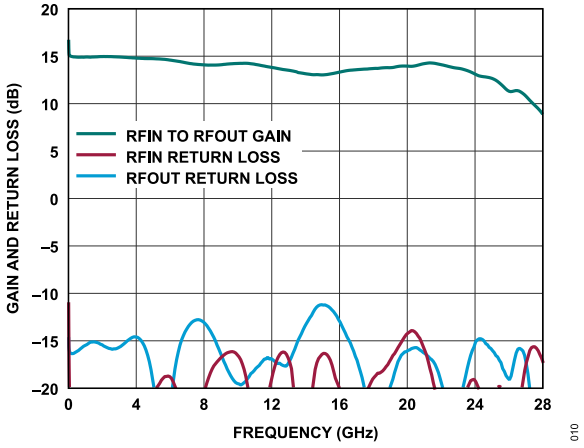

Figure 12. Gain and Return Loss vs. Frequency, 10 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

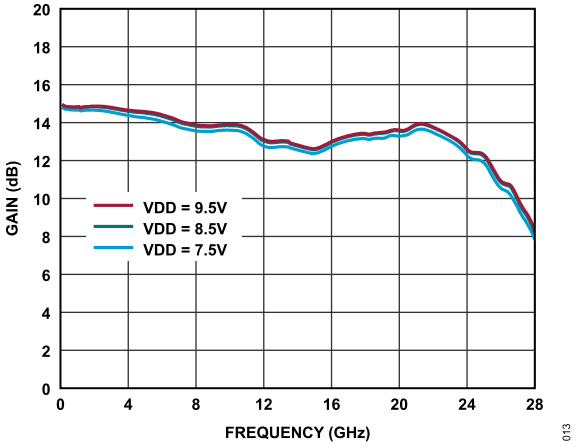

Figure 15. Gain vs. Frequency Over V_{DD}, I_{DQ} = 90 mA, 100 MHz to 28 GHz, Mode = Internal Amplifier

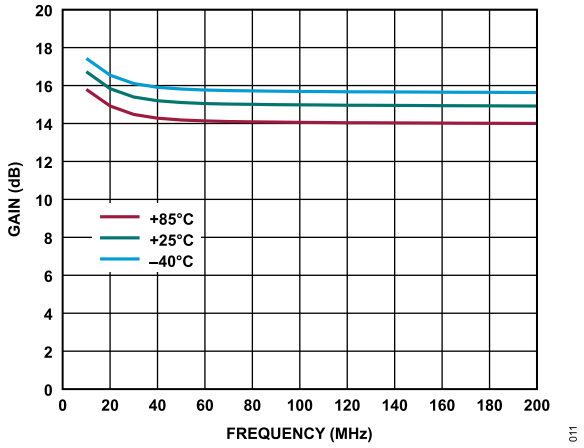

Figure 13. Gain vs. Frequency Over Temperature, 10 MHz to 200 MHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

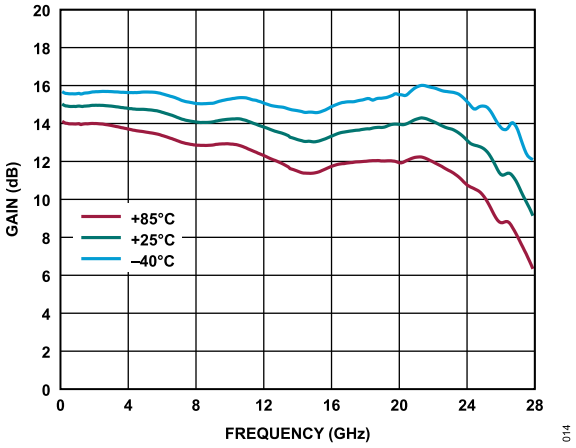

Figure 16. Gain vs. Frequency Over Temperature, 200 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

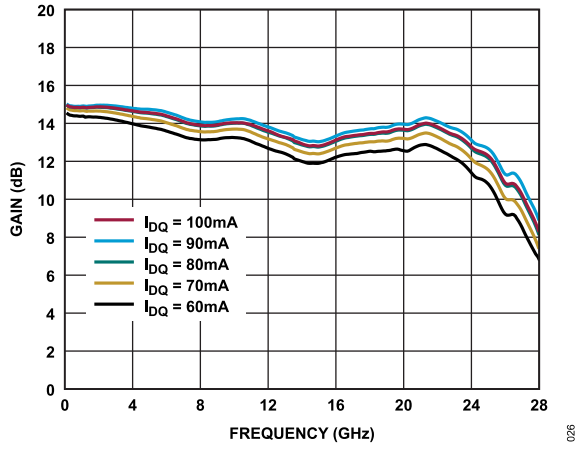

Figure 14. Gain vs. Frequency Over I_{DQ}, 100 MHz to 28 GHz, V_{DD} = 8.5 V, Mode = Internal Amplifier

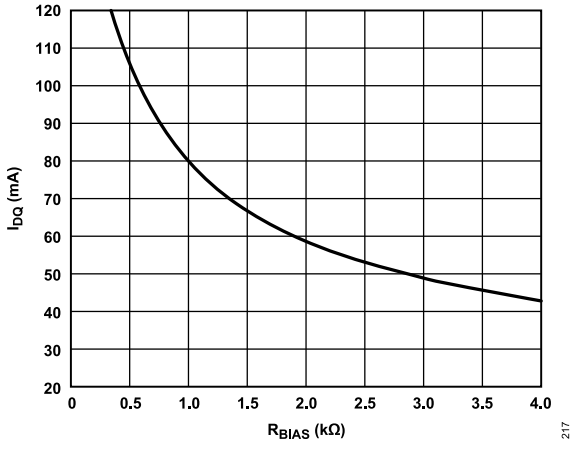

Figure 17. I_{DQ} vs. RBIAS, V_{DD} = 8.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

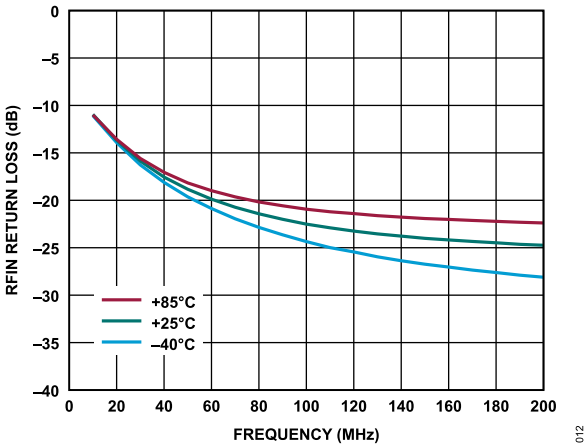

Figure 18. RFIN Return Loss vs. Frequency Over Temperature, 10 MHz to 200 MHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

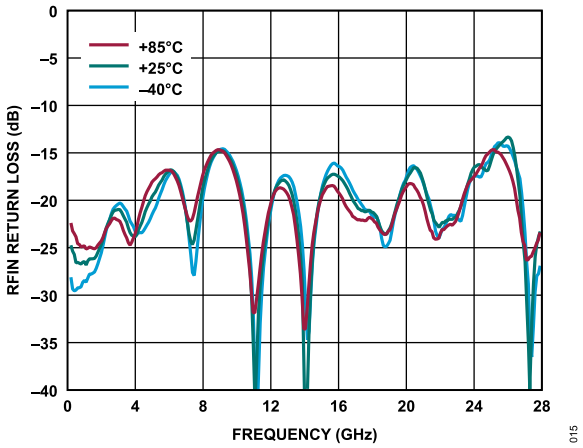

Figure 21. RFIN Return Loss vs. Frequency Over Temperature, 200 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

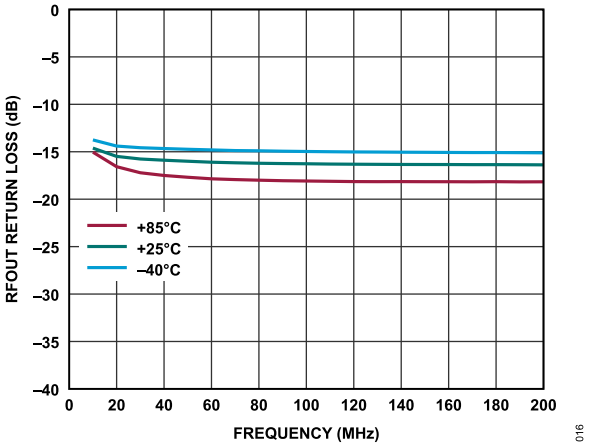

Figure 19. RFOUT Return Loss vs. Frequency Over Temperature, 10 MHz to 200 MHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

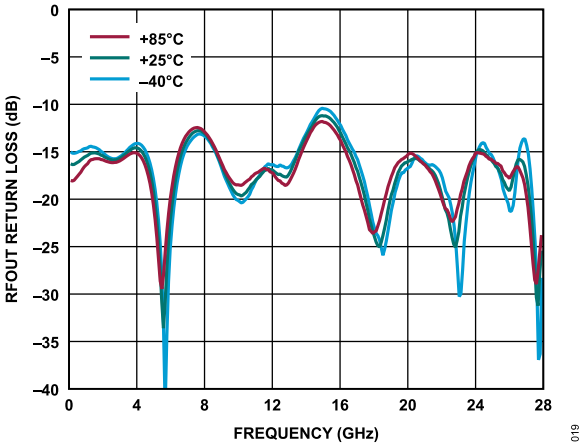

Figure 22. RFOUT Return Loss vs. Frequency Over Temperature, 200 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

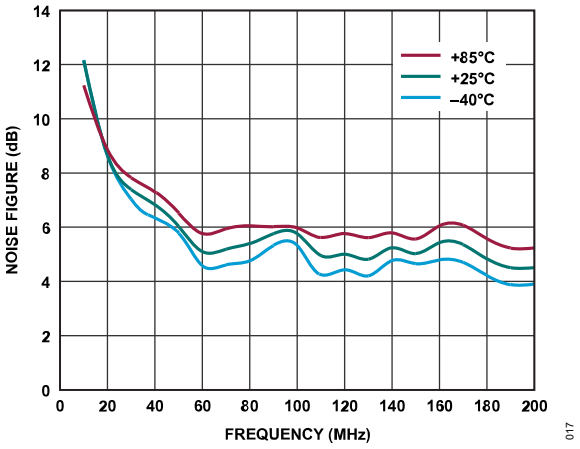

Figure 20. Noise Figure vs. Frequency Over Temperature, 10 MHz to 200 MHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

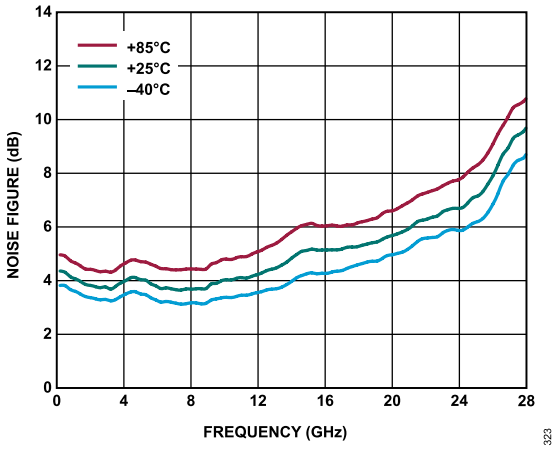

Figure 23. Noise Figure vs. Frequency Over Temperature, 200 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

TYPICAL PERFORMANCE CHARACTERISTICS

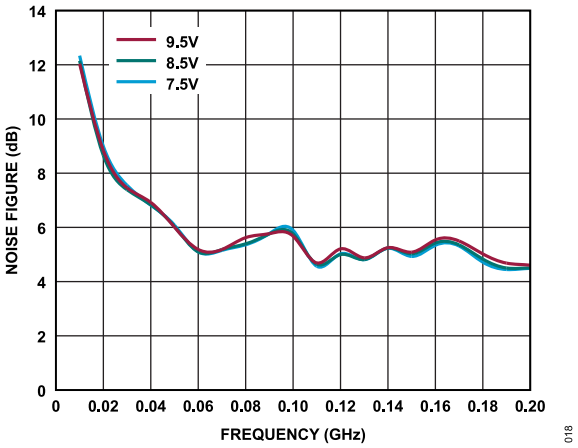

Figure 24. Noise Figure vs. Frequency Over V_{DD}, 10 MHz to 200 MHz, I_{DQ} = 90 mA, Mode = Internal Amplifier

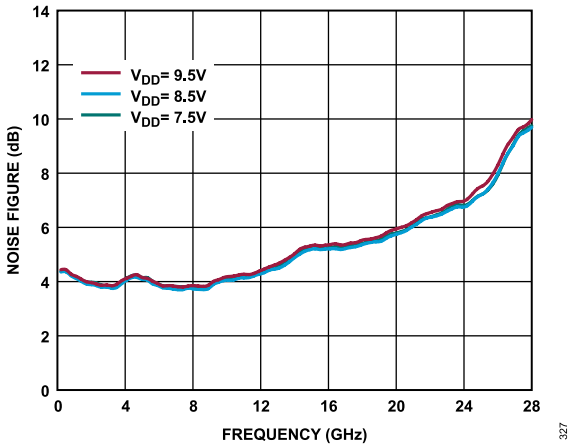

Figure 27. Noise Figure vs. Frequency Over V_{DD}, 200 MHz to 28 GHz, I_{DQ} = 90 mA, Mode = Internal Amplifier

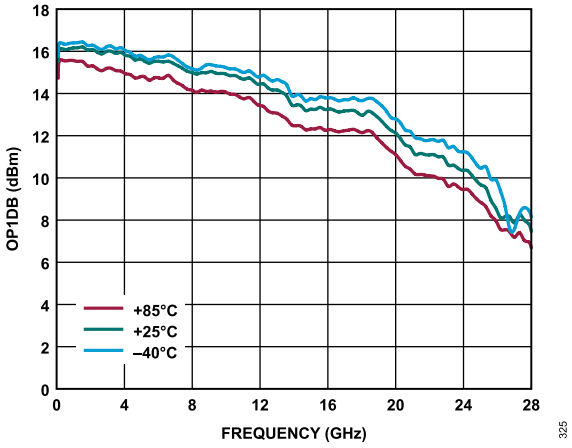

Figure 25. OP1dB vs. Frequency Over Temperature, 100 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

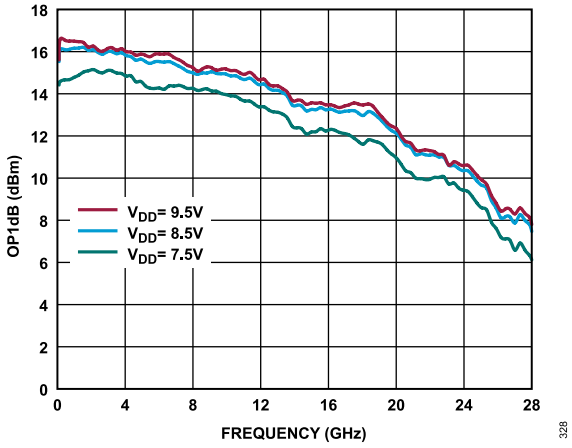

Figure 28. OP1dB vs. Frequency Over V_{DD}, 100 MHz to 28 GHz, I_{DQ} = 90 mA, Mode = Internal Amplifier

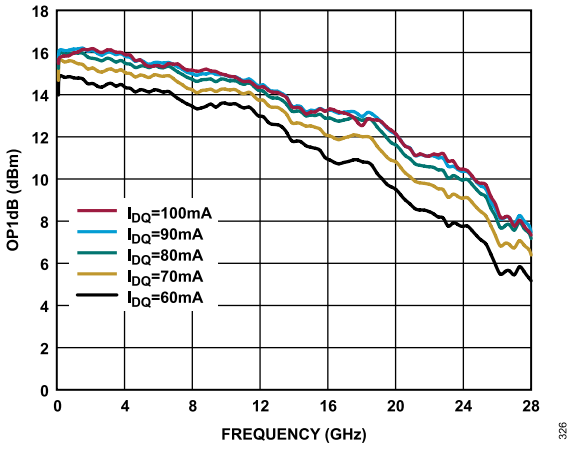

Figure 26. OP1dB vs. Frequency Over I_{DQ}, 100 MHz to 28 GHz, V_{DD} = 8.5 V, Mode = Internal Amplifier

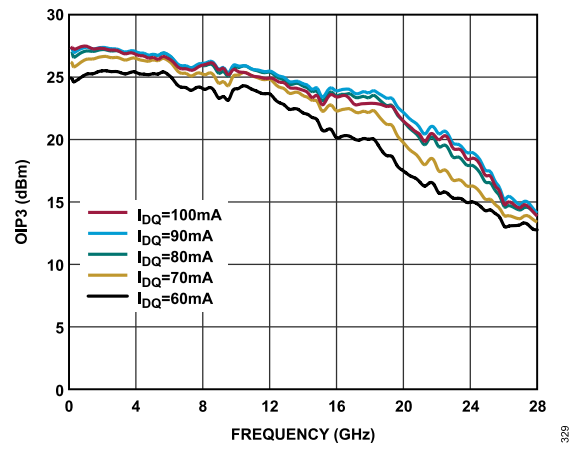

Figure 29. OIP3 vs. Frequency Over I_{DQ}, 100 MHz to 28 GHz, V_{DD} = 8.5 V, Mode = Internal Amplifier

TYPICAL PERFORMANCE CHARACTERISTICS

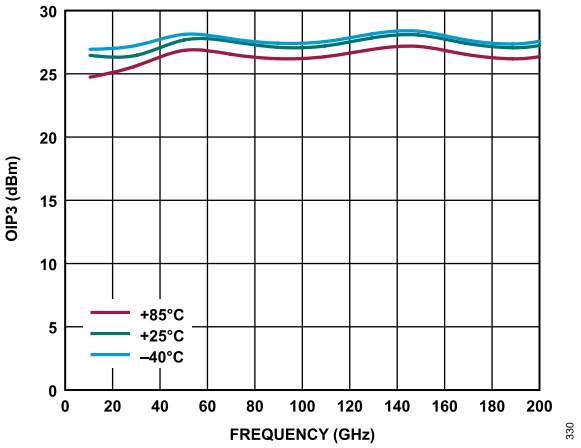

Figure 30. OIP3 vs. Frequency Over Temperature, 10 MHz to 200 MHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

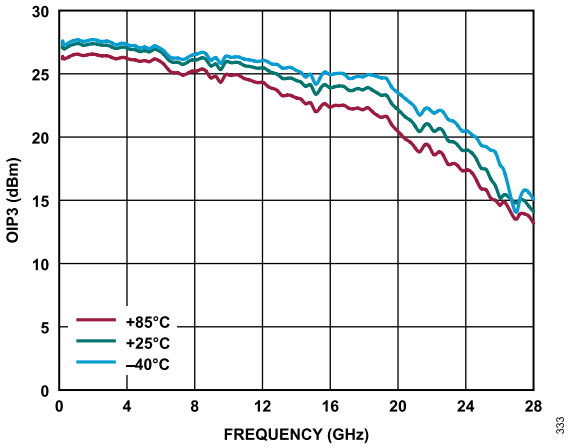

Figure 33. OIP3 vs. Frequency Over Temperature, 200 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

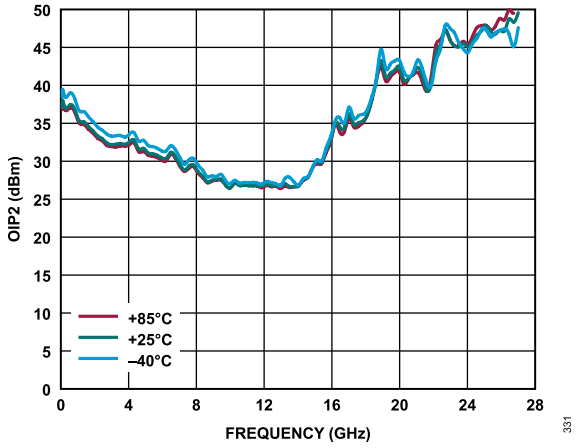

Figure 31. OIP2 vs. Frequency Over Temperature, 100 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

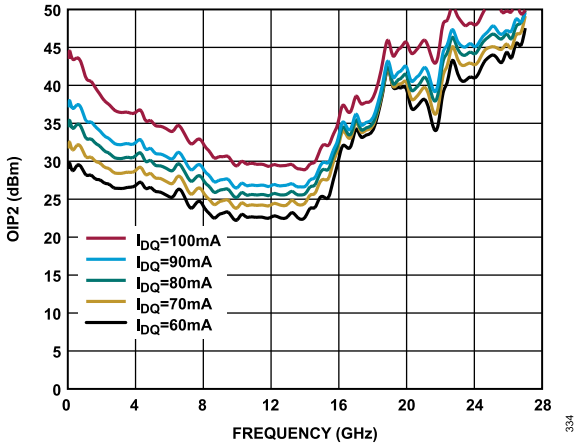

Figure 34. OIP2 vs. Frequency Over I_{DQ}, 100 MHz to 28 GHz, V_{DD} = 8.5 V, Mode = Internal Amplifier

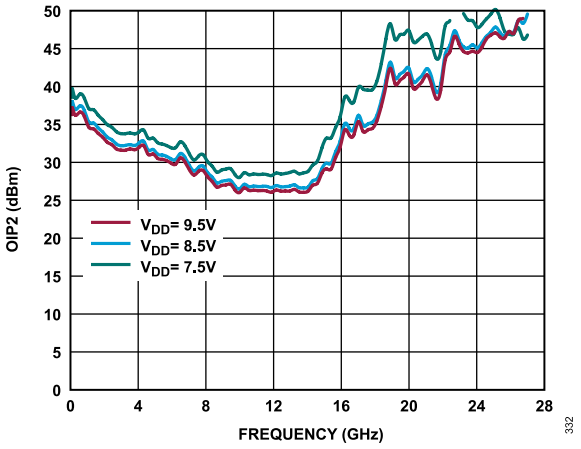

Figure 32. OIP2 vs. Frequency Over V_{DD}, 100 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

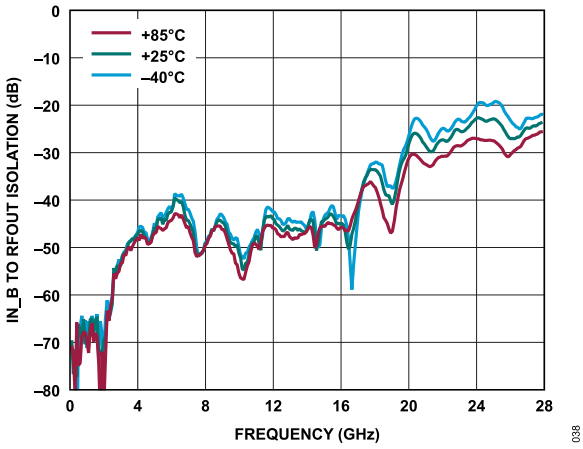

Figure 35. IN_B to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

TYPICAL PERFORMANCE CHARACTERISTICS

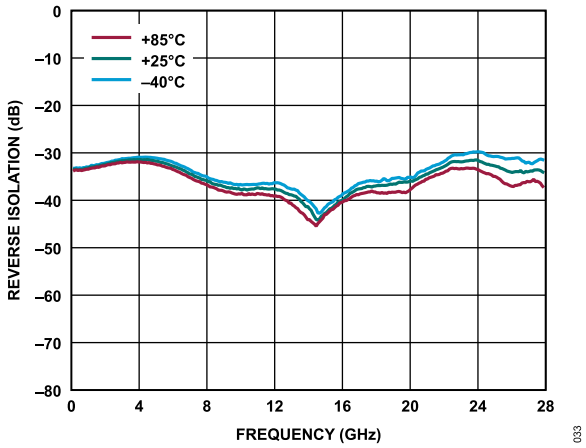

Figure 36. Reverse Isolation vs. Frequency Over Temperature, 200 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

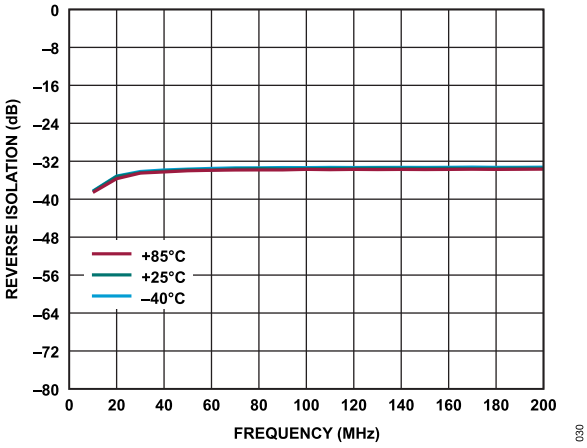

Figure 37. Reverse Isolation vs. Frequency Over Temperature, 10 MHz to 200 MHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

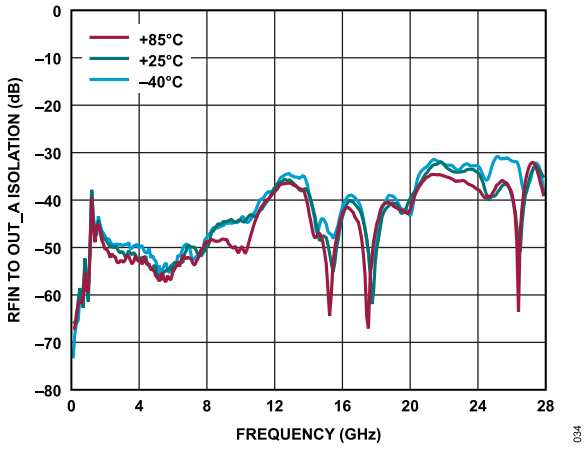

Figure 38. RFIN to OUT_A Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

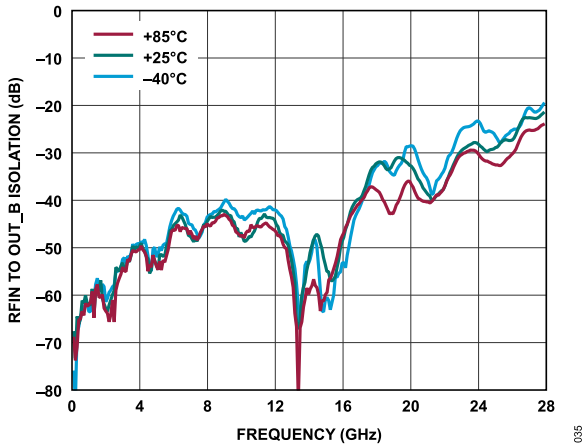

Figure 39. RFIN to OUT_B Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

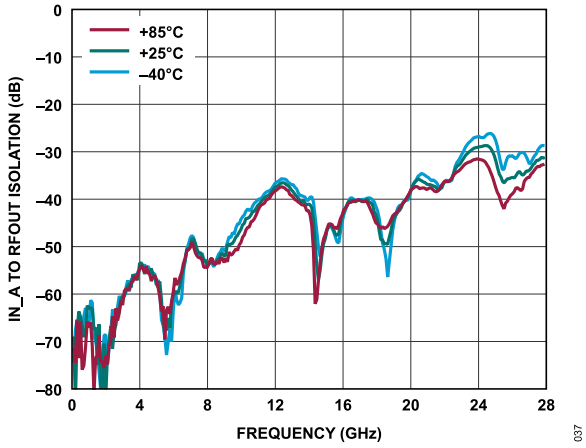

Figure 40. IN_A to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, V_{DD} = 8.5 V, I_{DQ} = 90 mA, Mode = Internal Amplifier

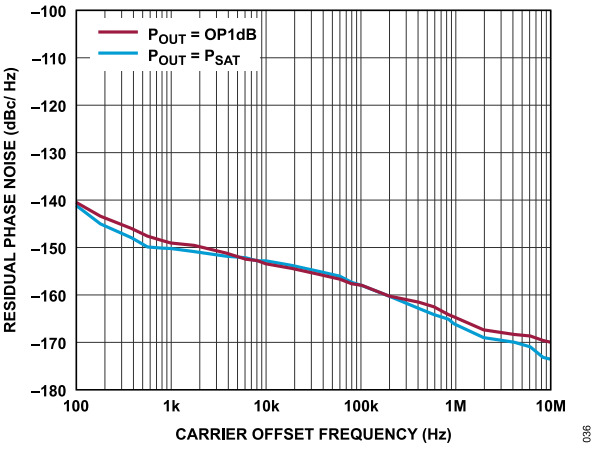

Figure 41. Phase Noise at 5 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

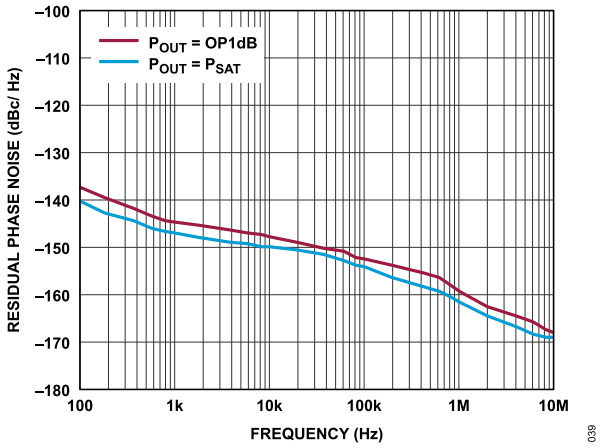

Figure 42. Phase Noise at 10 GHz

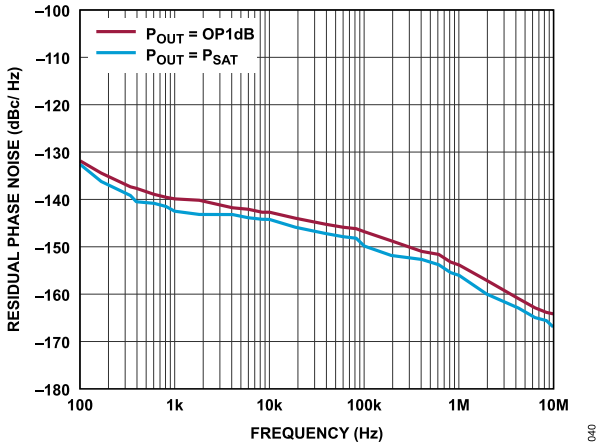

Figure 43. Phase Noise at 20 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

INTERNAL BYPASS MODE

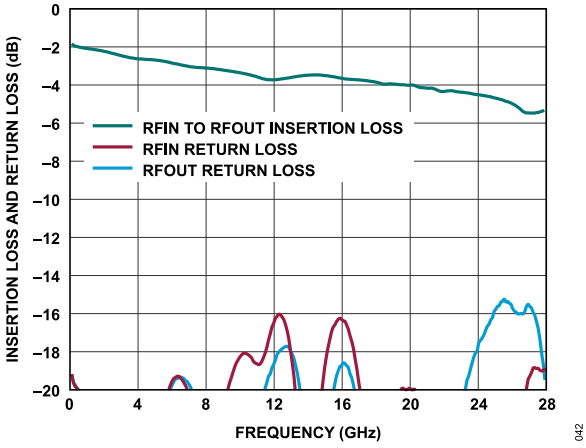

Figure 44. Insertion Loss and Return Loss vs. Frequency, 100 MHz to 28 GHz, Mode = Internal Bypass

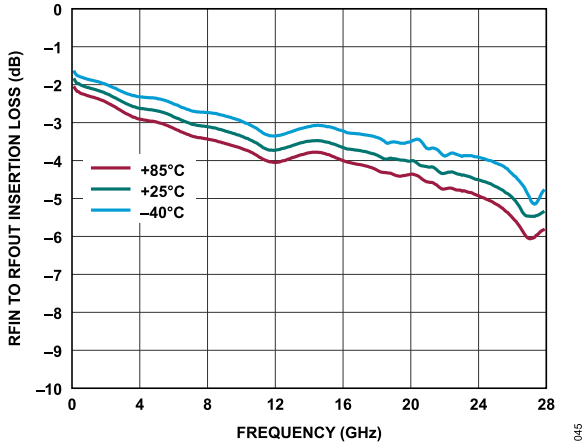

Figure 47. RFIN to RFOUT Insertion Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass

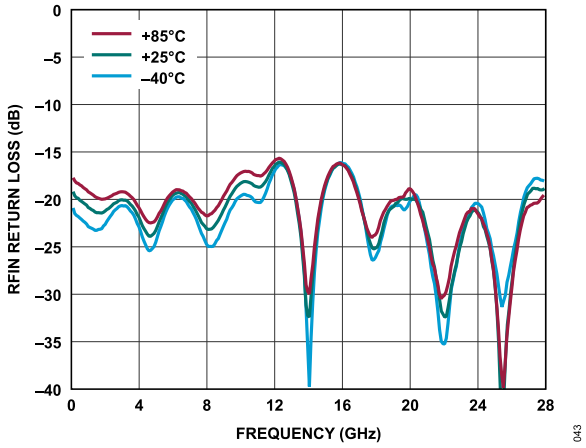

Figure 45. RFIN Return Loss vs. Frequency, Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass

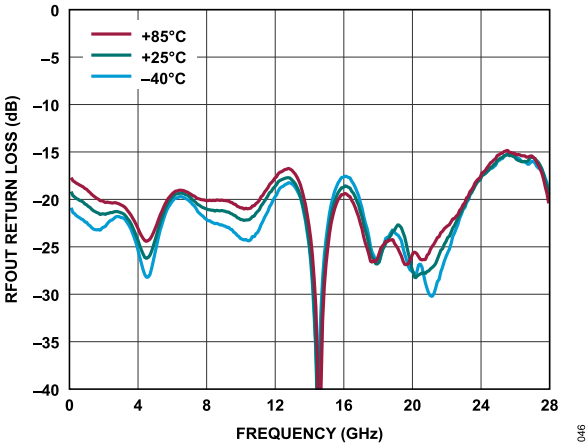

Figure 48. RFOUT Return Loss vs. Frequency, Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass

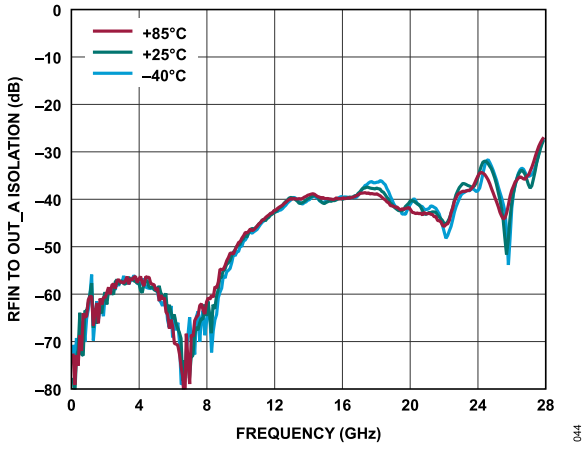

Figure 46. RFIN to OUT_A Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass

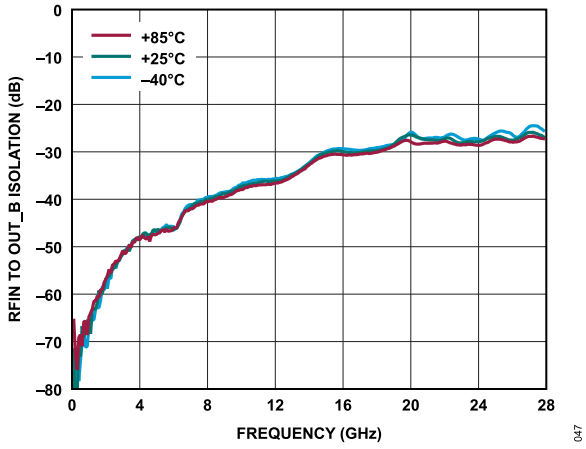

Figure 49. RFIN to OUT_B Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass

TYPICAL PERFORMANCE CHARACTERISTICS

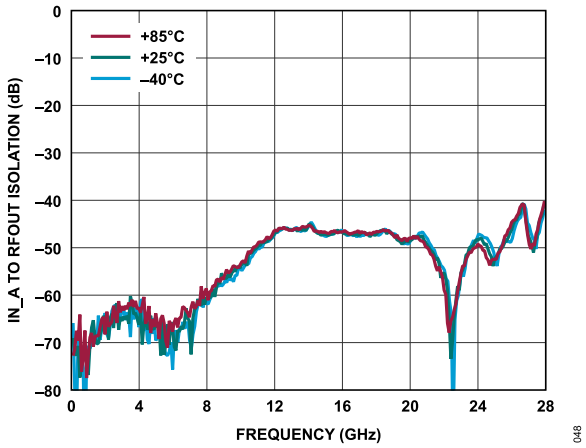

Figure 50. IN_A to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass

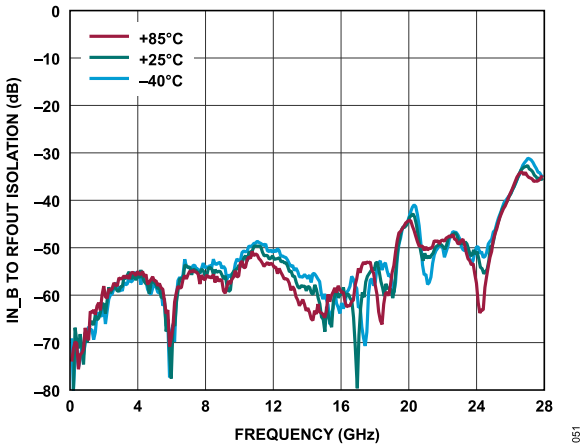

Figure 53. IN_B to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass

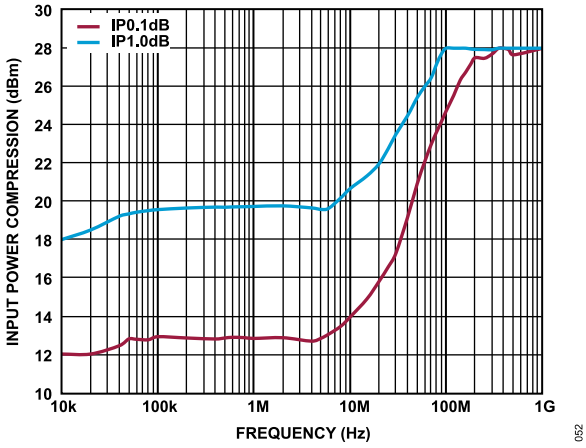

Figure 51. Input Power Compression vs. Frequency Over Temperature, 10 kHz to 1 GHz Mode = Internal Bypass and External Bypass A and B Paths

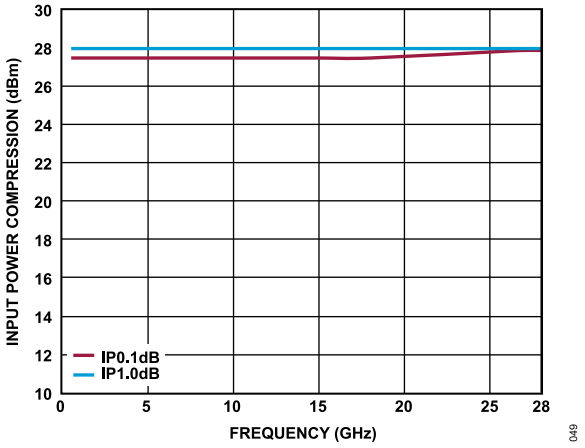

Figure 54. Input Power Compression vs. Frequency Over Temperature, 100 MHz to 28 GHz Mode = Internal Bypass and External Bypass A and B Paths

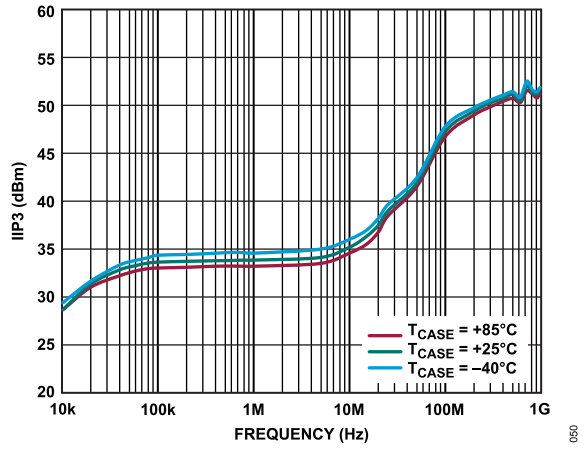

Figure 52. IIP3 vs. Frequency Over Temperature, 10 kHz to 1 GHz, Mode = Internal Bypass and External Bypass A and B Paths

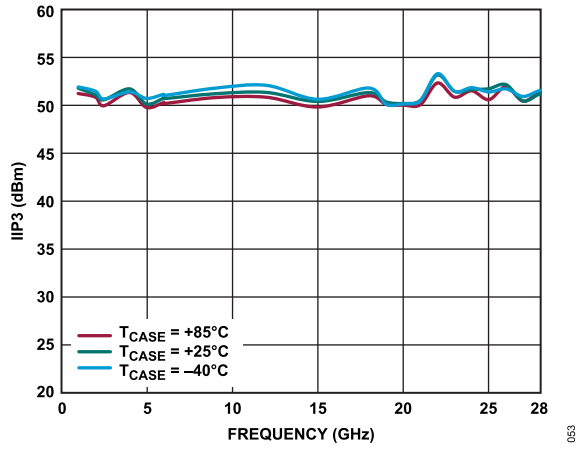

Figure 55. IIP3 vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = Internal Bypass and External A and B Paths

TYPICAL PERFORMANCE CHARACTERISTICS

EXTERNAL BYPASS A MODE

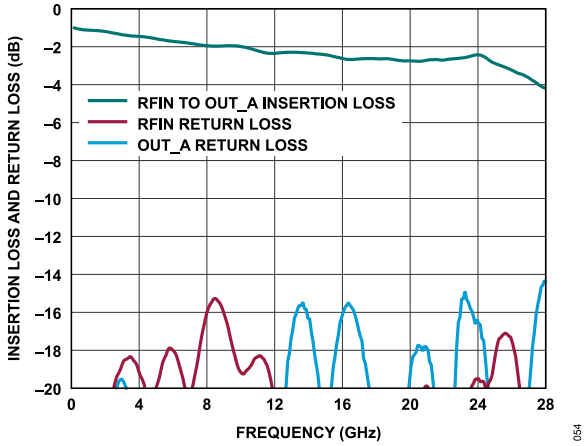

Figure 56. Insertion Loss and Return Loss vs. Frequency, 100 MHz to 28 GHz, Mode = External Bypass A

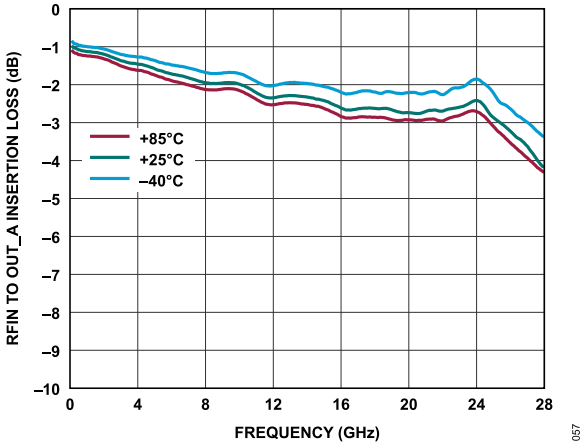

Figure 59. RFIN to OUT_A Insertion Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

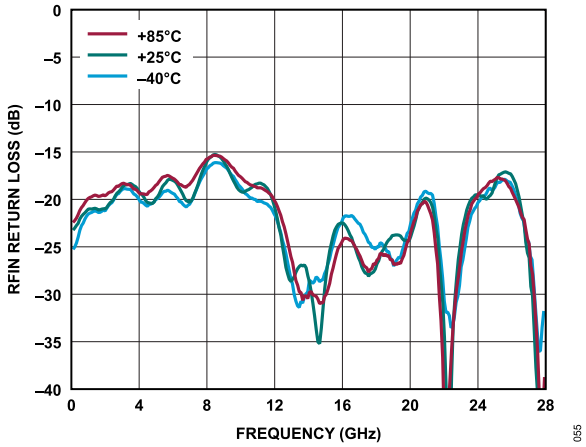

Figure 57. RFIN Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

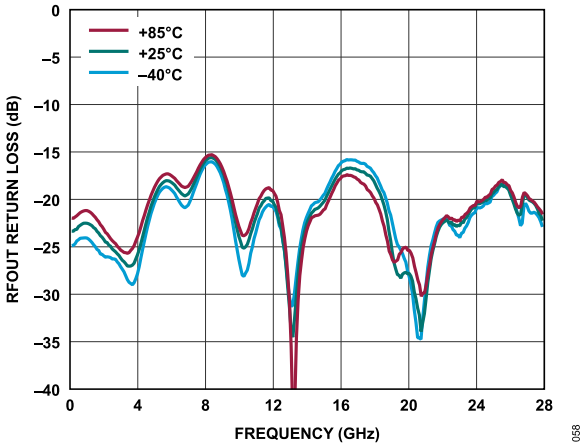

Figure 60. RFOUT Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

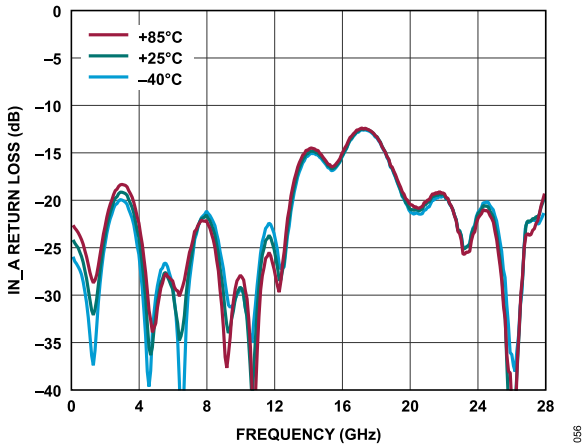

Figure 58. IN_A Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

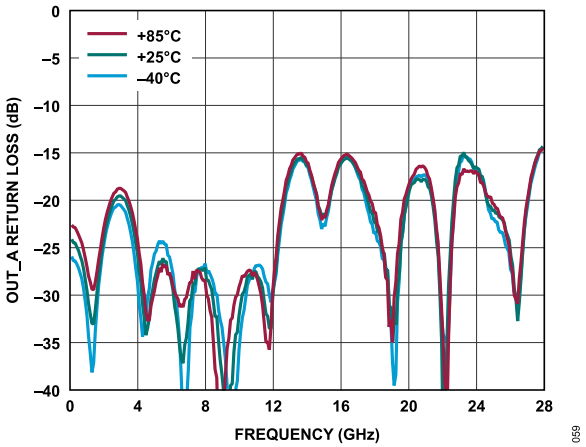

Figure 61. OUT_A Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

TYPICAL PERFORMANCE CHARACTERISTICS

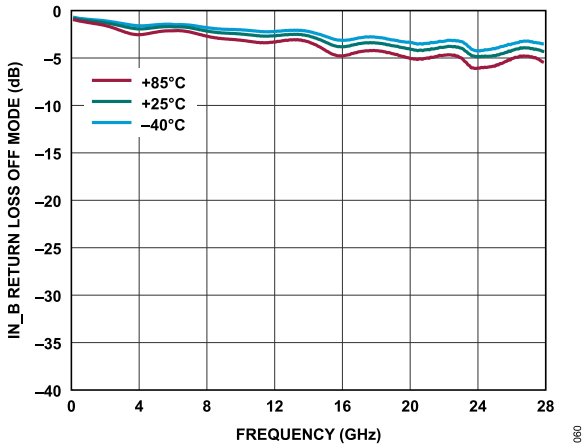

Figure 62. IN_B Return Loss Off Mode vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

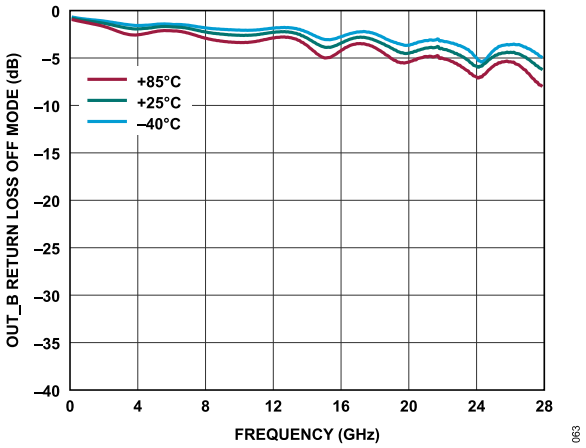

Figure 65. OUT_B Return Loss Off Mode vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

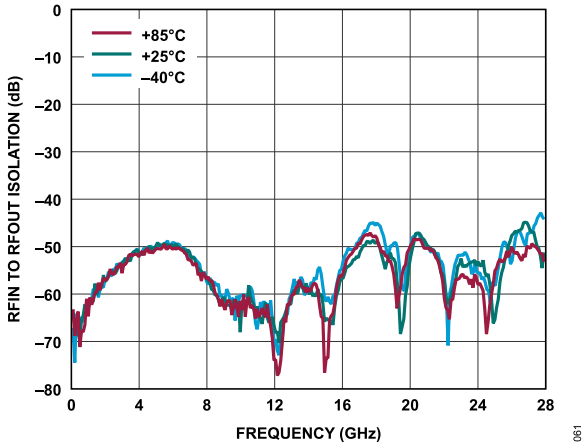

Figure 63. RFIN to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

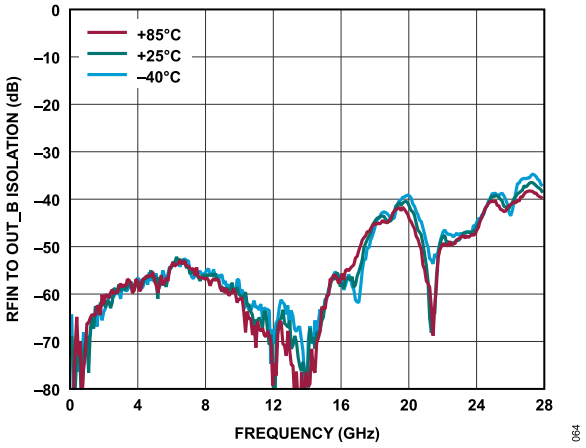

Figure 66. RFIN to OUT_B Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

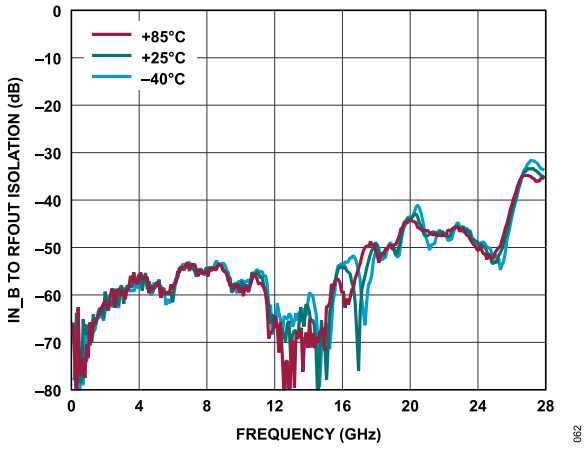

Figure 64. IN_B to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass A

TYPICAL PERFORMANCE CHARACTERISTICS

EXTERNAL BYPASS B MODE

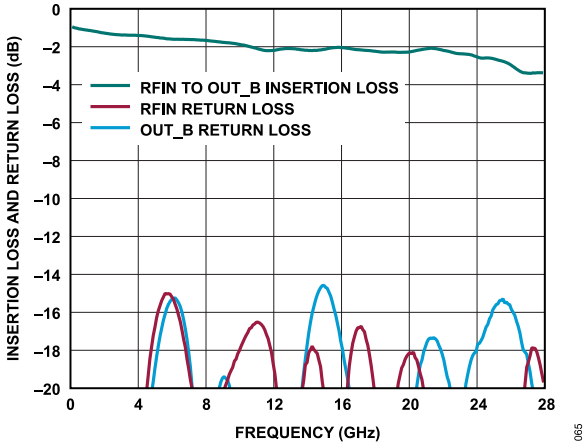

Figure 67. Insertion Loss and Return Loss vs. Frequency, 100 MHz to 28 GHz, Mode = External Bypass B

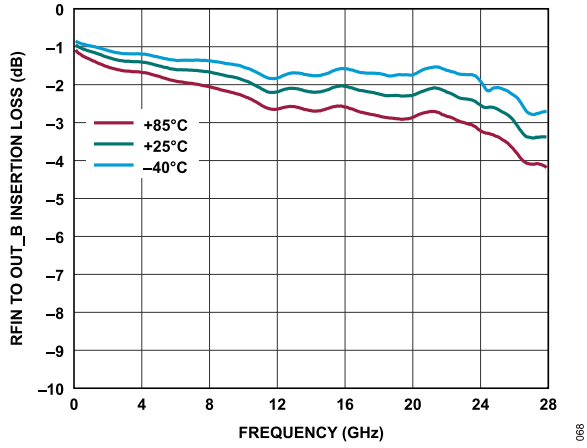

Figure 70. RFIN to OUT_B Insertion Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

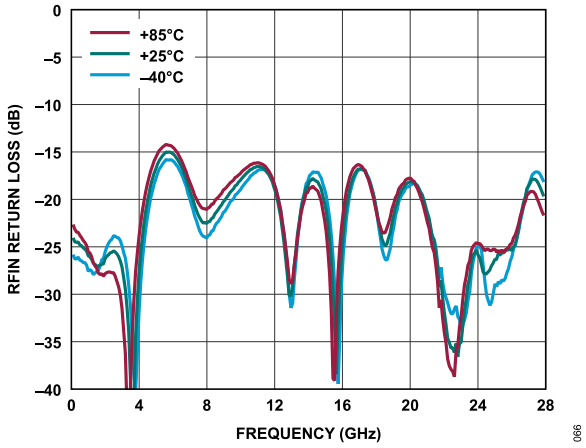

Figure 68. RFIN Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

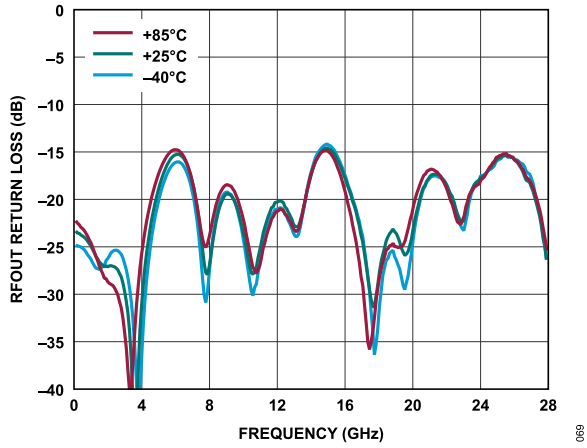

Figure 71. RFOUT Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

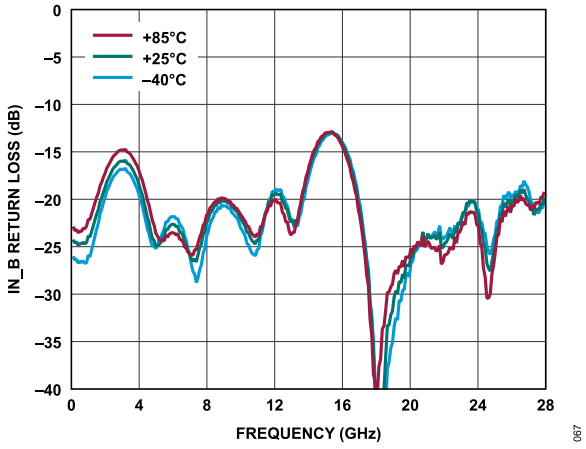

Figure 69. IN_B Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

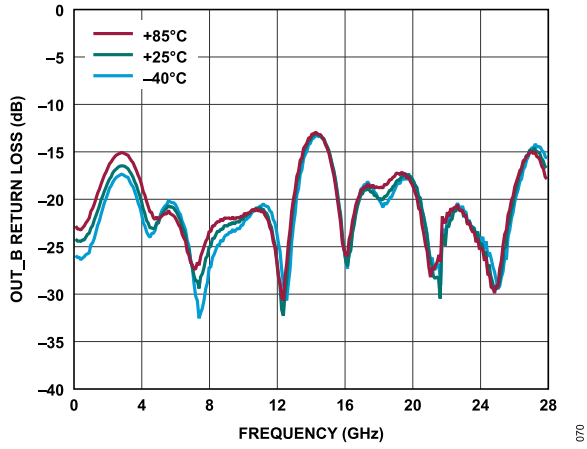

Figure 72. OUT_B Return Loss vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

TYPICAL PERFORMANCE CHARACTERISTICS

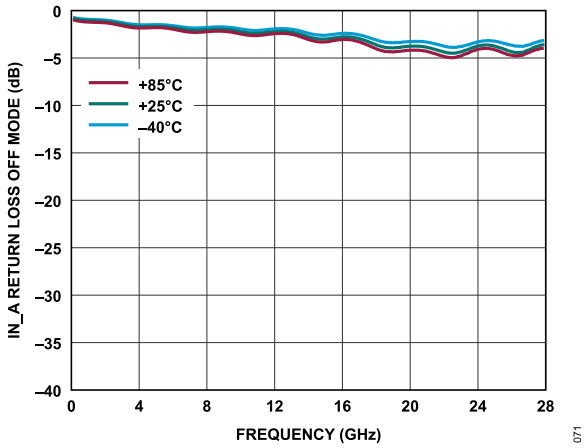

Figure 73. IN_A Return Loss Off Mode vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

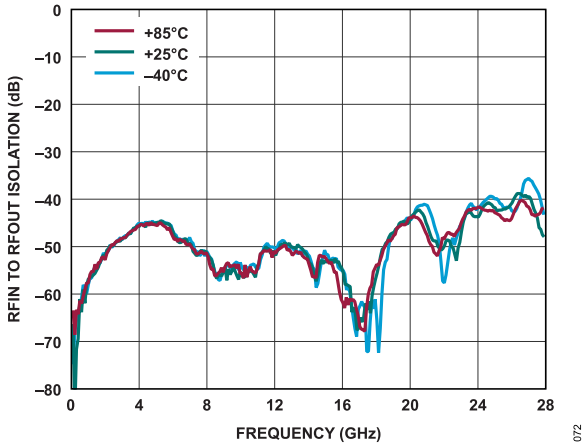

Figure 74. RFIN to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

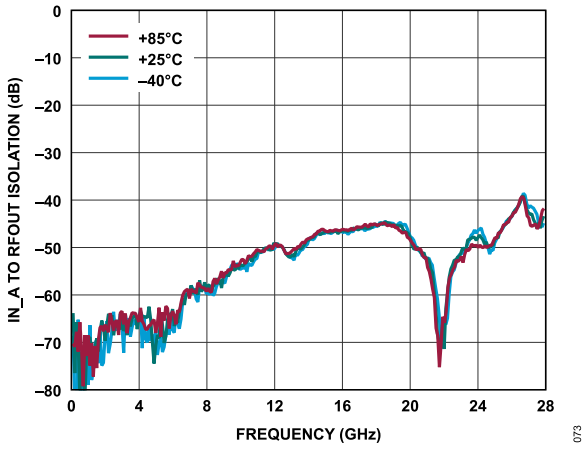

Figure 75. IN_A to RFOUT Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

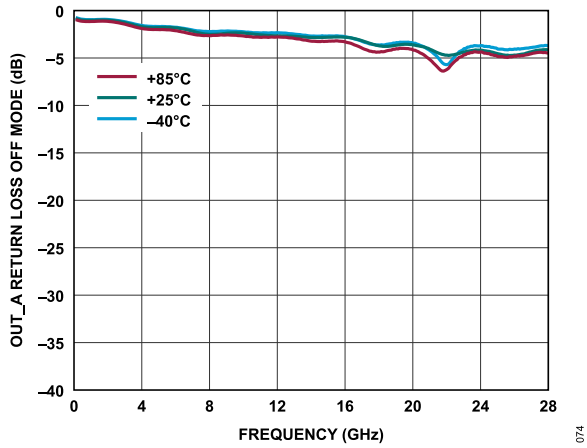

Figure 76. OUT_A Return Loss Off Mode vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

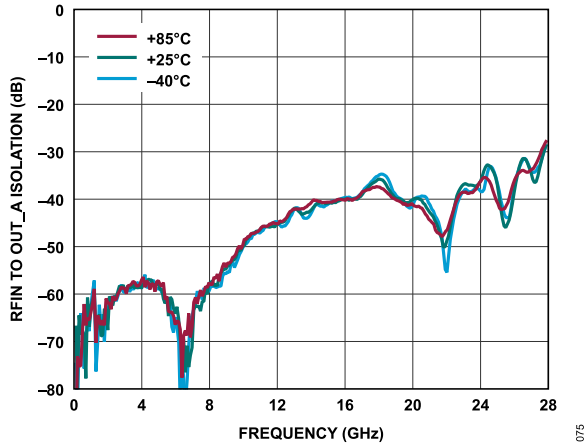

Figure 77. RFIN to OUT_A Isolation vs. Frequency Over Temperature, 100 MHz to 28 GHz, Mode = External Bypass B

THEORY OF OPERATION

The ADL8112 integrates an amplifier with two switching networks located at the RF input and output. The amplifier, which is internally AC-coupled on its input and output, uses a gallium arsenide (GaAs) LNA die. The switching network employs robust silicon-on-insulator (SOI) technology for fast switching and a short settling time. This integrated solution has four different signal path modes available: an internal amplifier, an internal bypass, External Bypass A, and External Bypass B. Signal path modes are controlled through the VA and VB digital pins. The internal amplifier is biased up by applying 8.5 V to VDD1 and by connecting a bias resistor between VDD1 and the RBIAS pin. The reflective switch network is powered by applying +3.3 V and −3.3 V to VDD2 and VSS2, respectively. DC bias to the switches is independent of the LNA. Turning off the bias to VDD1 that controls the LNA, provides better isolation between RF ports.

SIGNAL PATH MODES FOR DIGITAL CONTROL INPUTS

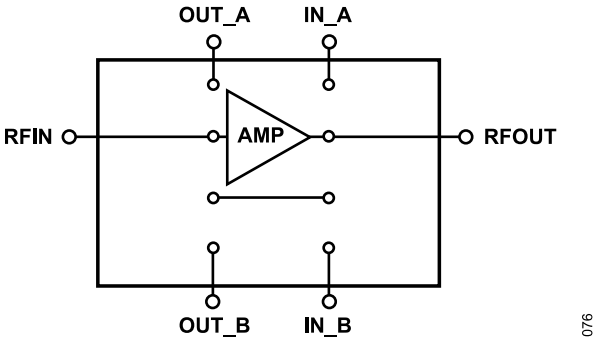

Figure 78. Internal Amplifier Mode, VA = 0 V and VB = 0 V

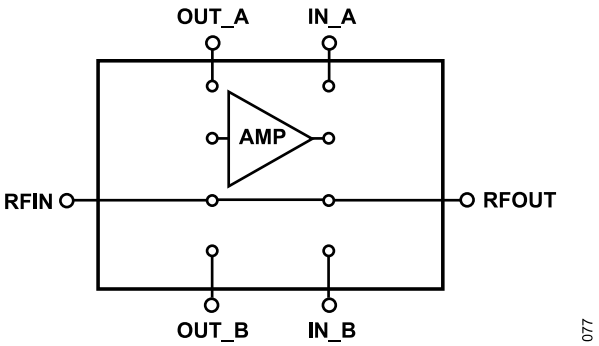

Figure 79. Internal Bypass Mode, VA = 3.3 V and VB = 3.3 V

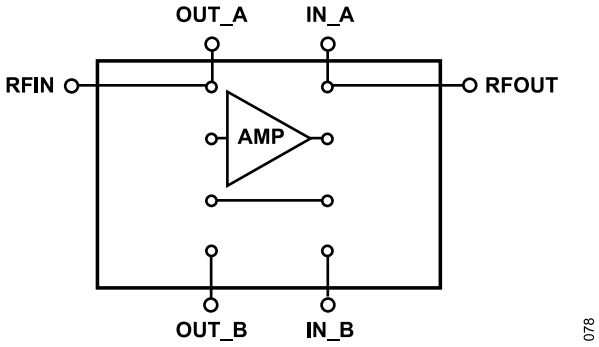

Figure 80. External Bypass A Mode, VA = 0 V and VB = 3.3 V

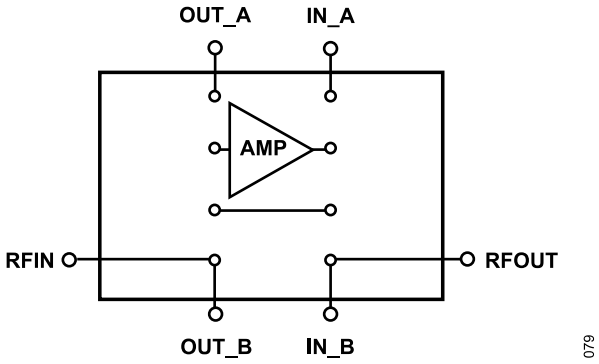

Figure 81. External Bypass B Mode, VA = 3.3 V and VB = 0 V

Table 12. Truth Table

	Digital Control		
Mode Name	**VA**	**VB**	**Signal Path Mode**
Internal Amplifier	Low	Low	RFIN to RFOUT through the amplifier path
Internal Bypass	High	High	RFIN to RFOUT through the bypass path
External Bypass A	Low	High	RFIN to OUT_A, IN_A to RFOUT
External Bypass B	High	Low	RFIN to OUT_B, IN_B to RFOUT

APPLICATIONS INFORMATION

The basic connections for operating the ADL8112 are shown in Figure 83. No additional external power supply decoupling capacitors are required. An 8.5 V DC bias is supplied to the amplifier via the VDD1 pin. The bias current of the amplifier is set by a resistor connected between the RBIAS pin and VDD1. Table 13 depicts the I_{DQ} vs. various R_{BIAS} values for the V_{DD1} voltage of 8.5 V. Do not leave the RBIAS pin open.

Table 13. Recommended Bias Resistor Values at V_{DD1} = 8.5 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
537	100	91.4	8.6
750	90	83	7
945	80	74	6
1278	70	65.2	4.8
1783	60	56.3	3.7

Power for the two SP4T switches comes from the +3.3 V and −3.3 V applied to the VDD2 and VSS2 pins, respectively.

VA and VB are digital inputs that set the operating modes shown in Table 12. The high logic state is between 1.2 V and 3.3 V and the low logic state is 0.8 V to 0 V.

Figure 82 shows the time domain response at RFOUT to the switching voltages on VA and VB when RFIN is driven by a steady level of approximately 2.5 dBm at 250 MHz.

Both of the external bypass connection paths (External Bypass A and External Bypass B) are left open. When VA and VB are low, the ADL8112 is in internal amplifier mode. With VA and VB high, the device switches to internal bypass mode, and the output drops correspondingly. When VA and VB are low or high, the device switches to either External Bypass A or External Bypass B. Because these two paths are left open in this case, no signal appears at the output for both cases.

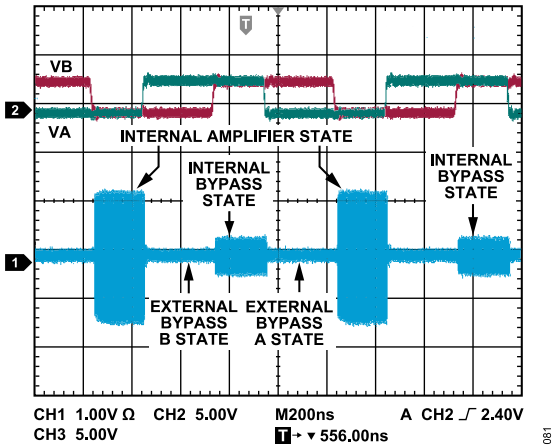

Figure 82. Time Domain Response of RFOUT to Switching of VA and VB Voltages with a Continuous 2.5 dBm RF Input

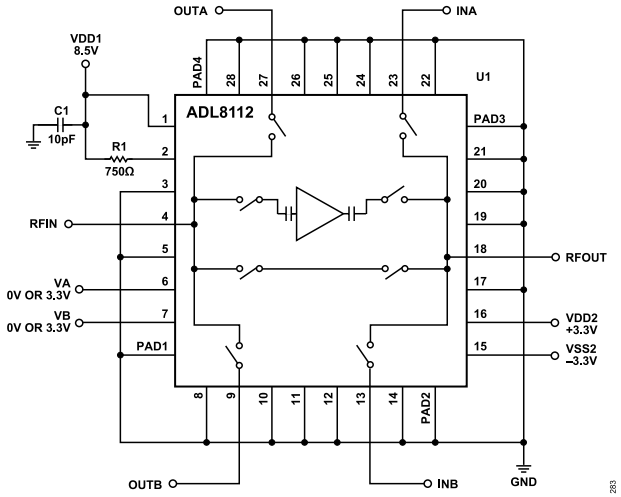

Figure 83. Basic Connections and Evaluation Board Schematic

APPLICATIONS INFORMATION

RECOMMENDED TURN ON/OFF SEQUENCING

Turn On

The recommended bias sequence during power-up is as follows:

1. Set VDD2 = 3.3 V.
2. Set VSS2 = −3.3 V.
3. Set VDD1 = 8.5 V.
4. Apply the RF signal.

Turn Off

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Set VDD1 = 0 V.
3. Set VSS2 = 0 V.
4. Set VDD2 = 0 V.

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 84 shows a recommended power management circuit that uses the MAX1697 inverting charge pump, the MAX17651 linear regulator, and the LT3042 linear regulator. The LT3042 linear regulator is used to step down the 12 V input voltage to a low noise 8.5 V output to VDD1 for the ADL8112.

The output voltage for the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$$R4 = (OUT/100\ \mu A) \quad (1)$$

The PGFB resistors are chosen to trigger the power-good (PG) signal when the output is under 95% of the target voltage of 8.5 V. The OUT pin of the LT3042 has a 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more (5%). Therefore, putting 5% between the OUT pin and the PGFB works well. In addition, the PG open collector is pulled up to the 8.5 V output to produce a convenient 0 V to 8.5 V voltage range.

The MAX17651 linear regulator is used to provide a 3.3 V input voltage to the MAX1697 inverting charge pump and a 3.3 V output voltage to the VSS2 for the ADL8112. The switching frequency for the MAX1697 is set to 250 kHz by the 1 µF capacitor, which sets the minimum output resistance to 12 Ω. The MAX1697 data sheet provides capacitor selector tables that can be used to select other switching frequencies ranging from 12 kHz to 250 kHz.

The output voltage for the MAX17651 is set by the R1 and R2 resistors connected to the OUT and FB pins, according to the following equation:

$$R1 = R2 \times (((IN/OUT) - 1))$$

APPLICATIONS INFORMATION

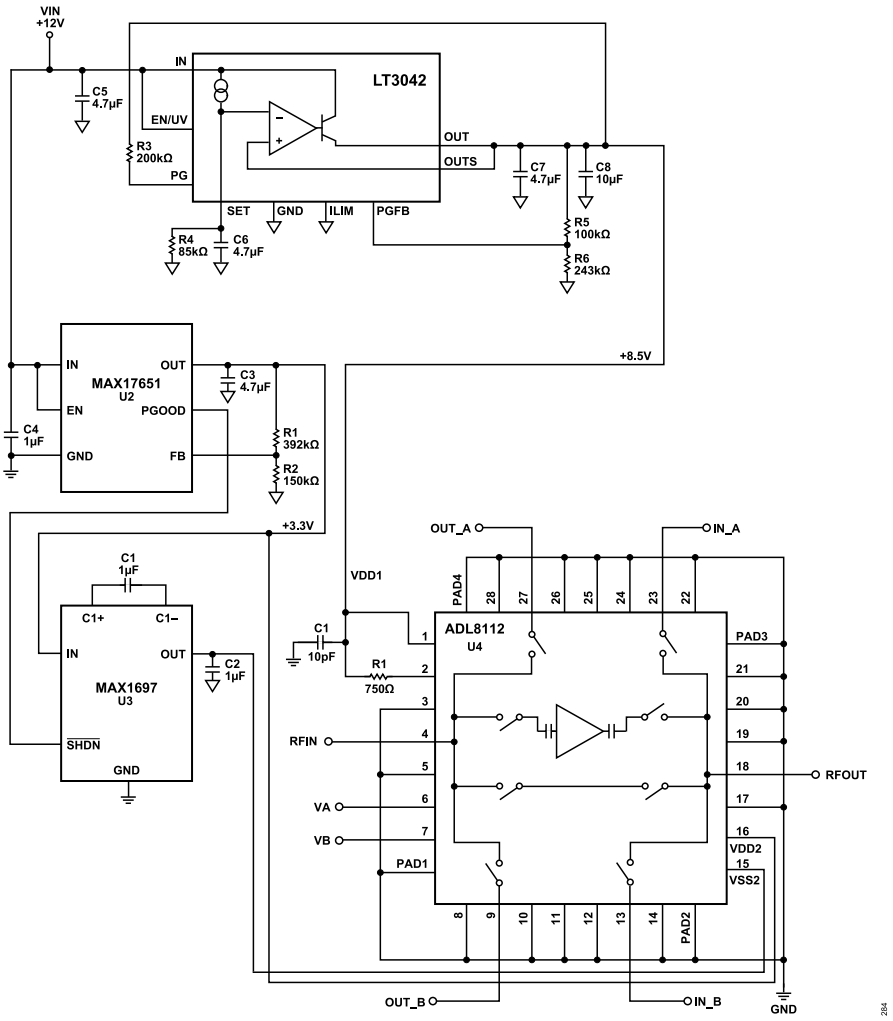

Figure 84. Power Management Circuit Schematic

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CC-28-4	LGA	28-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8112ACCZ	-40°C to +85°C	28-Terminal Land Grid Array [LGA]	Reel, 500	CC-28-4
ADL8112ACCZ-R7	-40°C to +85°C	28-Terminal Land Grid Array [LGA]	Reel, 500	CC-28-4

[1] Z = RoHS Compliant Part.

Updated: August 09, 2023

EVALUATION BOARDS

Table 14. Evaluation Boards

Model[1]	Package Description
ADL8112-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.