MAX25512B

I²C-Controlled 4-Channel Low-Voltage 120mA LED Backlight Driver with Integrated Boost Converter

General Description

The MAX25512B is a 4-channel white LED backlight driver with an integrated current-mode boost converter that operates over a switching frequency range of 400kHz to 2.2MHz and incorporates spread spectrum. Phase-shifting of the output channels is included as an option to further reduce electromagnetic interference (EMI).

The device provides up to 120mA per channel and includes a control output for an external nMOS series switch. It is capable of operating down to 3V after startup.

The device is hybrid-dimming-capable and provides a brightness calibration feature through a dedicated DAC. It can benefit from these two functions simultaneously.

The MAX25512B has an I²C interface to enable flexibility of control and detailed diagnostics. The MAX25512B is available in a compact TQFN package and operates over the -40°C to +125°C temperature range.

Applications

- Automotive Instrument Clusters
- Automotive Central Information Displays
- Automotive Head-Up Displays

Benefits and Features

- Operates down to 3V on Battery Input after Startup
  - Wide Boost Duty Cycle to Support Low Input Voltage
- Boost or SEPIC Current-Mode DC-DC Controller
  - 400kHz to 2.2MHz Operating Frequency Range
  - Spread Spectrum Available
  - Ability to Synchronize to an External Clock
- LED Current Sinks
  - Up to 120mA Output Current per String with Fine-Adjust DAC for brightness calibration
  - Low OUT_ Regulation Voltage for Best Efficiency
  - Optional Phase-Shifting of Outputs
- I²C Control for Enhanced Flexibility
- 16667:1 Dimming Ratio at 200Hz
- NTC Input for LED Current Foldback at High Temperature
- Hybrid Dimming Capable
- Built-in Programmable Automatic Fading Functionality
- Detailed Diagnostic Using I²C and FLTB Output
  - Shorted or Open LEDs
  - Continuous Short-to-GND Monitoring
  - Thermal Shutdown
  - Output Undervoltage
- Compact, 4mm x 4mm TQFN Package
- AEC-Q100 Grade 1

***Ordering Information** appears at end of data sheet.*

19-101860; Rev 2; 6/24

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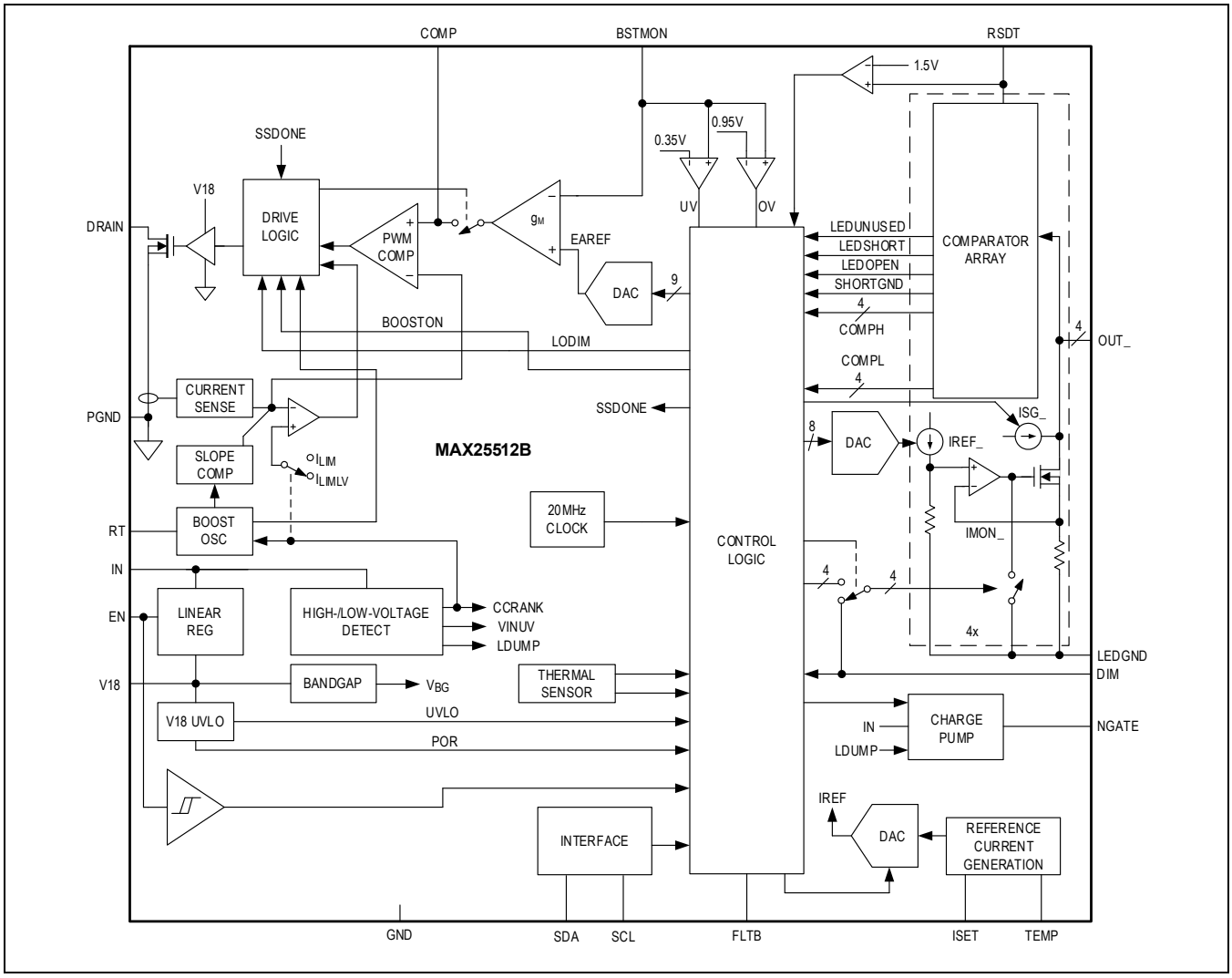
Simplified Block Diagram



Absolute Maximum Ratings

IN, EN to GND ..... -0.3V to +40V
NGATE to IN ..... +6V
NGATE to GND ..... -0.3V to +42V
OUT_ to LEDGND ..... -0.3V to +40V
DRAIN to PGND ..... -0.3V to +40V
V18, BSTMON to GND ..... -0.3V to +2.2V
SDA, SCL to GND ..... -0.3V to +6V
FLTB, DIM to GND ..... -0.3V to +6V
RT, COMP, ISET, TEMP, RSDT to GND ....-0.3V to V18+0.3V
PGND to GND .....-0.3V to +0.3V
LEDGND to GND .....-0.3V to +0.3V
DRAIN Current .....±4.5A
OUT_ Continuous Current ..... ±150mA
Continuous Power Dissipation (multilayer board) (T_A = +70°C, derate 24.2mW/°C above +70°C) 1938mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... -40°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T2444+4C
Outline Number	21-0139
Land Pattern Number	90-0022
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{IN} = V_{EN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Operating Voltage Range	V_{IN}		4.5		36	V
Operating Voltage Range after Startup		Maximum duration 100ms	3		36	V
Supply Current	I_{IN}	No switching		1.3	1.8	mA
Shutdown Supply Current		V_{EN} = 0V, +25°C		2.4	5	µA

(V_{IN} = V_{EN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Undervoltage Lockout, Rising	V_{INUVR}		4.15	4.29	4.4	V
IN Undervoltage Lockout, Falling	V_{INUVF}		2.77	2.9	2.95	V
Threshold for Low-Voltage Operation Mode, Falling	V_{LVF}		5.3	5.5	5.7	V
Threshold for Low-Voltage Operation Mode, Rising	V_{LVR}		5.55	5.72	5.85	V
V18 REGULATOR						
V18 Voltage			1.75	1.8	1.85	V
V18 Undervoltage Lockout, Rising	$UVLOV18_R$		1.6	1.65	1.69	V
V18 Undervoltage Lockout, Falling	$UVLOV18_F$		1.54	1.575	1.61	V
V18 Short-Circuit Current Limit	I_{SCV18}	V18 shorted to GND		50		mA
NGATE OUTPUT						
NGATE Source Current			30	50		µA
NGATE Sink Current			0.5	1		mA
NGATE Output Voltage		Above V_{IN}, 3V < V_{IN} < 33V, I_{NGATE} = 0µA	4.3	5.25	6.3	V
		Above V_{IN}, 3V < V_{IN} < 33V, I_{NGATE} = 10µA	3.8	4.6	6	
NGATE Output Voltage at High Input Voltage		Above V_{IN}, V_{IN} > 35.5V, I_{NGATE} = 1µA	-0.05		0	V
V_{IN} OV Comparator Threshold for NGATE, Rising	V_{LDUMP_TH}		33		35.5	V
V_{IN} OV Comparator Hysteresis for NGATE				0.7		V
NGATE Start Delay		Delay between NGATE charge-pump turning on and the boost converter starting		2	2.2	ms
RT OSCILLATOR						
Switching Frequency Range	f_{SW}	Frequency dithering disabled	400		2200	kHz
Oscillator Frequency Accuracy		f_{SW} = 400kHz to 2200kHz, frequency dithering disabled	-10		+10	%
Boost Converter Maximum Duty Cycle, High Frequency		f_{SW} = 1.3MHz to 2.2MHz	86	88	92	%
Boost Converter Maximum Duty Cycle, Low Frequency		f_{SW} = 400kHz to 1.3MHz	94	95	98	%
Boost Minimum On-Time				60		ns
Frequency Dither, High Setting		SSL = 0		±6		%

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Dither, Low Setting		SSL = 1			±4		%
RT Output Voltage	V_{RT}	R_{RT} = 65kΩ or R_{RT} = 10kΩ			0.9		V
RT Out-of-Range Lower Limit					5	6.4	kΩ
RT Out-of-Range Upper Limit				90	111		kΩ
Sync Falling Threshold				0.77		0.84	V
Sync Frequency Duty-Cycle Range					50		%
Sync Frequency Range				400		2200	kHz
MOSFET							
DRAIN MOSFET $R_{DS(ON)}$		I_{DRAIN} = 1A			0.075	0.125	Ω
DRAIN Leakage Current		V_{DRAIN} = 36V, T_A = +25°C			0.03	1	µA
CURRENT-SENSE COMPARATOR							
Current-Limit Threshold at Low Input Voltage	I_{LIMLV}			8.1	9.1	9.8	A
Current-Limit Threshold	I_{LIM}			4.3	5.3	6	A
ERROR AMPLIFIER							
OUT_ Regulation High Threshold	V_{OUTH}	$V_{OUT_}$ falling		0.825	0.85	0.875	V
OUT_ Regulation Low Threshold	V_{OUTL}	$V_{OUT_}$ rising		0.55	0.58	0.61	V
Transconductance				410	630	890	µS
COMP Sink Current		V_{COMP} = 1V		270	380	500	µA
COMP Source Current		V_{COMP} = 1V		270	380	500	µA
LED CURRENT SINKS							
ISET Output Voltage	V_{ISET}				0.75		V
OUT_ Output Current		R_{ISET} = 12.5kΩ	120mA setting	116	120	124	mA
		R_{ISET} = 15kΩ	100mA setting	97	100	103	
		R_{ISET} = 30kΩ	50mA setting	48	50	52	
Channel-to-Channel Matching		$I_{OUT_}$ = 120mA		-2		+2.2	%
		$I_{OUT_}$ = 50mA		-3.25		+3.25	
Total OUT_ Leakage Current	$I_{OUTLEAK}$	$V_{OUT_}$ = 36V, DIM = 0V, all OUT_ are shorted together			0.01	4	µA
OUT_ Minimum Pulse Width					300		ns
OUT_ Minimum Negative Pulse Width					90		ns
OUT_ Current Rise Time		10% to 90% $I_{OUT_}$ (Note 2)			150		ns
OUT_ Current Fall Time		90% to 10% $I_{OUT_}$ (Note 2)			30		ns
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION							
BSTMON Overvoltage Trip Threshold	V_{BST_OV}	V_{BSTMON} rising		0.93	0.95	0.97	V

(V_{IN} = V_{EN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BSTMON Hysteresis				50		mV
BSTMON Input Bias Current		0 < V_{BSTMON} < 1.3V	-1		+1	µA
BSTMON Undervoltage Detection Threshold, Rising	$V_{BST_UVR,N}$	Normal soft-start	384	400	416	mV
	$V_{BST_UVR,F}$	Fast soft-start	720	750	780	
BSTMON Undervoltage Detection Threshold, Falling	V_{BST_UVF}	BSTMON falling, NGATE latched off	0.335	0.35	0.363	V
Boost Undervoltage Blanking Time, Standard Soft-Start		After EN pin taken high	49	53.25	57.5	ms
Boost Undervoltage Blanking Time, Fast Soft-Start		After EN pin taken high	26.18	28.46	30.74	ms
BSTMON Undervoltage Detection Delay	$t_{BST_UV_DEL}$	BSTMON falling	4	10	18	µs
LED FAULT DETECTION						
Maximum LED Short-Detection Threshold		V_{RSDT} = 833mV rising	9.7	10	10.3	V
LED Short-Detection Threshold		V_{RSDT} = 0.667V	7.5	8	8.5	V
Minimum LED Short-Detection Threshold		V_{RSDT} = 200mV rising	2.25	2.4	2.5	V
LED Short Disable Threshold		All active OUT_S rising	1.9	2	2.15	V
RSDT Pin Voltage Range			0.2		1	V
RSDT Disable/Switch-to-I²C Threshold			1.45	1.5	1.55	V
RSDT Pin Bias Current			-5		+5	µA
Short-Detection Comparator Delay	t_{SD_DEL}			6.8		µs
OUT_ Check LED Source Current	I_{CHKLED}		50	60	70	µA
OUT_ Short-to-GND Detection Falling Threshold	V_{TH_SGND}		230	250	270	mV
OUT_ Unused Detection Threshold	V_{TH_UNUSED}		0.775	0.85	0.925	V
OUT_ Open-LED Detection Threshold	V_{OOL}	During operation	230	250	270	mV
LOGIC INPUT AND OUTPUTS						
DIM, SDA, SCL Input Logic-High			1.6			V
DIM, SDA, SCL Input Logic-Low					0.4	V
DIM, SCL Input Leakage Current			-1		+1	µA
EN Input Logic-High			0.9			V
EN Input Logic-Low					0.6	V

(V_{IN} = V_{EN} = 12V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Input Current		V_{EN} = 5V		0.01	1	µA
Minimum EN Pulse Width for Device Enable	t_{EN_ON}		5			ms
EN Turn-Off Delay	t_{EN_OFF}	Time between EN going low and complete device shutdown	11.5	12.8	14.1	ms
DIM Frequency Range			90		50000	Hz
DIM Sampling Frequency				20		MHz
FLTB Output Low Voltage		Sinking 3mA			0.4	V
FLTB Output Leakage Current		V_{FLTB} = 5.5V	-1		+1	µA
SDA Output Leakage Current			-1		+1	µA
TEMP PIN						
TEMP Voltage			180	200	220	mV
TEMP to ISET Gain		V_{TEMP} < 250mV	13.7	14.3	14.9	V/mA
TEMP Disable Threshold				0.25		V
TEMP Leakage Current				0.005	1	µA
ISET Voltage Threshold for LED Current Disable				150		mV
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SHDN}			160		°C
Thermal-Shutdown Hysteresis				17		°C
Thermal Warning Threshold	T_{WARN}	Temperature rising		130		°C
I²C INTERFACE						
Clock Frequency	f_{SCL}				0.4	MHz
Hold Time (Repeated) START	$t_{HD:STA}$		600			ns
SCL Low Time	t_{LOW}		1300			ns
SCL High Time	t_{HIGH}		600			ns
Setup Time (Repeated) START	$t_{SU:STA}$		600			ns
Data Hold Time	$t_{HD:DAT}$		0			ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		600			ns
Spike Suppression				50		ns

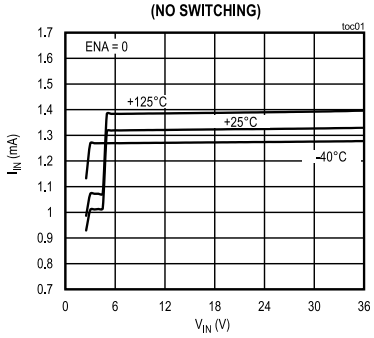
Note 1: Limits are 100% tested at T_A = +25°C, T_A = +125°C, and T_A = -40°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design.

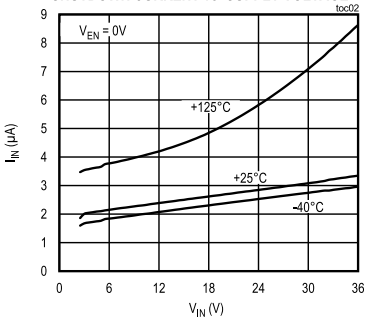
Typical Operating Characteristics

(V_{IN} = V_{EN} = 12V, 4 x 9 LED load at 100mA, f_{SW} = 2.2MHz, T_A = +25°C unless otherwise noted.)

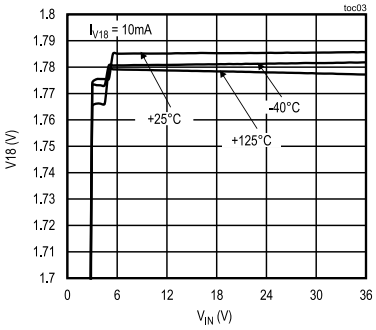
SUPPLY CURRENT vs. SUPPLY VOLTAGE (NO SWITCHING)



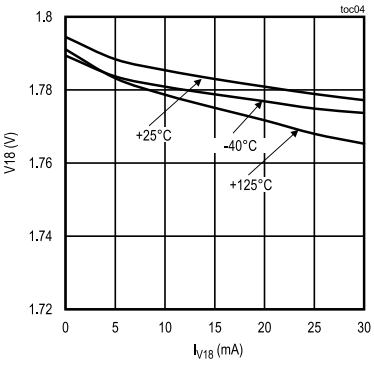
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



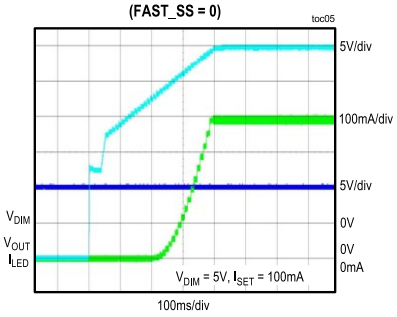
V18 LINE REGULATION



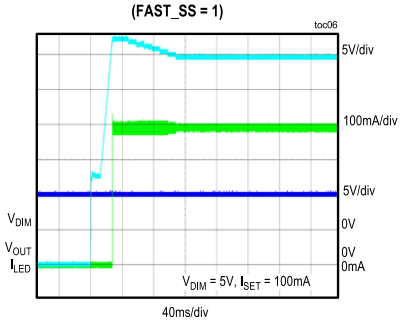
V18 LOAD REGULATION



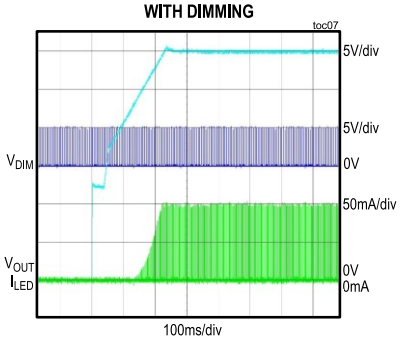
STARTUP WAVEFORM (FAST_SS = 0)



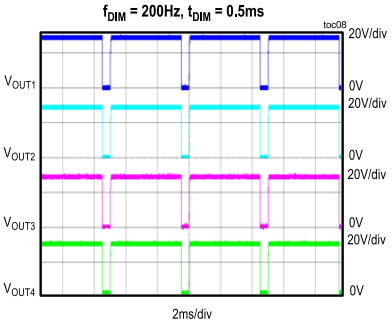
STARTUP WAVEFORM (FAST_SS = 1)



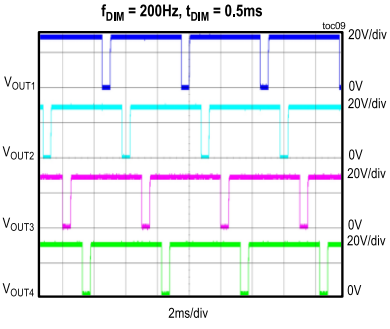
SLOW STARTUP WAVEFORM WITH DIMMING



DIMMING WAVEFORM (PSEN = 0)
f_{DIM} = 200Hz, t_{DIM} = 0.5ms

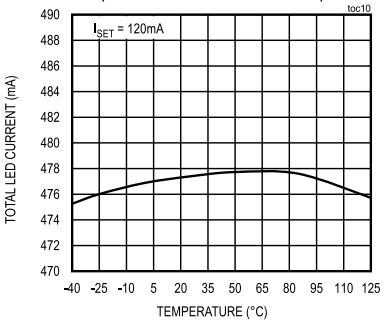


DIMMING WAVEFORM (PSEN = 1)
f_{DIM} = 200Hz, t_{DIM} = 0.5ms

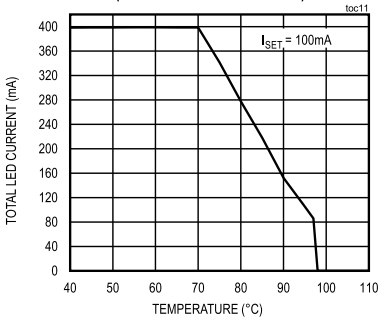


(V_{IN} = V_{EN} = 12V, 4 x 9 LED load at 100mA, f_{SW} = 2.2MHz, T_A = +25°C unless otherwise noted.)

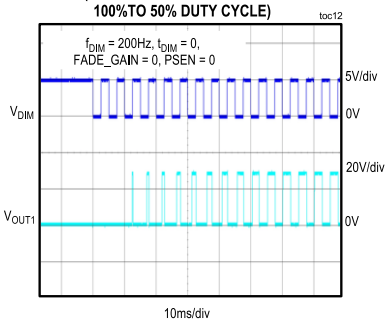
TOTAL LED CURRENT vs. TEMPERATURE (2.2MHz SWITCHING FREQUENCY)



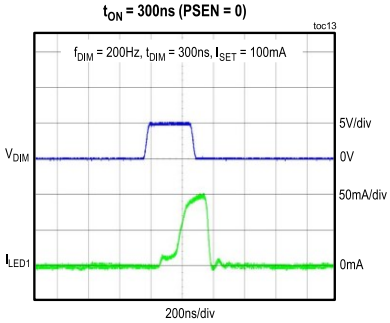
LED CURRENT vs. TEMPERATURE (TEMPERATURE FOLDBACK)



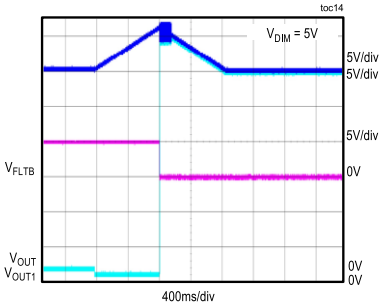
FADING WAVEFORM (DIMMING TRANSITION FROM 100%TO 50% DUTY CYCLE)



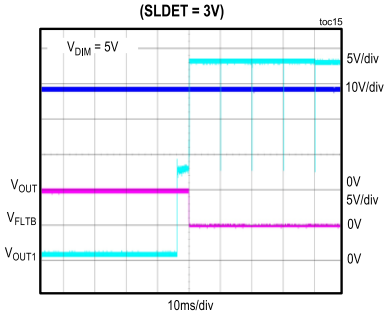
LED CURRENT WITH DIMMING t_{ON} = 300ns (PSEN = 0)



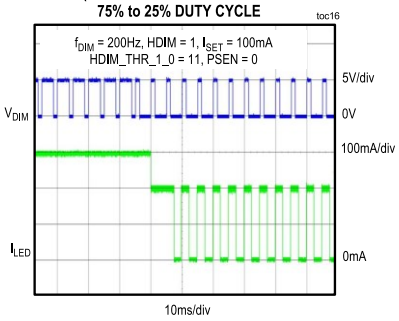
LED OPEN FAULT ON OUT1



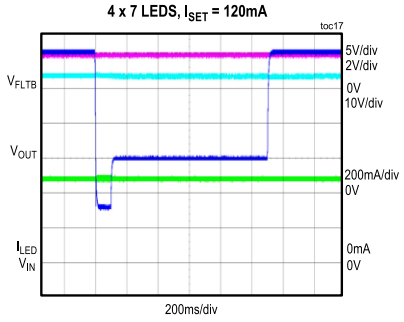
LED SHORT FAULT ON OUT1 (SLDET = 3V)



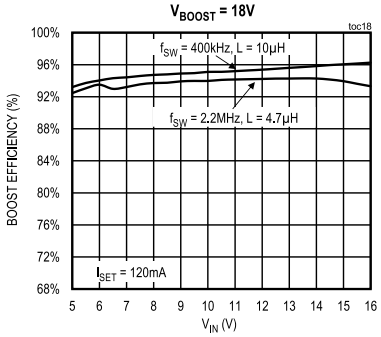
HYBRID DIMMING WAVEFORM (DIMMING TRANSITION FROM 75% to 25% DUTY CYCLE



COLD CRANK TO V_{IN} = 3V 4 x 7 LEDS, I_{SET} = 120mA

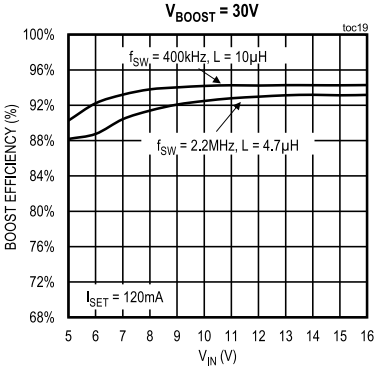


EFFICIENCY vs. INPUT VOLTAGE V_{BOOST} = 18V

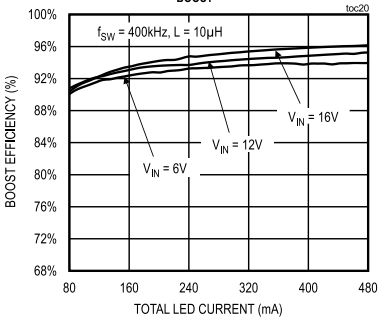


(V_{IN} = V_{EN} = 12V, 4 x 9 LED load at 100mA, f_{SW} = 2.2MHz, T_A = +25°C unless otherwise noted.)

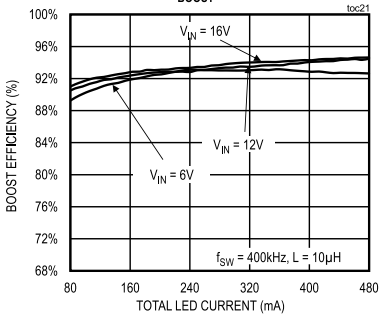
EFFICIENCY vs. INPUT VOLTAGE
V_{BOOST} = 30V



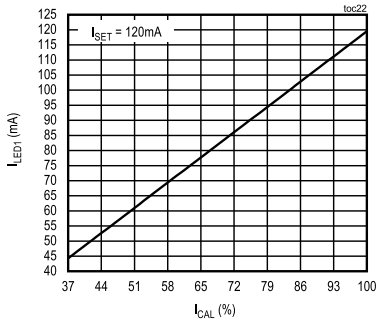
EFFICIENCY vs. LED CURRENT
V_{BOOST} = 18V



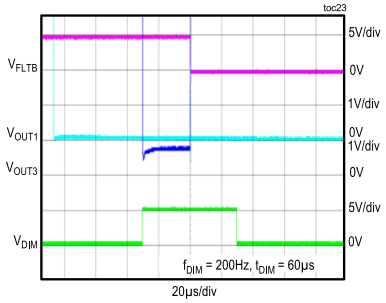
EFFICIENCY vs. LED CURRENT
V_{BOOST} = 30V



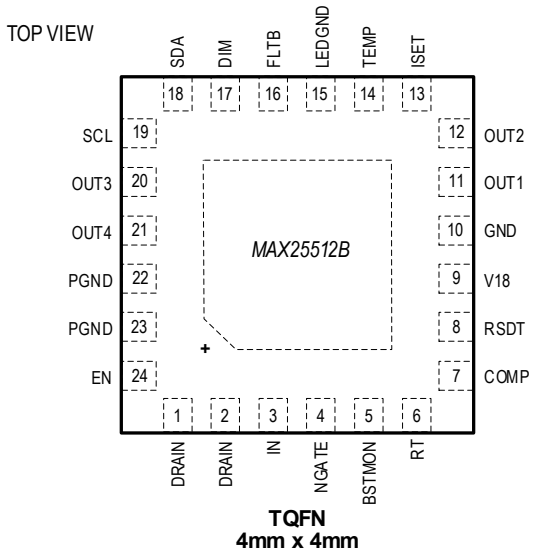
I_{LED1} vs. I_{CAL} SETTING



SHORT-TO-GROUND FAULT
ON OUT1 DURING OPERATION



Pin Configurations

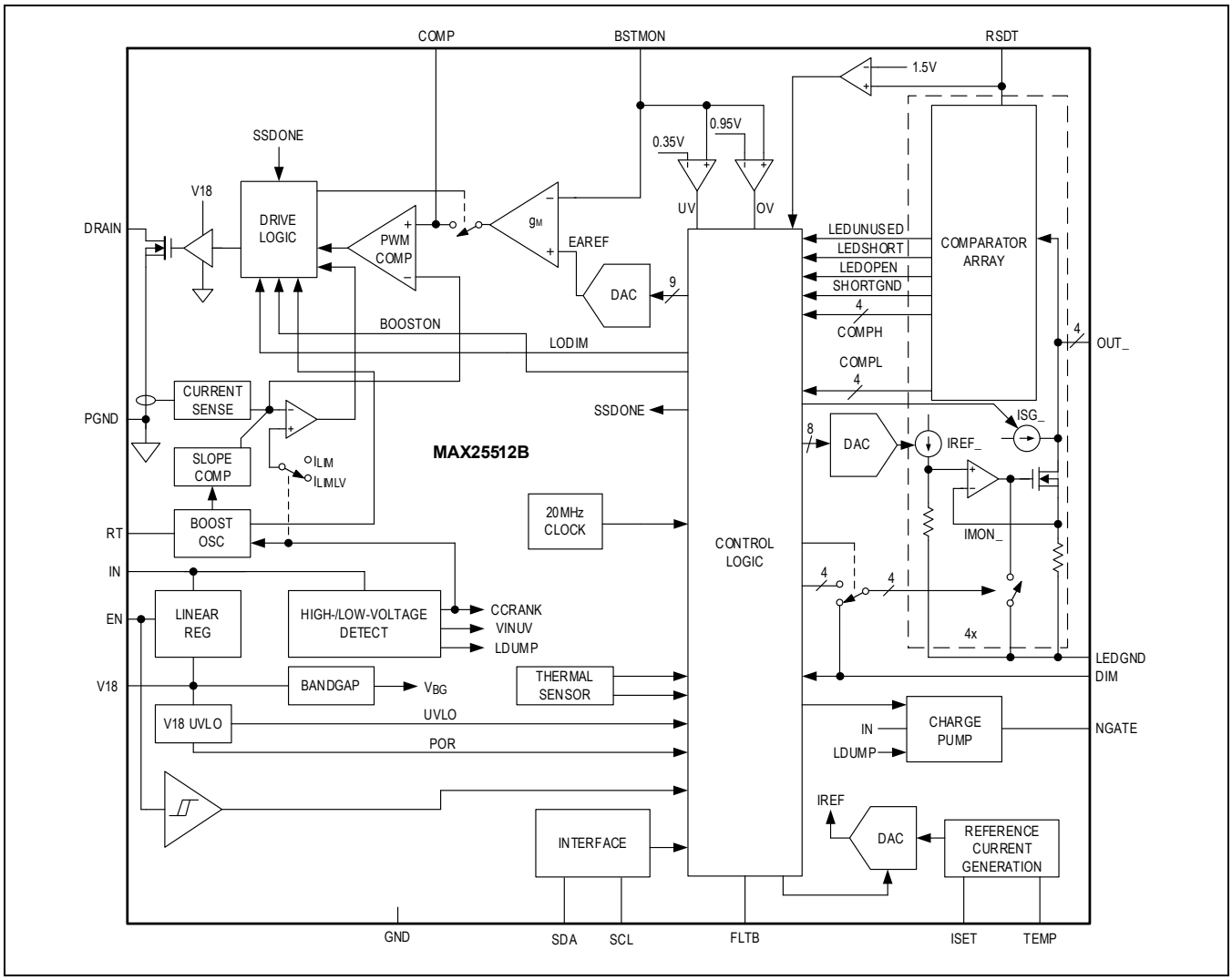


Pin Descriptions

PIN	NAME	FUNCTION
1, 2	DRAIN	Drain Connection of Internal Switching Power nMOSFET. Connect to the external inductor and rectifier diode.
3	IN	Input Voltage. Connect to protected battery. Bypass IN with a minimum of 2.2µF in parallel with 0.1µF placed close to the pin.
4	NGATE	Gate Connection for External Series nMOSFET. Driven by the internal charge pump.
5	BSTMON	Boost Voltage Monitoring Input. Connect a resistor-divider from the boost converter output to GND with its midpoint connected to the BSTMON pin in order to set the maximum boost output voltage.
6	RT	Oscillator Timing Resistor Connection. Connect a timing resistor (RT) to GND to program the switching frequency. Apply an AC-coupled external clock at RT to synchronize the switching frequency with an external clock.
7	COMP	Switching Converter Compensation Input. Connect the compensation network from COMP to GND for current-mode control (see the *Feedback Compensation* section).
8	RSDT	LED Short-Detection Threshold-Adjust Input. Connect a resistor-divider from V18 to RSDT and GND to program the LED short-detection threshold. Connect RSDT directly to V18 to disable LED short detection or when programming the threshold using the I²C interface.
9	V18	Output of Internal 1.8V Regulator. Connect 1µF and 0.1µF capacitors from V18 to GND with the 0.1µF capacitor placed closest to the pin.
10	GND	Signal GND. GND is the current return path connection for the low-noise analog signals. Connect GND, LEDGND, and PGND at a single point.
11	OUT1	LED String Cathode Connection 1. OUT1 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT1. OUT1 sinks up to 120mA.
12	OUT2	LED String Cathode Connection 2. OUT2 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT2. OUT2 sinks up to 120mA. If OUT2 is unused, connect a 10kΩ resistor from OUT2 to LEDGND.
13	ISET	LED Current-Adjust Input. Connect a resistor (R_{ISET}) from I_{SET} to GND to set the current through each LED string (I_{LED}), according to the formula $I_{LED} = 1500/R_{ISET}$. Place the resistor close to the pin to avoid parasitic capacitance.

14	TEMP	Temperature Sensor Input. To implement LED current reduction at high temperatures, connect an NTC temperature sensor to GND with resistors from the NTC to TEMP and to V18. If unused, connect TEMP to V18.
15	LEDGND	LED Ground. LEDGND is the return path connection for the linear current sinks. Connect GND, LEDGND, and PGND at a single point.
16	FLTB	Open-Drain Fault Output. FLTB asserts low when a fault is detected. Connect a pull-up resistor from FLTB to a logic supply of 5V or lower.
17	DIM	Digital PWM Dimming Input. Apply a PWM signal to DIM for LED dimming control. Connect DIM to a logic supply of 5V or lower if dimming control is not used.
18	SDA	Bidirectional I²C Data Pin. Connect a pull-up resistor from this node to the logic supply voltage.
19	SCL	I²C Clock Input Pin. Connect a pull-up resistor from this node to the logic supply voltage.
20	OUT3	LED String Cathode Connection 3. OUT3 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT3. OUT3 sinks up to 120mA. If OUT3 is unused, connect a 10kΩ resistor from OUT3 to LEDGND.
21	OUT4	LED String Cathode Connection 4. OUT4 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT4. OUT4 sinks up to 120mA. If OUT4 is unused, connect a 10kΩ resistor from OUT4 to LEDGND.
22, 23	PGND	Power Ground. PGND is the DRAIN current return path connection. Connect GND, LEDGND, and PGND at a single point.
24	EN	Enable Input. Connect EN to logic-high for normal operation. When EN is taken low, the device is disabled after a delay of t_{EN_OFF}. Do not leave the EN input open.

Functional Diagrams



Detailed Description

The MAX25512B is a 4-channel backlight driver IC with integrated boost converter for automotive displays. The integrated current outputs can each sink up to 120mA LED current. The device accepts a wide 3V to 36V input voltage range. The IC provides load-dump voltage protection up to 40V in automotive applications and incorporates three major blocks: a DC-DC converter with peak current-mode control to implement a boost or SEPIC-type switched-mode power supply, a 4-channel LED driver with up to 120mA constant-current sink capability per channel, and a logic control block.

The internal current-mode switching DC-DC converter supports boost or SEPIC topologies and operates in the 400kHz to 2.2MHz frequency range. Optional spread spectrum helps reduce EMI. An adaptive output-voltage-control scheme minimizes power dissipation in the LED current-sink paths.

The device tracks the external pulse-width-modulation (PWM) dimming input on DIM. The minimum pulse width is 300ns. Phase-shifted dimming of the strings is selectable for lower EMI.

Comprehensive diagnostic and protection features are implemented. The MAX25512B features an I²C interface for enhanced control and diagnostics.

Enable

The internal regulator is enabled when the EN pin is high. To shut down the device, drive EN low. The current consumption reduces to µA levels.

The internal low dropout (LDO) regulator converts the input voltage at IN to a 1.8V output voltage at V18. The LDO regulator supplies current to the internal control circuitry and gate driver.

Undervoltage Lockout

The IC features two undervoltage lockouts (UVLOs) that monitor the input voltage at IN and the output of the internal LDO regulator at V18. The device turns on when EN is taken high, and the boost converter can be enabled if both IN and V18 are higher than their respective UVLO thresholds.

After start-up, the device can operate down to 3V, as described in the *Low-Voltage Operation* section.

High-Voltage Operation

When the input voltage exceeds V_{LDUMP_TH}, the NGATE output follows the IN voltage and the external nMOSFET operates as a source follower. During this time, the power dissipation in the nMOSFET is higher than normal and is approximately $V_t \times I_{LED(TOTAL)}$ where V_t is the threshold voltage of the external nMOSFET.

Low-Voltage Operation

After the boost soft-start is complete, the MAX25512B continues to operate with IN voltages as low as 3V. At very low input voltages, the efficiency of the boost converter reduces, and the input current can reach very high levels as a consequence. When the input voltage falls below V_{LVF}, the boost converter current limit is automatically increased to I_{LIMLV}, and the switching frequency is reduced if it is greater than 1.4MHz. In this mode, if the standard current limit (I_{LIM}) is exceeded on four consecutive cycles, a 100ms timer is started. This returns the current limit to I_{LIM} when it expires. When the input voltage returns above V_{LVR}, operation at the normal switching frequency is resumed.

The external boost converter components must be selected for worst-case operation. An alternative is to reduce the output power at low input voltages.

If the voltage at IN drops below the undervoltage lockout level (V_{INUVF}) at any time, the boost converter is disabled.

Operating Modes

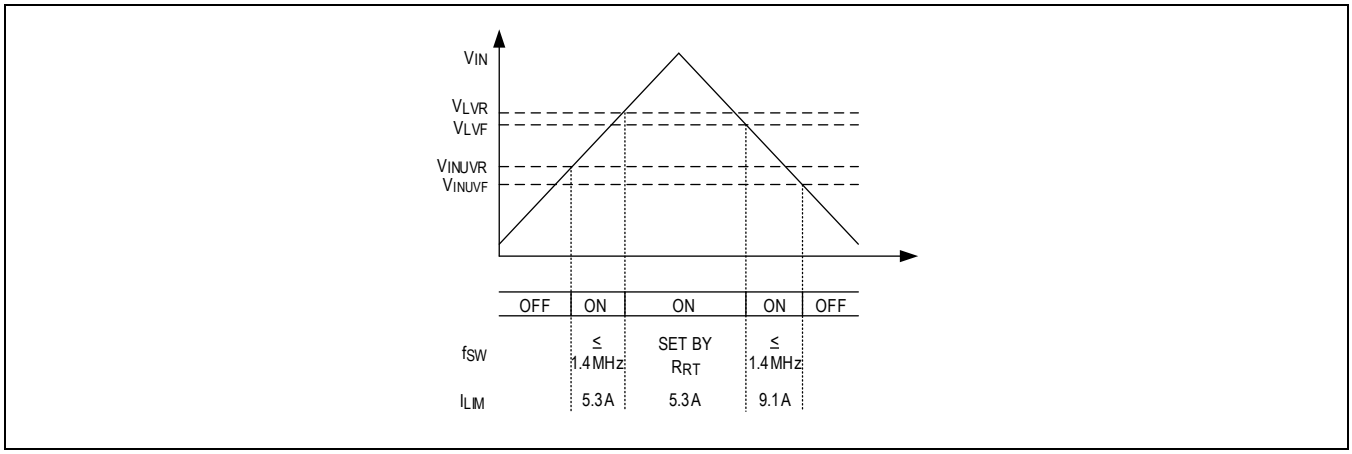


Figure 1. Boost Converter Operating Modes

Disabling Individual Strings

To disable an unused LED string, connect the unused OUT_ to ground through a 10kΩ resistor, or set the corresponding DIS_ bit to 1 in the DISABLE (0x13) register before the ENA bit is set. During startup, the device sources 60µA (typ) current through the OUT_ pins and measures the corresponding voltage. For the string to be properly disabled, the OUT_ voltage should measure between 270mV and 0.775V during this check. 270mV is the maximum threshold for the OUT_ short-to-ground check, and 0.775V is the minimum unused string-detection threshold.

Note: When disabling unused strings, it is necessary to start by disabling the highest numbered current sinks first (e.g., if two strings need to be disabled, disable OUT4 and OUT3. Do not disable any two strings at random). During normal operation, strings can be selectively turned off by changing the corresponding TON_ setting to 0. This is only possible when internal dimming is used, not when using the DIM input pin.

Current-Mode DC-DC Controller

The IC has a constant-frequency, current-mode controller designed to drive the LEDs in a boost or SEPIC configuration. The IC features multiloop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks, to minimize power dissipation.

The internal MOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until it is turned off at the peak current level set by the feedback loop. The peak inductor current is sensed internally, and slope compensation is added.

The IC features leading-edge blanking to suppress the MOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the MOSFET when the total current-sense voltage exceeds the error amplifier's output voltage, which is also the voltage on the COMP pin. This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the IC has two other feedback loops for control. The converter output voltage is sensed through the BSTMON input, which goes to the inverting input of the error amplifier. The other feedback comes from the OUT_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation while still ensuring accurate LED current matching. Each current sink has a window comparator with a low threshold of V_{OUTL} and a high threshold of V_{OUTH}. The outputs of these comparators control an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives a 9-bit DAC that sets the reference to the error amplifier. When dimming is set to 100%, the counter is updated at intervals of 10ms.

9-Bit Digital-to-Analog Converter (DAC)

The error amplifier's reference input is controlled with an 9-bit DAC. The DAC output is ramped up slowly during startup to implement a soft-start function (see the *Startup Sequence* section). During normal operation, the DAC output range is limited to 0.48V to 1V. Because the DAC output is limited to no less than 0.48V during normal operation, the overvoltage threshold for the output should be set to a value less than twice the minimum LED forward voltage. The DAC LSB determines the minimum step in output voltage according to the equation:

$V_{STEP_MIN} = V_{DAC_LSB} \times A_{OVP}$

where:

V_{STEP_MIN} = Minimum output-voltage step

V_{DAC_LSB} = DAC least significant bit size (1.95mV)

A_{OVP} = BSTMON resistor-divider gain (1 + R6/R7)

LED Current Control

The full-scale sink current for the outputs (OUT1–OUT4) is set using the resistor on the ISET pin. Use the following equation to calculate the resistor value:

$$R_{ISET} = \frac{1500}{I_{LED}}$$

where:

I_{LED} is the individual OUT_ current.

If the R_{ISET} value is less than 11.9kΩ, the device may not operate.

When PWM dimming is used, the current in the OUT_ channels switches between zero and the full-scale sink current at the set duty cycle.

Analog Dimming

By using the ADIM register, the OUT_ current set by the resistor on the ISET pin can be reduced in 255 steps in a similar way to when using the ICAL[5:0] setting. Each step represents 0.4% of the ISET current. When ADIM is set to 0xFF, the full-scale current is provided.

When using hybrid dimming, ADIM cannot be used, but current calibration can still be accomplished using ICAL[5:0].

Hybrid Dimming

In hybrid dimming mode, the external LEDs are dimmed by first reducing their current as the dimming duty-cycle decreases from 100% (see *Figure 2*). At the crossover level set by the HDIM_THR_1_0[1:0] bits (50%, 25%, 12.5%, or 0.25%), dimming transitions to PWM dimming where the LED current is chopped. To select hybrid dimming, set the HDIM bit in the IMODE (0x03) register. Select the desired crossover level between analog and PWM dimming using the HDIM_THR_1_0[1:0] bits in the same register. Depending on the DIM_EXT bit, the device functions in one of the following two ways:

- (DIM_EXT = 1) measures the duty cycle on the DIM pin and translates it into a combined LED current value and PWM setting.
- (DIM_EXT = 0) takes the 18-bit value from the TON1 register and translates it into a combined LED current value and PWM setting.

When hybrid dimming is used with an internal dimming setting (DIM_EXT = 0), only the value TON1[17:0] is used. It is not possible to have individual dimming settings for each channel in this mode.

Note that when hybrid dimming is enabled, the ADIM register has no effect.

Figure 3 illustrates the difference between standard and hybrid dimming with phase-shifting enabled.

Hybrid Dimming Operation

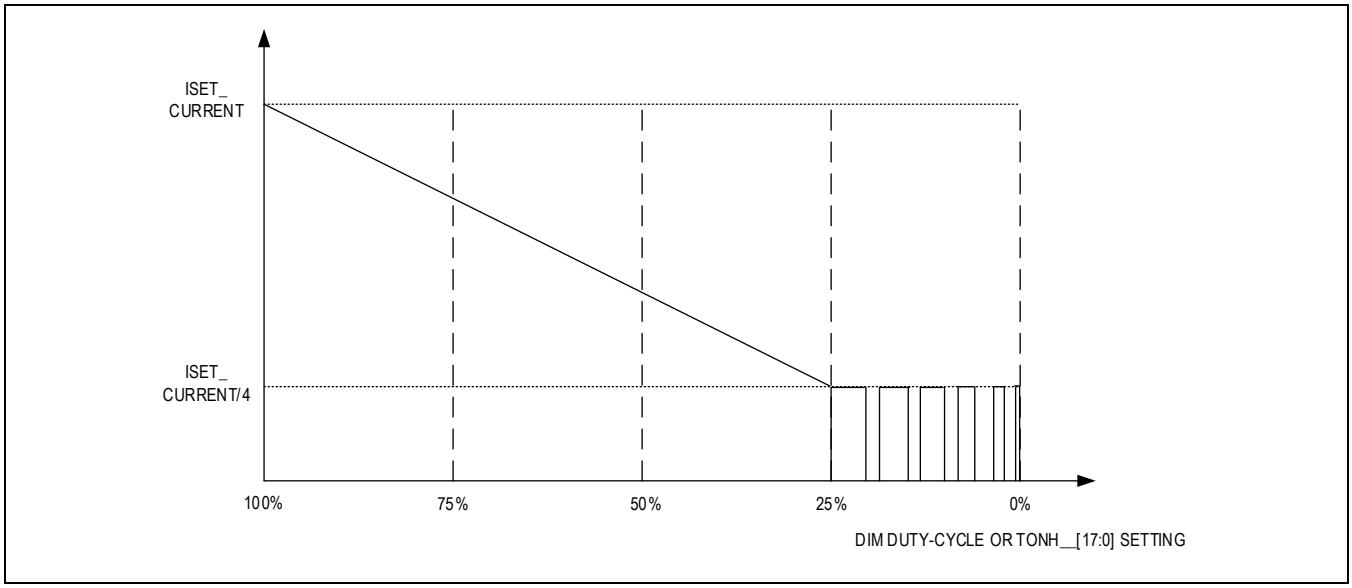


Figure 2. Hybrid Dimming Operation with HDIM[1:0]=10 (25%)

Hybrid Dimming Operation Modes

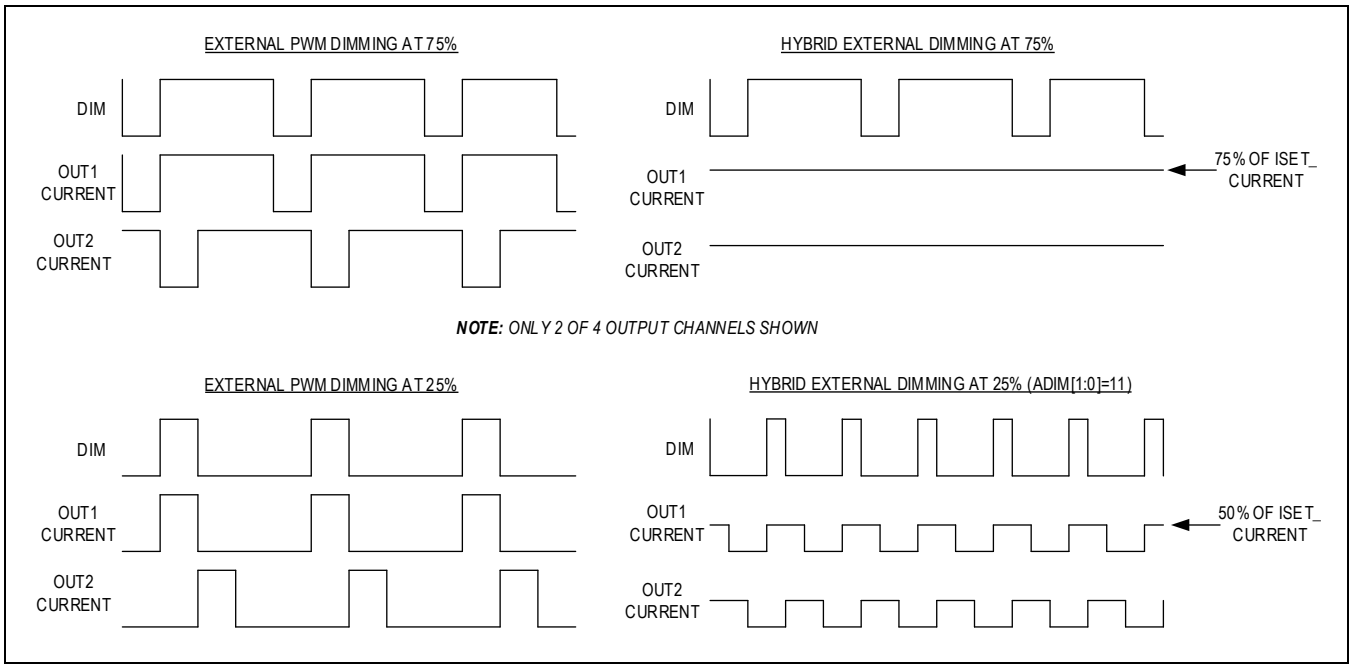


Figure 3. Hybrid Dimming Operation Modes

Brightness Calibration

The full-scale current can also be modified using the ICAL[5:0] field in the register according to *Table 1*:

Table 1. ICAL Setting

ICAL[5:0] SETTING	OUT_ CURRENT AS PERCENTAGE OF 1500/RISET
0x3F	100%
0x3E	99%
0x3D	98%
...	...
0x02	39%
0x01	38%
0x00	37%

Modifications to the full-scale current through the ICAL[5:0] field are effective independently from ADIM and the hybrid dimming settings.

Dimming

Dimming can be performed using an external PWM signal applied to the DIM pin or by writing to the TON_ registers. The signal on the DIM pin is sampled with a 20MHz internal clock except when phase-shifting is disabled, in which case the DIM signal controls the OUT_ outputs directly.

The device tracks frequency changes in the external pulse-width-modulation (PWM) dimming input on DIM in phase-shift mode.

Low-Dimming Mode

The IC's operation changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. If the dimming on-time is lower than 50µs (typ), the device enters low-dimming mode. In this state, the converter switches continuously, and LED short detection is disabled. When the DIM input is greater than 51µs (typ), the device goes back into normal operation, enabling the short-LED detection and switching the power FET only when the effective dimming signal is high.

By setting the BSTFORCE bit in the ISET_REG register to 1, it is possible to force the boost converter to run continuously independent of the state of the DIM input.

Phase-Shift Dimming

When the PSEN bit in register 0x02 is set, phase shifting of the LED strings is enabled. The device automatically sets the phase shift between strings to 90°, 120°, or 180° depending on the number of strings enabled.

Automatic Fade-In/Fade-Out During Dimming

The device can be configured to perform a smooth change in brightness, even when the DIM input duty cycle or TON_ setting is suddenly changed by setting the FADE_IN_OUT bit in the FADING_REG register to 1.

When using the fade function, it is important to maintain the DIM frequency constant while entering and leaving 100% duty cycle. This is necessary in order to avoid erroneous frequency measurement that can change the speed of the fade-in/out.

The step size in the dimming transition is either 6.25% or 12.5%, depending on the setting of the FADE_GAIN bit. The total transition time can be set by writing the TDIM field to a value between 0 to 5, where the value sets the update speed to once every 2TDIM. The transition time depends on the initial and final dimming values according to:

$$t = \frac{1}{f_{DIM}} \times 2^{TDIM} \times \frac{\ln(DIM_F) - \ln(DIM_i)}{FADE_GAIN}$$

where:

f_{DIM} = Dimming frequency

TDIM = TDIM register setting

DIM_F = Final dimming setting

DIM_i = Initial dimming setting

FADE_GAIN = Either 0.0625 or 0.125

For this equation, DIM_F should be larger than DIM_i, but, since the fading function is symmetrical, the values can be swapped if the final dimming ratio is lower than the initial one.

When transitioning to 100% dimming with fading enabled, do not change the input dimming from 100% until the complete fading transition to 100% is complete. Use the above equation to determine the transition time.

Startup Sequence

When the EN pin is taken high (assuming the IN voltage is above its undervoltage-lockout value), the internal regulator and the I²C interface are turned on. The total duration of this phase of the startup is 2ms (max). After this phase, the I²C interface can be used, and the device registers can be written. The ENA bit should be set to 1 to enable the boost and subsequently the OUT_ current sinks. Before setting the ENA bit to 1, fast soft-start can be chosen by setting the FAST_SS bit to 1. When the ENA bit is set high, the device checks the OUT_ channels for short-circuits to GND. If any of the OUT_ pins are detected as shorted to GND, the boost converter does not start. This avoids possible damage.

The corresponding OUT_SG bit(s) are set. The device also detects and disconnects any unused current-sink channels connected to GND by means of a 10kΩ resistor. Alternatively, individual channels can be disabled using the DIS[4:1] bits. The subsequent startup sequence occurs in three stages.

Stage 1

After the ENA bit is set high, the controller turns on the charge-pump for the external nMOSFET. The output current of the charge-pump charges the gate of the external nMOSFET to turn it on. After a 2ms timeout expires, stage 2 of the startup begins.

Stage 2

After the external nMOSFET is turned on, the converter starts switching, and the output begins to ramp. The DAC reference to the error amplifier is stepped up 1 bit at a time until the voltage at BSTMON reaches 480mV or 0.88V when fast soft-start is selected. This stage duration is fixed at approximately 50ms (typ) or 25ms (typ) when fast soft-start is selected. If the BSTMON voltage is greater than 480mV at the end of stage 2, the device transitions directly to stage 3.

The BSTMON pin is sampled at the end of this stage. If its voltage is less than 400mV (typ) or 750mV (typ), FLTB is asserted low, the power converter is turned off, the external nMOSFET on NGATE is turned off, and they all remain off until the ENA bit is toggled.

Stage 3

The third stage begins once stage 2 is complete and the DIM input goes high. During stage 3, the output of the converter is adjusted until the minimum OUT_ voltage falls between the V_{OUTH} and V_{OUTL} comparator limits. The output adjustment is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input pin. If the DIM input is at 100% duty cycle (DIM = high), the DAC output is updated once every 10ms.

The total soft-start time can be calculated using:

$$t_{SS} = 55.25ms + \frac{(V_{LED} + 0.715) - (0.48 \times A_{OVP})}{f_{DIM} \times 0.00975 \times A_{OVP}}$$

where:

t_{SS} = Total soft-start time

55.25ms = Fixed stage 1 + stage 2 duration

V_{LED} = Total forward voltage of the LED strings

0.715V = Midpoint of the window comparator

f_{DIM} = Dimming frequency (use 100Hz for f_{DIM} when input duty cycle is 100%)

0.00975V = 5 times the 1.95mV LSB of the DAC

A_{OVP} = Gain of the BSTMON resistor-divider or 1 + R6/R7

0.48V = Voltage on BSTMON after stage 2

If fast soft-start is enabled, the soft-start is accelerated, and the final value of the voltage on the BSTMON pin is 0.88V.

The equation for the total soft-start time then becomes:

$$t_{SS} = 30.46ms + \frac{(0.88 \times A_{OVP}) - (V_{LED} + 0.715)}{f_{DIM} \times 0.00975 \times A_{OVP}}$$

After the soft-start period, a fault is detected whenever the BSTMON pin falls below V_{BST_UVF}.

Boost Startup

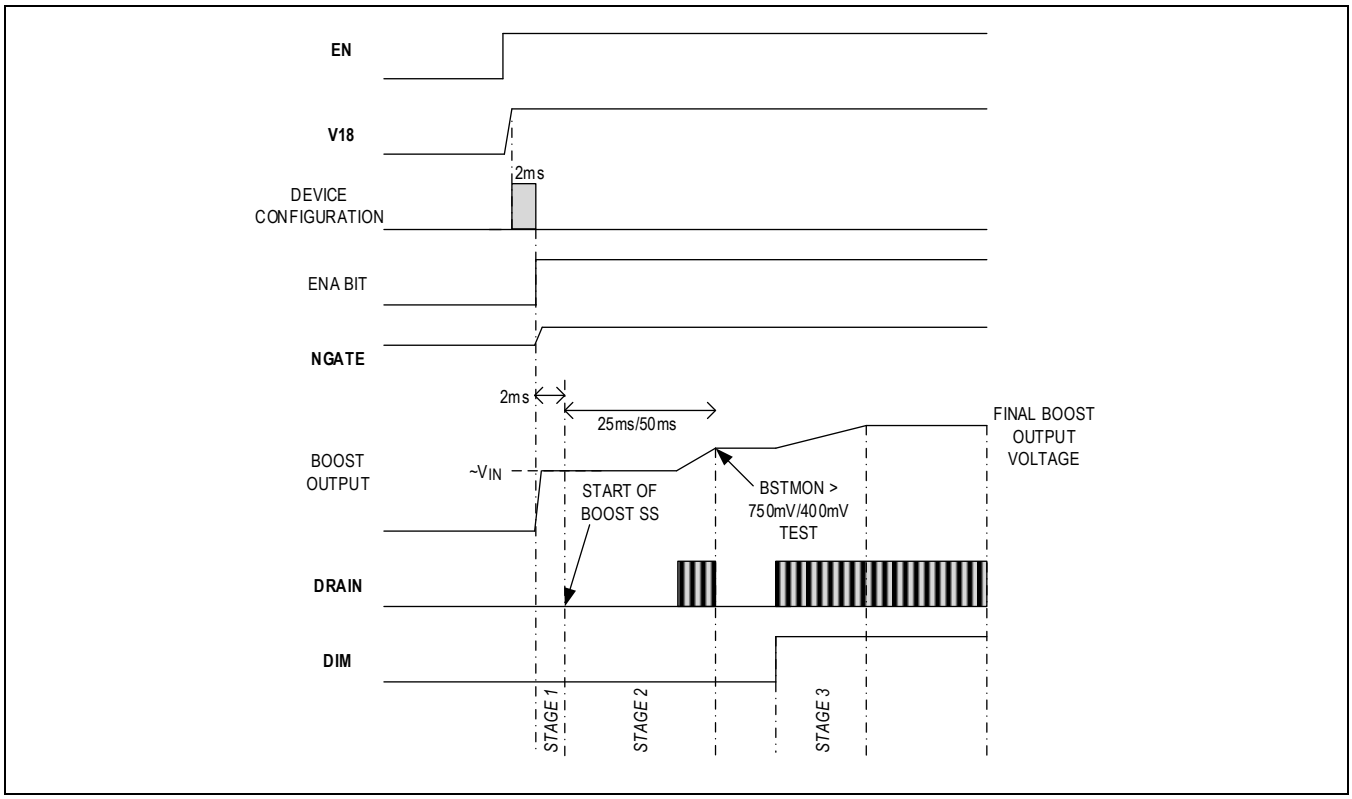


Figure 4. Boost Startup Waveforms

Oscillator Frequency/External Synchronization

The internal oscillator frequency is programmable between 400kHz and 2.2MHz using a timing resistor (R_{RT}) connected from the RT pin to GND. Use the following equation to calculate the value of R_{RT} for the desired switching frequency (f_{SW}):

$$R_{RT} = \frac{26.4 \times 10^6}{f_{SW}} - 0.32$$

where R_{RT} is in kΩ and f_{SW} is in Hz. For example, a 12kΩ resistor on pin RT sets a switching frequency of 2.14MHz.

If the value of the RT resistor is out of range or the pin is shorted to GND, the boost converter cannot start when the ENA bit is set to 1, the RTOOR bit is set, and the FLTB pin goes low.

Synchronize the oscillator with an external clock by AC-coupling the external clock to the RT input. The value of the capacitor used for AC-coupling is C_{SYNC} = 10pF. The duty cycle of the external clock should be 50%. When synchronizing the converter, do not apply the synchronizing signal to the RT pin at startup, as this may cause the RT resistor value check to fail.

At low input voltages and when the switching frequency is above 1.4MHz, the switching frequency is automatically reduced by 30% to enable high-duty-cycle operation and maintain output voltage regulation. This also applies when the device is synchronized to an external frequency.

Spread Spectrum

The IC includes spread spectrum that reduces peak electromagnetic interference (EMI) at the switching frequency and its harmonics. Spread spectrum can be enabled and disabled using the SS_OFF bit in the register SETTING_REG.

The spread-spectrum feature uses a pseudorandom dithering technique where the switching frequency is varied in the range 94% to 106% or 96% to 104% of the programmed switching frequency set through the external resistor from RT to GND. Spread spectrum is disabled if external synchronization is used.

Fault Protection

Fault protection in the IC includes cycle-by-cycle current limiting in the PWM controller, DC-DC converter output-undervoltage protection, output-overvoltage protection, open-LED detection, short-LED detection and protection, and overtemperature shutdown. Thermal shutdown and shorted-LED faults are automatically cleared when the fault is removed; however, FLTB stays low until the relevant fault register is read. It is cleared when the fault condition is removed during thermal shutdown and when shorted LEDs are identified. FLTB is latched low for an open-LED and can be reset by cycling power or by toggling the EN pin.

Open-LED Management and Overvoltage Protection

After the soft-start of the boost converter, the IC detects open-LED strings and disconnects any such strings from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency.

During normal operation, the DC-DC converter output-regulation loop uses the minimum OUT_ voltage as the feedback input. If any LED string is open, the voltage at the opened OUT_ goes to V_{LEDGND}. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, the BSTMON input, and GND. The overvoltage-protection threshold at the DC-DC converter output is determined using the following equation:

$$V_{OUT_BSTMON} = 0.95 \times \left(1 + \frac{R6}{R7}\right)$$

where:

0.95V (typ) = Overvoltage threshold on BSTMON (see the *Functional Diagrams*)

Select VOUT_BSTMON according to the following formula:

$1.1 \times (V_{LED_MAX} + 0.875) < V_{OUT_BSTMON} < 2 \times (V_{LED_MIN} + 0.55)$

where:

V_{LED_MAX} = Maximum expected LED string voltage

V_{LED_MIN} = Minimum expected LED string voltage

Select R6 and R7 so that the voltage at OUT_ does not exceed the absolute maximum rating. As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the internal MOSFET is switched off.

The overvoltage threshold should be set to less than twice the minimum LED voltage to ensure proper operation and so that the BSTMON minimum regulation point of 0.48V (typ) is not breached. When an open-LED overvoltage condition occurs, FLTB is latched low. Any current-sink output with $V_{OUT_} < V_{OOL}$ is permanently disconnected from the minimum voltage detector.

OUT_ Short-to-GND Detection

During device startup, the OUT_ pins are checked for short circuits to ground by sourcing a current I_{CHKLED} into the OUT_ pin and measuring the resultant voltage. If the voltage is below V_{TH_SGND}, the OUT_ is considered shorted to ground and the boost converter does not start. This check will be always active, regardless of the DIS_S2G bit status.

During operation, if any active OUT_ is detected as shorted to GND, the boost converter is disabled and the NGATE output is disabled to turn off the external nMOSFET (DIS_S2G bit set to 0). If retry is enabled (SG_RETRY bit set to 1) the device will perform a retry after 150ms, first performing a boost soft-start. If retry is not enabled, the EN pin or power

to the device must be toggled to reenable the part. Once the fault has been removed, normal operation can be recovered also by toggling the ENA bit without power-cycling the device.

Short-to-GND detection during operation only functions if the DIM on-time is greater than 50µs.

Shorted-LED Detection

The IC checks for shorted LEDs after the current in any channel is turned on. A shorted-LED is detected at OUT_ if the following condition is met:

$V_{OUT_} > V_{SLDET}$

where either V_{SLDET} = 12x the voltage set on the RSDT pin or V_{SLDET} = SLDET[1:0] when the RSDT pin is connected to V18.

If a short is detected on any of the strings, the affected LED strings are disconnected and the FLTB output flag asserts low until the device detects that the shorts are removed. If SLDET [1:0] bits are left to their default value, short-LED detection will be permanently disabled when connecting R_{SDT} to V18.

Shorted-LED detection is disabled in low-dimming mode and when the current set by the ADIM input is lower than 6.25% of the ISET setting. Shorted-LED detection is also disabled in cases where all active OUT_ channels rise above 2V (typ). This can occur in a boost-converter application when the input voltage becomes higher than the total LED string voltage drop, such as during a battery load dump. During a load dump or other input voltage transient, an erroneous shorted-LED fault may be indicated if one of the outputs exceeds the shorted-LED detection threshold before the others. This condition is most likely to occur when phase-shifting is enabled.

When the DIM input is connected continuously high, the OUT_ pins are periodically scanned to detect shorted LEDs. The scan frequency is 100Hz.

Thermal Warning

If the junction temperature of the device reaches T_{WARN} or if the TEMP pin reaches the voltage representing the temperature T1, the overtemperature warning (OTW) bit in the DIAG_REG register is set. In addition, if the OTWMASK bit is 0 the FLTB pin is asserted low.

Thermal Shutdown

The IC includes thermal protection that operates at a temperature of T_{SHDN}. When the thermal-shutdown temperature is reached, the device is immediately disabled so it can cool. When the junction temperature falls by 17°C, the device is re-enabled and the boost converter performs a soft-start. When a thermal shutdown occurs, the FLTB pin goes low.

Temperature Foldback

When an NTC temperature sensor is connected between GND and a resistor (RT1) connected to the V18 supply, with a further resistor (RT2) connected from the junction of the NTC and RT1 to the TEMP pin, temperature foldback is implemented. When the temperature reaches the temperature T1 (set by RT1), the current in the LEDs is reduced according to the linear scheme shown in *Figure 5*. The slope of the current reduction is set nominally by RT2. The MAX25512B is designed to be used with the NTCLE100E3 or a similar NTC device. *Table 2* illustrates some examples of values of RT1 and RT2 to obtain certain values of T1 and T_{DELTA}.

Table 2. Temperature Foldback RT1 and RT2 Values

RT1	RT2	T1	T_{DELTA}
20kΩ	1.9kΩ	+60°C	+40°C
14kΩ	2kΩ	+70°C	+30°C
10kΩ	1.5kΩ	+80°C	+25°C

Above Temperature T1

When the temperature reaches T1, the OTW bit in register DIAG_REG is asserted. When the temperature reaches T1 + T_{DELTA} = T_{OFF}, the LED current is turned off and the FLTB pin asserts low.

Temperature Foldback Curve

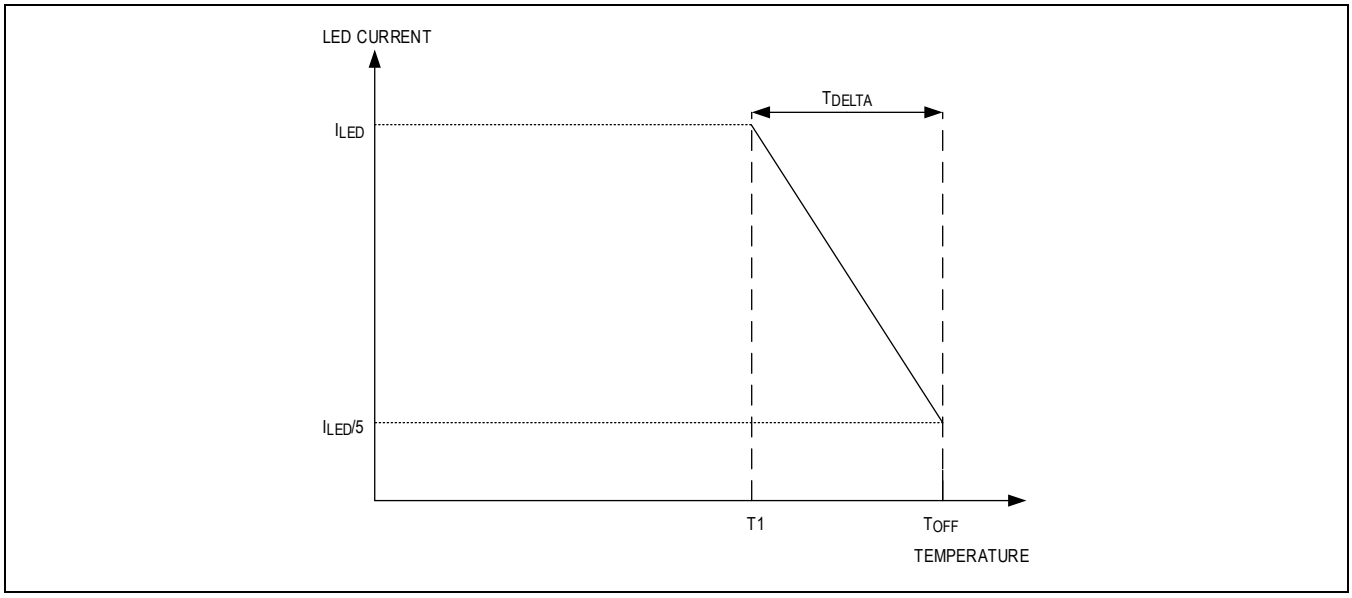


Figure 5. Temperature Foldback Curve

TEMP External Circuit

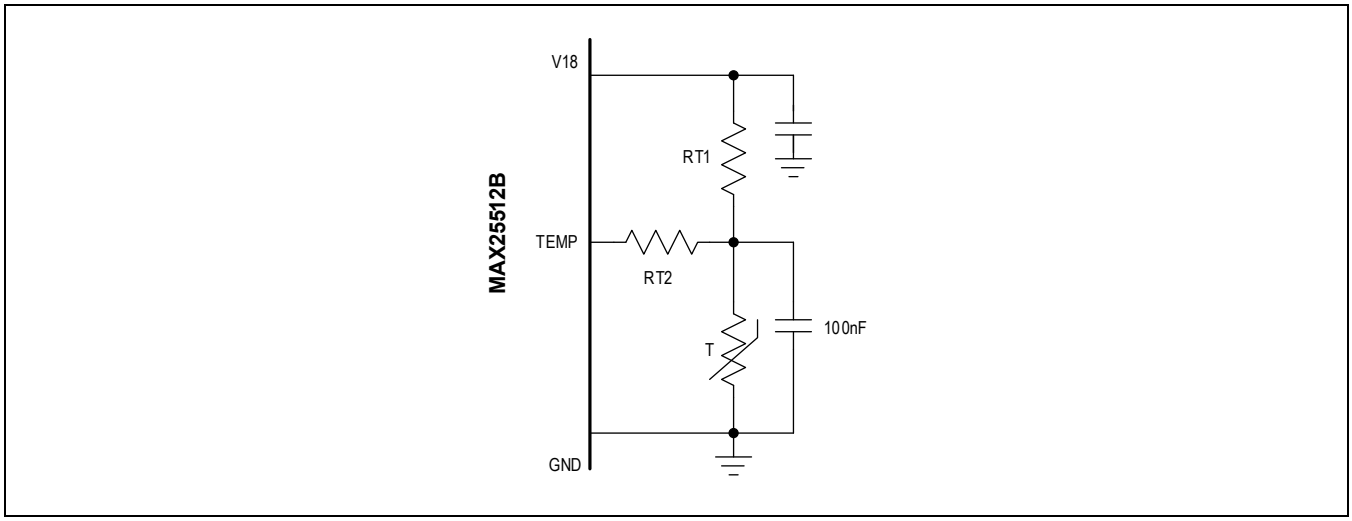


Figure 6. TEMP External Circuit

I²C Interface

Target Address

Table 3. I²C Target Address

	DEVICE ADDRESS							WRITE ADDRESS	READ ADDRESS
	A6	A5	A4	A3	A2	A1	A0		
MAX25512BATGA	0	1	0	0	0	1	0	0x44	0x45
MAX25512BATGB	1	1	0	0	0	1	0	0xC4	0xC5

Register Map

MAX25512B

ADDRESS	NAME	MSB							LSB
USER_REGISTERS									
0x00	DEV_ID_REG[7:0]	DEV_ID[7:0]							
0x01	REV_ID_REG[7:0]	–	–	–	–	REV_ID[3:0]			
0x02	ISET_REG[7:0]	–	–	–	–	BSTFORCE	FAST_SS	ENA	PSEN
0x03	IMODE_REG[7:0]	LO_DIM4	LO_DIM3	LO_DIM2	LO_DIM1	DIM_EXT	HDIM	HDIM_THR_1_0[1:0]	
0x04	ADIM_REG[7:0]	ADIM[7:0]							
0x05	TON1H_REG[7:0]	TON1H[7:0]							
0x06	TON1L_REG[7:0]	TON1L[7:0]							
0x07	TON2H_REG[7:0]	TON2H[7:0]							
0x08	TON2L_REG[7:0]	TON2L[7:0]							
0x09	TON3H_REG[7:0]	TON3H[7:0]							
0x0A	TON3L_REG[7:0]	TON3L[7:0]							
0x0B	TON4H_REG[7:0]	TON4H[7:0]							
0x0C	TON4L_REG[7:0]	TON4L[7:0]							
0x0D	TON1_4LSB_REG[7:0]	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
0x0E	SETTING_REG[7:0]	SG_RETRY	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
0x0F	DISABLE_REG[7:0]	–	–	CP_DIS	DIS_S2G	DIS4	DIS3	DIS2	DIS1
0x10	FADING_REG[7:0]	–	–	–	FADE_GAIN	FADE_IN_OUT	TDIM[2:0]		
0x11	OPEN_REG[7:0]	–	–	–	–	OUT4O	OUT3O	OUT2O	OUT1O
0x12	SHORTGND_REG[7:0]	–	–	–	–	OUT4SG	OUT3SG	OUT2SG	OUT1SG
0x13	SHORTED_LED_REG[7:0]	–	–	–	–	OUT4SL	OUT3SL	OUT2SL	OUT1SL

ADDRESS	NAME	MSB							LSB
0x14	MASK_REG[7:0]	–	–	–	BSTUVMASK	OMASK	SGMASK	OTWMASK	SLMASK
0x15	DIAG_REG[7:0]	RTOOR	–	ISETOOR	BSTUV	BSTOV	HW_RST	OTW	OT
0x16	ICAL[7:0]	–	–	ICAL[5:0]					

Register Details

DEV_ID_REG (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0x12							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DEV_ID	7:0	Device ID 0x28.

REV_ID_REG (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	REV_ID[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
REV_ID	3:0	Device revision ID.

ISET_REG (0x2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BSTFORCE	FAST_SS	ENA	PSEN

Reset	–	–	–	–	0b0	0b0	0b0	0b1
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BSTFORCE	3	When 1, this bit forces the boost converter to run continuously and independent of the dimming signal.
FAST_SS	2	Selects slow or fast boost soft-start. Set to 1 for fast soft-start.
ENA	1	Boost converter and LED outputs enable bit. Set to 1 to enable the device.
PSEN	0	When 0, phase shifting is disabled. When 1, phase shifting is enabled.

IMODE_REG (0x3)

BIT	7	6	5	4	3	2	1	0
Field	LO_DIM4	LO_DIM3	LO_DIM2	LO_DIM1	DIM_EXT	HDIM	HDIM_THR_1_0[1:0]	
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b00	
Access Type	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
LO_DIM4	7	When 1, indicates channel 4 is in low-dimming mode.
LO_DIM3	6	When 1, indicates channel 3 is in low-dimming mode.
LO_DIM2	5	When 1, indicates channel 2 is in low-dimming mode.
LO_DIM1	4	When 1, indicates channel 1 is in low-dimming mode.
DIM_EXT	3	When 1, dimming through the DIM pin is enabled. When 0, dimming is controlled using the TON__ registers.
HDIM	2	When 1, hybrid dimming is enabled. Default value is 0.
HDIM_THR_1_0	1:0	Set hybrid dimming threshold. 00 – 6.25% 10 – 12.5% 10 – 25% 11 – 50%

ADIM_REG (0x4)

BIT	7	6	5	4	3	2	1	0
Field	ADIM[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ADIM	7:0	8-bit linear analog dimming value. 0xFF is full-scale current, and each bit represents a current step of 0.4%.

TON1H_REG (0x5)

On-time setting for channel 1 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1H	7:0	High byte of 18-bit TON setting for channel 1.

TON1L_REG (0x6)

On-time setting for channel 1 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1L	7:0	Middle byte of 18-bit TON setting for channel 1.

TON2H_REG (0x7)

On-time setting for channel 2 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2H	7:0	High byte of 18-bit TON setting for channel 2.

TON2L_REG (0x8)

On-time setting for channel 2 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2L	7:0	Middle byte of 18-bit TON setting for channel 2.

TON3H_REG (0x9)

On-time setting for channel 3 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON3H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3H	7:0	High byte of 18-bit TON setting for channel 3.

TON3L_REG (0xA)

On-time setting for channel 3 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON3L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3L	7:0	Middle byte of 18-bit TON setting for channel 3.

TON4H_REG (0xB)

On-time setting for channel 4 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON4H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4H	7:0	High byte of 18-bit TON setting for channel 4.

TON4L_REG (0xC)

On-time setting for channel 4 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON4L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4L	7:0	Middle byte of 18-bit TON setting for channel 4.

TON1_4LSB_REG (0xD)

LSBs of on-time setting for all channels with 50ns resolution.

BIT	7	6	5	4	3	2	1	0
Field	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
Reset	0b11		0b11		0b11		0b11	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
TON4LSB	7:6	2 least significant bits of 18-bit TON setting for channel 4.
TON3LSB	5:4	2 least significant bits of 18-bit TON setting for channel 3.
TON2LSB	3:2	2 least significant bits of 18-bit TON setting for channel 2.
TON1LSB	1:0	2 least significant bits of 18-bit TON setting for channel 1.

SETTING_REG (0xE)

BIT	7	6	5	4	3	2	1	0
Field	SG_RETRY	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
Reset	0x0	0b001			0b0	0b0	0b00	
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td>SG_RETRY</td><td>7</td><td>When 1 this bit enables retry when a short-to-GND is detected during device operation.</td><td>0x0: Retry disabled
0x1: Retry enabled</td></tr>
<tr><td>FPWM</td><td>6:4</td><td>These bits set the PWM frequency in internal PWM mode.
<table>
<tr><th>FPWM2</th><th>FPWM1</th><th>FPWM0</th><th>PWM FREQUENCY (Hz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>153</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>203</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>305</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>610</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>980</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1220</td></tr>
</table></td><td></td></tr>
</table>

BITFIELD	BITS	DESCRIPTION	DECODE
		1 1 0 1401 1 1 1 1634	
SS_OFF	3	When 1, spread-spectrum switching is disabled. Default value is 0.	
SSL	2	When spread spectrum is enabled, the SSL bit chooses the amount of spread. When 0, the spread is nominally ±6%. When 1, the spread is ±4%. When changing the percentage, disable spread spectrum using the SS_OFF bit first. Then, change the value of SSL. Finally, reenable spread spectrum using SS_OFF.	
SLDET	1:0	Shorted-LED-Threshold Settings. 00 Disabled 01 3V 10 6V 11 8V	

DISABLE_REG (0xF)

Channel-disable bits.

BIT	7	6	5	4	3	2	1	0
Field	–	–	CP_DIS	DIS_S2G	DIS4	DIS3	DIS2	DIS1
Reset	–	–	0b0	0x1	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CP_DIS	5	When 1, this bit disables the internal charge pump, which drives the NGATE pin. Set to 1 when an external series switch is not used. Setting CP_DIS to 1 during operation will cause complete shutdown of the device and is not recommended.
DIS_S2G	4	When 1 this bit disables short-to-GND detection during device operation.
DIS4	3	Set bit to 1 to disable OUT4. This must be done before ENA is written to 1.
DIS3	2	Set bit to 1 to disable OUT3. This must be done before ENA is written to 1.
DIS2	1	Set bit to 1 to disable OUT2. This must be done before ENA is written to 1.
DIS1	0	Set bit to 1 to disable OUT1. This must be done before ENA is written to 1.

FADING_REG (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FADE_GAIN	FADE_IN_OUT	TDIM[2:0]		
Reset	–	–	–	0b0	0b0	0b000		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_GAIN	4	When set to 1, the fade-in-out function has a gain of 12.5%, otherwise 6.25%	
FADE_IN_OUT	3	When set to 1, the fade-in-out function for the LED dimming is enabled.	
TDIM	2:0	Sets the fading update time interval according to 2^{TDIM}. TDIM can be between 0 and 5. When set to 0, fading is updated on every dimming cycle.	0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: N/A 0x7: N/A

OPEN_REG (0x11)

Open-string diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4O	OUT3O	OUT2O	OUT1O
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4O	3	If 1, an open is detected on channel 4.
OUT3O	2	If 1, an open is detected on channel 3.
OUT2O	1	If 1, an open is detected on channel 2.
OUT1O	0	If 1, an open is detected on channel 1.

SHORTGND_REG (0x12)

Short-to-ground diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4SG	OUT3SG	OUT2SG	OUT1SG
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4SG	3	If 1, a short-to-ground is detected on channel 4 at startup.
OUT3SG	2	If 1, a short-to-ground is detected on channel 3 at startup.
OUT2SG	1	If 1, a short-to-ground is detected on channel 2 at startup.
OUT1SG	0	If 1, a short-to-ground is detected on channel 1 at startup.

SHORTED_LED_REG (0x13)

Shorted-LED diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4SL	OUT3SL	OUT2SL	OUT1SL
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4SL	3	If 1, a shorted-LED condition is detected on channel 4.
OUT3SL	2	If 1, a shorted-LED condition is detected on channel 3.
OUT2SL	1	If 1, a shorted-LED condition is detected on channel 2.
OUT1SL	0	If 1, a shorted-LED condition is detected on channel 1.

MASK_REG (0x14)

Mask register for the FLTB pin.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BSTUVMASK	OMASK	SGMASK	OTWMASK	SLMASK
Reset	–	–	–	0b0	0b0	0b0	0b1	0b0

Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BSTUVMASK	4	When 1, a boost undervoltage fault does not cause the FLTB pin to assert low.
OMASK	3	When 1, an open-LED fault does not cause the FLTB pin to assert low.
SGMASK	2	When 1, a short-to-ground LED fault does not cause the FLTB pin to assert low.
OTWMASK	1	When 1, an overtemperature warning does not cause the FLTB pin to assert low.
SLMASK	0	When 1, a shorted-LED fault does not cause the FLTB pin to assert low.

DIAG_REG (0x15)

Boost state, overtemperature-warning/shutdown diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	RTOOR	–	ISETOOR	BSTUV	BSTOV	HW_RST	OTW	OT
Reset	0b0	–	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RTOOR	7	This bit is set to 1 if the resistor on the RT pin is out of the expected range. When this happens, the device cannot operate.
ISETOOR	5	When 1, this bit indicates that the ISET current is out of range. This is more than likely due to an incorrect resistor value on ISET. In this condition, the IC stops operation.
BSTUV	4	If 1, an undervoltage is detected on the boost output, and the boost is disabled.
BSTOV	3	If 1, the boost converter is at its overvoltage limit.
HW_RST	2	If 1, the device has just emerged from a hardware reset (power-up). This bit is reset after the first read from this register.
OTW	1	If 1, the junction temperature of the device is over T_{WARN}, or the temperature foldback circuit has reached the temperature T1.
OT	0	If 1, the junction temperature of the device exceeds T_{SHDN}, and the device is shut down.

ICAL (0x16)

BIT	7	6	5	4	3	2	1	0

Field	–	–	ICAL[5:0]
Reset	–	–	0x3F
Access Type	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ICAL	5:0	LED current calibration register.

Applications Information

DC-DC Converter

The MAX25512B DC-DC converter offers the capability to work with two different converter topologies that have the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string-forward voltage is always greater than the input supply voltage range, use the boost-converter topology. If the LED string-forward voltage falls within the supply voltage range, use the SEPIC topology.

The boost-converter topology provides the highest efficiency of these topologies. The SEPIC configuration requires either two inductors or a coupled inductor and a coupling capacitor.

Power-Circuit Design

First, select a converter topology based on the factors listed above. Determine the required input supply voltage range, the maximum voltage needed to drive the LED strings including the minimum 0.875V across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}), as shown in the following equation:

$I_{LED} = I_{STRING} \times N_{STRING}$

where:

I_{STRING} = Current per string

N_{STRING} = Number of strings used

Next, calculate the maximum duty cycle (D_{MAX}) using one of the following equations, depending on the configuration:

Boost Configuration:

$$D_{MAX} = \frac{(V_{LED} + V_{D1} - V_{IN_MIN})}{(V_{LED} + V_{D1} - V_{DS})}$$

SEPIC Configuration:

$$D_{MAX} = \frac{V_{LED} + V_{D1}}{(V_{IN_MIN} - V_{DS} + V_{LED} + V_{D1})}$$

where:

V_{D1} = Forward drop of the rectifier diode in volts (approximately 0.6V)

V_{IN_MIN} = Minimum input supply voltage

V_{DS} = Drain-to-source voltage of the internal MOSFET when it is on, given by I_{LAVG} x $R_{DS(ON)}$ where $R_{DS(ON)}$ = 125mΩ

Select the switching frequency (f_{SW}) depending on space, noise, and efficiency constraints.

Boost Configuration

In the converter configurations, the average inductor current varies with the input voltage; the maximum average current occurs at the lowest input voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔIL). The recommended maximum peak-to-peak ripple is 60% of the average inductor current, but lower and higher ripple values are also acceptable.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (I_{LP}) in amps (A):

$$IL_{AVG} = \frac{I_{LED}}{(1 - D_{MAX})}$$

Allowing the peak-to-peak inductor ripple (ΔIL) to be ±30% of the average inductor current:

$\Delta IL = IL_{AVG} \times 0.3 \times 2$

and:

$$IL_{p} = IL_{AVG} + \frac{\Delta IL}{2}$$

Calculate the minimum inductance value (L_{MIN}) in henries (H) with the inductor current ripple set to the maximum value:

$$L_{MIN} = \frac{(V_{IN_MIN} - V_{DS}) \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where V_{DS} is IL_{AVG} x 0.125. Choose an inductor with a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts. One of the inductors (L2) takes LED current as the average current, and the other (L1) takes input current as the average current.

Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL2_{AVG}$) and peak inductor currents ($IL1_P$, $IL2_P$) in A.

$$IL1_{AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a margin of 10% to account for the converter losses.

$IL2_{AVG} = I_{LED}$

Assuming the peak-to-peak inductor ripple (ΔIL) is ±30% of the average inductor current:

$\Delta IL1 = IL1_{AVG} \times 0.3 \times 2$

and:

$$IL1_{P} = IL1_{AVG} + \frac{\Delta IL1}{2}$$

and:

$\Delta IL2 = IL2_{AVG} \times 0.3 \times 2$

and:

$$IL2_{P} = IL2_{AVG} + \frac{\Delta IL2}{2}$$

Calculate the minimum inductance values ($L1_{MIN}$ and $L2_{MIN}$) in H with the inductor current ripple set to the values previously calculated.

$$L1_{MIN} = \frac{(V_{IN_MIN} - V_{DS}) \times D_{MAX}}{f_{SW} \times \Delta IL1}$$

$$L2_{MIN} = \frac{(V_{IN_MIN} - V_{DS}) \times D_{MAX}}{f_{SW} \times \Delta IL2}$$

Choose inductors with a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$ and current ratings of greater than $IL1_P$ and $IL2_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

To simplify further calculations, consider a single inductor equivalent to L1 and L2 connected in parallel. The combined inductance value and current is calculated as follows:

$$L = \frac{L1 \times L2}{L1 + L2}$$

and:

$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$

where IL_{AVG} represents the total average current through both of the inductors in the SEPIC configuration. Use these values in the calculations in the following sections.

Select coupling-capacitor C_S so that its peak-to-peak ripple is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series-resonant circuit comprising L1, C_S, and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of C_S:

$$C_S = \frac{I_{LED} \times D_{MAX}}{V_{IN_MIN} \times 0.02 \times f_{SW}}$$

where,

C_S = Minimum value of the coupling capacitor in farads (F)

0.02 = 2% ripple factor

Output Capacitor Selection

The output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across the constant-current sink outputs because the LED-string voltages are stable due to the constant current. For the MAX25512B, limit peak-to-peak output-voltage ripple to 250mV to get stable output current.

The equivalent series resistance (ESR), equivalent series inductance (ESL), and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce this, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming, the amount of ceramic capacitors on the output is usually minimized. In this case, an additional electrolytic or aluminum organic polymer capacitor can provide most of the bulk capacitance.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. Select a diode with low reverse-recovery losses to reduce the MOSFET switching losses and avoid increased EMI. The voltage rating of the diode should be 20% higher than the maximum boost-converter output voltage and its current rating greater than the following:

$IL_{AVG} \times (1 - D_{MAX}) \times 1.2$

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to fall within the window comparator limits of V_{OUTL} and V_{OUTH} when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter (when BSTFORCE = 0) and stores the previous boost output-voltage value for use during the next on cycle.

The switching converter small-signal-transfer function has a right-half plane (RHP) zero in the boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate.

Worst-Case RHP Zero Frequency (f_{ZRHP}):

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED}}$$

SEPIC Configuration:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED} \times D_{MAX}}$$

The standard way to avoid this zero is to roll off the loop gain to 0dB at a frequency of less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f_{P1}) that is calculated for the boost configuration, as shown in the following equation:

$$f_{P1} = \frac{I_{LED}}{\pi \times V_{LED} \times C_{OUT}}$$

SEPIC Configuration:

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{\pi \times V_{LED} \times C_{OUT}}$$

Compensation components R_{COMP} and C_{COMP} perform two functions. C_{COMP} introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain, and R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this zero is placed at f_{P1} to provide a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP} needed to fix the total loop gain at f_{P1} so the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency is calculated for the boost configuration as follows:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX})}$$

SEPIC Configuration:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP} \times D_{MAX}}{5 \times f_{P1} \times g_{m_COMP} \times V_{LED} \times (1 - D_{MAX})}$$

where:

R_{COMP} = Compensation resistor in Ω

A_{OVP} = BSTMON resistor-divider gain (a value >> 1)

R_{CS} = Current-sense resistor of value 0.066Ω

g_{m_COMP} = Transconductance of the error amplifier (630µS)

The value of C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{Z1} \times R_{COMP}}$$

where f_{Z1} is the compensation zero placed at 1/5 the crossover frequency; in turn, it is set at 1/5 the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency can fall below the 0dB crossover frequency. An additional pole may be required to cancel out this zero placed at the same frequency. This can be added by connecting a capacitor from the COMP pin directly to GND with a value shown as follows:

$$C_{PAR} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

where,

R_{ESR} = Capacitor ESR value

C_{OUT} = Output-capacitor value

External Disconnect MOSFET Selection

An external nMOSFET can be used to disconnect the boost output from the battery in the event of an output overload or short condition. There is no need for the nMOSFET in the case of the SEPIC or buck-boost, since this protection is not necessary. Leave the NGATE pin disconnected when an external nMOSFET is not used. If it is necessary to have output-short protection for the boost even at power-up, then the current through the nMOSFET must be sensed (refer to the MAX25512B evaluation kit (EV kit) for a reference circuit). Once the current-sense voltage exceeds a certain threshold, it should limit the input current to the programmed threshold. This threshold should be set at a sufficiently high level so it never trips at startup or under normal operating conditions. Check the safe operating area (SOA) of the nMOSFET to confirm that the current-limit trip threshold and voltage on the MOSFET do not exceed the limits of the SOA curve of the nMOSFET at the highest operating temperature.

Ensure that the maximum value of the nMOSFET gate threshold voltage is lower than 4V for reliable operation.

V_{OUT} to OUT_ Bleed Resistors

The OUT_ pins have a leakage specification of 4µA (max) in cases where all OUT_ pins are shorted to 36V (see $I_{OUTLEAK}$ in the *Electrical Characteristics* table). This leakage current is dependent on the OUT_ voltage and is higher at higher voltages. Therefore, in cases where large numbers of LEDs are connected in series, a 100kΩ (or larger) bleed resistor can be placed in parallel with the LED string to prevent the OUT_ leakage current from turning on the LEDs dimly, even when the DIM signal is low (see resistors R8–R11 in the *Typical Application Circuits*).

Thermal Considerations

The on-chip power dissipation of the MAX25512B comprises four main factors:

1. Current-sink power loss = 0.875V × I_{LED}

2. Device operating current power loss = V_{IN} × 1.3mA

3. Power due to $R_{DS(ON)}$ of the internal MOSFET = BoostDutyCycle × I_{LAVG}^2 × 0.125

4. Power due to switching losses in the internal MOSFET = 0.5 × V_{LED} × I_{LED} × $t_{R/F}$ × f_{SW} where $t_{R/F}$ is the rise/fall time of the boost converter switching node approximated to 6ns.

Calculate the total power dissipation by adding the values calculated above. The junction temperature at the maximum ambient temperature can then be calculated as follows:

$T_J = T_A + P_{TOT} \times \theta_{JA}$

where:

T_A = Ambient temperature

θ_{JA} = Junction-to-ambient thermal resistance of the package (36°C/W on a four-layer board). Ensure that the junction temperature does not exceed +150°C.

As an example, consider an application with a minimum operating voltage of 9V, a total output current of 400mA at 28.7V, and an average 1.5A inductor current. With a switching frequency of 400kHz, the total power dissipation is calculated in the following equation:

$$P_{TOT} = (0.875 \times 0.4) + (9 \times 0.0013) + (\frac{28.7}{28.7 + 9} \times 1.5^2 \times 0.125) + (0.5 \times 28.7 \times 0.4 \times 6E - 9 \times 400000) = 0.59W$$

The maximum junction temperature at an ambient temperature of +85°C is shown in the following equation:

T_J = 85 + 0.59 × 36 = + 106°C

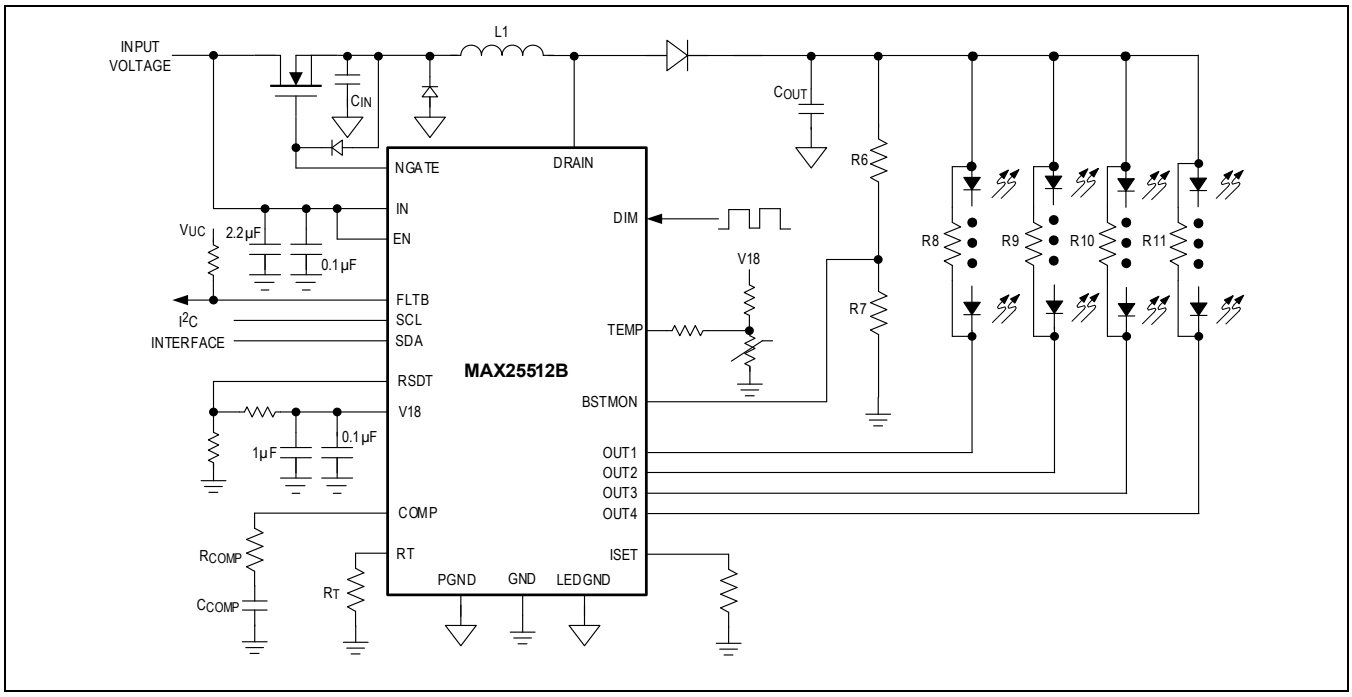
PCB Layout Considerations

LED driver circuits based on the MAX25512B use a high-frequency switching converter to generate the voltage for LED strings. Take proper care while laying out the circuit to ensure correct circuit operation. The switching-converter part of

the circuit has nodes with fast voltage changes that can lead to undesirable effects on the sensitive parts of the circuit. Use the following guidelines to reduce noise as much as possible:

- Connect the bypass capacitors on V18 as close as possible to the device. Make the connections directly to the device's V18 and GND pins. Connect the GND pin of the device to the analog ground plane and to the exposed pad of the device. Place the analog ground plane on an inner layer.
- Place a power ground plane for the switching-converter power circuit under the power components (input filter capacitor, output filter capacitor, inductor, and rectifier diode). Connect the PGND pins to the power ground plane and to the exposed pad of the device. Connect all other ground connections to the power ground plane using vias close to the terminals.
- There are two loops in the power circuit that carry high-frequency switching currents. One loop exists when the internal MOSFET is on (from the input filter capacitor positive terminal, through the inductor and internal MOSFET, to the input capacitor negative terminal). The other loop exists when the MOSFET is off (from the input capacitor positive terminal, through the inductor, rectifier diode, output filter capacitor, to the input capacitor negative terminal). Analyze these two loops in order to make the loop areas as small as possible. Wherever possible, have a return path on the power ground plane for the switching currents on the top-layer copper traces or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also decreases radiation during switching.
- Connect the power ground plane for the constant-current LED driver part of the circuit to the LEDGND pin. Also connect the LEDGND pin to the device's exposed pad.
- Add a small bypass capacitor (22pF to 47pF) to the BSTMON input. Place the capacitor as close as possible to the pin to suppress high-frequency noise.
- Boost output voltage for the LED strings must be taken directly from the output capacitors and not from the boost diode anode.
- Input and output capacitors need good grounding with wide traces and multiple vias to the ground plane.
- To enhance device power dissipation, add multiple vias under the device's exposed pad connected to an area of copper on the backside of the PCB. This is important for maintaining device efficiency and reducing junction temperature during operation.
- Refer to the EV kit for a reference layout.

Typical Application Circuits



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	7-BIT I²C ADDRESS
MAX25512BATGA/V+	-40°C to +125°C	24 TQFN-EP	0x22
MAX25512BATGA/VY+	-40°C to +125°C	24 TQFN-EP	0x22
MAX25512BATGB/V+	-40°C to +125°C	24 TQFN-EP	0x62
MAX25512BATGB/VY+	-40°C to +125°C	24 TQFN-EP	0x62

/V Denotes an automotive-qualified part.
+ Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
EP = Exposed pad.
Y = Side-wettable (SW) package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/24	Initial release	—
1	6/24	Corrections to DMAX and LMIN formulas in the Applications Information section	35, 36
2	6/24	Removed asterisks and future product footer from the Ordering Information Table	41

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