MAX20069C

Automotive I²C-Controlled 4-Channel 150mA Backlight Driver and 4-Output TFT-LCD Bias

General Description

The MAX20069C is a highly integrated TFT power supply and LED backlight driver IC for automotive TFT-LCD applications. The IC integrates one buck-boost converter, one boost converter, two gate-driver supplies, and a boost/SEPIC converter that can power one to four strings of LEDs in the display backlight.

The source-driver power supplies consist of a synchronous boost converter and an inverting buck-boost converter that can generate voltages up to +18V and down to -7V. The positive source driver can deliver up to 120mA, while the negative source driver is capable of 100mA. The positive source-driver supply-regulation voltage (V_{POS}) is set by connecting an external resistor-divider on FBP or through I²C. The negative source-driver supply voltage (V_{NEG}) is always tightly regulated to -V_{POS} (down to a minimum of -7V). The source-driver supplies operate from an input voltage between 2.8V and 5.5V.

The gate-driver power supplies consist of regulated charge pumps that generate from +28V to -21.5V and can deliver up to 3mA each.

The IC features a quad-string LED driver that operates from a separate input voltage (V_{BATT}) and can power up to four strings of LEDs with 150mA (max) of current per string. The IC features logic-controlled pulse-width-modulation (PWM) dimming, with minimum pulse widths as low as 500ns with the option of phase shifting the LED strings with respect to one another. When phase shifting is enabled, each string is turned on at a different time, reducing the input and output ripple, as well as audible noise. With phase shifting disabled, the current sinks turn on simultaneously and parallel connection of current sinks is possible.

The startup and shutdown sequences for all power domains are controlled using one of the seven preset modes, which are selectable through a resistor on the SEQ pin or through the I²C interface.

The MAX20069C is available in a 40-pin (6mm x 6mm) TQFN package with an exposed pad, and operates over the -40°C to +105°C ambient temperature range.

Applications

- Automotive Dashboards
- Automotive Central Information Displays
- Automotive Head Up Displays
- Automotive Navigation Systems

Benefits and Features

- 4-Output TFT-LCD Bias Power
  - 2.8V to 5.5V Input for the TFT-LCD Section
  - Integrated 440kHz or 2.2MHz Boost and Buck-Boost Converters
  - Positive and Negative 3mA Gate Voltage Regulators with Adjustable Output Voltage
  - Flexible Resistor-Programmable Sequencing through the SEQ Pin
  - Undervoltage Detection on All Outputs
  - Low-Quiescent-Current Standby Mode
- 4-Channel LED Backlight Driver
  - Up to 150mA Current per Channel
  - 4.5V to 42V Input Voltage Range
  - Integrated Boost/SEPIC Controller (440kHz or 2.2MHz)
  - Dimming Ratio 10,000:1 at 200Hz
  - Adaptive Voltage Optimization to Reduce Power Dissipation in the LED Current Sinks
  - Open-String, Shorted-LED, and Short-to-GND Diagnostics
- Low EMI
  - Phase-Shift Dimming of LED Strings
  - Spread Spectrum on LED Driver and TFT
  - Selectable Switching Frequency
- I²C Interface for Control and Diagnostics
  - Fault Indication through the FLTB pin and I²C
- Overload and Thermal Protection
- -40°C to +105°C Ambient Temperature Operation
- 40-Pin (6mm x 6mm) TQFN Package with Exposed Pad

Ordering Information appears at end of data sheet.

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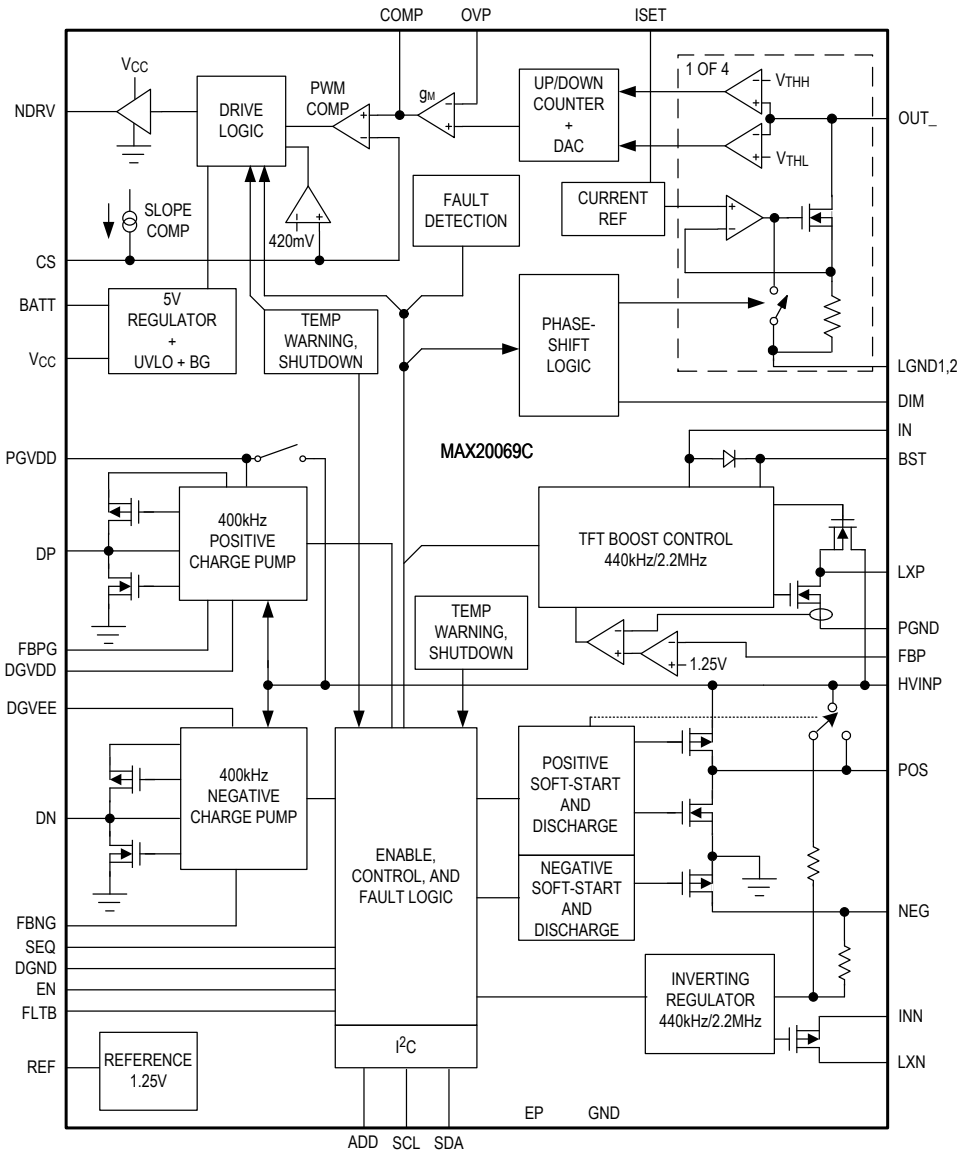
Simplified Block Diagram



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Absolute Maximum Ratings

BATT, OUT_, OVP to GND ..... -0.3V to +52V
IN, INN, V_{CC}, FLTB, DIM, CS, EN, SDA, SCL, ADD to GND..... -0.3V to +6V
COMP, NDRV, ISET to GND..... -0.3V to V_{CC} + 0.3V
REF, FBP, FBNG, FBPG, SEQ to GND .....-0.3V to V_{IN} + 0.3V
LXP, HVINP, BST to GND..... -0.3V to +26V
LXP, PGND RMS Current Rating 2.4A
BST to LXP..... -0.3V to +6V
PGVDD, POS, DP, DN to GND ..... -0.3V to V_{HVINP} + 0.3V
LXN to INN ..... -24V to +0.3V
LXN, INN RMS Current Rating 1.6A
DGVDD to GND..... -0.3V to +40V
NEG, DGVEE to GND.....-24V to +0.3V
GND to PGND.....-0.3V to +0.3V
GND to LGND1, LGND2 .....-0.3V to +0.3V
GND to DGND .....-0.3V to +0.3V
Continuous Power Dissipation ((T_A = +70°C))
40-Pin TQFN-EP (derate 37mW/°C above +70°C), (Multilayer Board).....2963mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

40 TQFN

Package Code	T4066-5C
Outline Number	21-0141
Land Pattern Number	90-0055
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	38
Junction to Case (θ_{JC})	1
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	27
Junction to Case (θ_{JC})	1

40 TQFN-SW

Package Code	T4066Y-6C
Outline Number	21-100361
Land Pattern Number	90-0055
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	38°C/W
Junction to Case (θ_{JC})	1°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	27°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
IN Voltage Range			2.8		5.5	V
IN UVLO Threshold	IN_UVLO_R	Rising	2.45	2.55	2.65	V
IN UVLO Hysteresis	IN_UVLO_HYS			100		mV
IN Shutdown Current	I_{IN_SHDN}	EN = GND, V_{IN} = 3.6V		4	10	µA
IN Quiescent Current	I_{IN_Q}	V_{EN} = V_{IN} = 3.6V, no switching		2.2		mA
REFERENCE						
Reference Output Voltage	V_{REF_NL}	No load	1.232	1.25	1.268	V
Reference UVLO Threshold	REF_UVLO_R	REF rising		1	1.2	V
Reference UVLO Hysteresis	REF_UVLO_HYS			100		mV
Reference Load Regulation	REF_LDREG	0 < I_{REF} < 100µA		10	20	mV
Reference Line Regulation	REF_LNREG	2.7V < V_{IN} < 5.5V		2	5	mV
BOOST REGULATOR						
Output Voltage Range	V_{HVINP}	V_{IN} ≥ 4V	V_{IN} + 1		18	V
		V_{IN} < 4V	5		18	
POS Voltage Range, I²C Mode		SEQ connected to IN	5		18	V
POS Adjustment Step Size, I²C Mode		SEQ connected to IN		0.1		V
POS Output Regulation	V_{POS}	vpos[7:0] = 0x1A	6.37	6.5	6.63	V
Operating Frequency	f_{BOOSTH}	swfreq_tft bit = 0, dither disabled	1900	2200	2500	kHz
	f_{BOOSTL}	swfreq_tft bit = 1, dither disabled	360	430	500	
Frequency Dither	f_{BOOSTD}			+4/-4		%
Oscillator Maximum Duty Cycle	BOOST_MAXDC		90	94	98	%
FBP Regulation Voltage	V_{FBP}		1.23	1.25	1.27	V
FBP Load Regulation	FBP_LDREG	1mA < I_{POS} < 100mA		-1		%
FBP Line Regulation	FBP_LNREG	V_{IN} = 2.8V to 5.5V	-0.4	0	+0.4	%
FBP Input Bias Current	I_{FBP_BIAS}	V_{FBP} = 1.25V, T_A = +25°C	20	100	200	nA
Low-Side Switch On-Resistance	LXP_RON_LS	I_{LXP} = 0.1A		0.2	0.4	Ω
Synchronous Rectifier On-Resistance				0.25	0.5	Ω
Synchronous Rectifier Zero-Crossing Threshold	ZX_TH			20		mA

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LXP Leakage Current	LXP_L_LEAK	EN = GND, V_{LXP} = 15V			20	µA
LXP Current Limit, High Setting	I_{LIMPH}	Duty cycle = 80%, lxp_lim_low = 0	1.7	2.0	2.3	A
LXP Current Limit, Low Setting	I_{LIMPL}	Duty cycle = 80%, lxp_lim_low = 1	0.74	1	1.3	A
Soft-Start Period	BOOST_SSTIME	Current-limit ramp		10		ms
INVERTING REGULATOR						
INN Voltage Range			2.7		5.5	V
INN Quiescent Current		EN = GND, V_{INN} = 3.6V			1	µA
	I_{INN}	EN = V_{INN} = 3.6V		1		mA
Operating Frequency	f_{INVL}	swfreq_tft bit = 0, dither disabled	1900	2200	2500	kHz
	f_{INVH}	swfreq_tft bit = 1, dither disabled	360	430	500	
Frequency Dither	f_{INV_DITH}			±4		%
Oscillator Maximum Duty Cycle	INV_MAXDC			94		%
V_{POS} + V_{NEG} Regulation Voltage	$V_{NEG_POS_REG}$	V_{INN} = 2.8V to 5.5V, V_{POS} = 7.1V, 1mA < I_{NEG} < 100mA, I_{POS} = no load	-60	0	70	mV
Inverting-Regulator Disable Threshold	V_{POSth}	Above this value on POS, the inverting regulator is turned off	7.5	7.9	8.2	V
LXN On-Resistance	LXN_RON	INN to LXN, I_{LXN} = 0.1A		0.6	1.2	Ω
LXN Leakage Current	LXN_LEAK	V_{IN} = 3.6V, V_{LXN} = V_{NEG} = -7V, T_A = +25°C			20	µA
LXN Current Limit, High Setting	I_{LIMNH}	Duty cycle = 80%, neg_lim_low = 0	1.2	1.5	1.8	A
LXN Current Limit, Low Setting	I_{LIMNL}	Duty cycle = 80%, neg_lim_low = 1	0.6	0.75	1.1	A
Soft-Start Period	INV_SSTIME	Current-limit ramp		5		ms
POSITIVE CHARGE-PUMP REGULATOR						
PGVDD Operating Voltage Range	V_{PGVDD}		5		V_{HVINP}	V
HVINP-PGVDD Threshold For DGVDD Charge-Pump Start-Up	$V_{HVINP-PGVDD}$	V_{HVINP} = 5V	400	510	620	mV
HVINP-DP Current Limit			15			mA
Oscillator Frequency			300	400	500	kHz
DGVDD Voltage Range, I²C Mode			8		28	V
DGVDD Adjustment Step Size, I²C Mode				0.5		V
DGVDD Output Voltage		I²C mode, DGVDD set to 16V (0x10)	15.68	16	16.32	V
FBPG Regulation Voltage	V_{FBPG_REG}		1.23	1.25	1.27	V

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBPG Line Regulation		V_{HVINP} = 11V to 15V		0	0.2	%/V
FBPG Input Bias Current		V_{FBPG} = 1.25V, T_A = +25ºC	-100		100	nA
DP On-Resistance, High		I_{DP} = +10mA		30	60	Ω
DP On-Resistance, Low		I_{DP} = -10mA		15	30	Ω
NEGATIVE CHARGE-PUMP REGULATOR						
HVINP to DN Current Limit			15			mA
Oscillator Frequency			300	400	500	kHz
DGVEE Voltage Range, I²C Mode			-22		-8	V
DGVEE Adjustment Step Size, I²C Mode				0.5		V
DGVEE Output-Voltage Accuracy			-2		+2	%
FBNG Regulation Voltage			-12	0	+12	mV
FBNG Line Regulation		V_{NEG} = -11V to -15V		0	0.2	%/V
FBNG Input Bias Current		V_{FBNG} = 0V, T_A = +25°C	-100		+100	nA
DN On-Resistance, High		I_{DN} = 10mA		30	60	Ω
DN On-Resistance, Low		I_{DN} = -10mA		15	30	Ω
SEQUENCE SWITCHES						
POS Output-Voltage Range	V_{POS}	Tracks HVINP	5		18	V
POS On-Resistance		RON_{POS} (HVINP-POS), I_{POS} = 80mA		1.5	2.6	Ω
POS Charge Current Limit		Expires after soft-start period	120			mA
	$ILIM_{POS}$	Expires after soft start period	120		380	
POS Discharge Resistance			2	3.4	6	kΩ
POS Soft-Start Charge Time		Current mode (0A to full current limit)		5		ms
NEG Output-Voltage Range	V_{NEG}	Tracks HVINN	-7			V
NEG Discharge Resistance			2	3.4	6	kΩ
PGVDD On-Resistance		(HVINP-PGVDD), I_{PGVDD} = 3mA		30	60	Ω
PGVDD Current Limit		Expires when PGVDD charging is completed	15	50		mA
DGVDD Input Voltage Range			6		22	V

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DGVDD Discharge Resistance			7	12	17	kΩ
DGVEE Input Voltage Range			-22		-6	V
DGVEE Discharge Resistance			7	12	17	kΩ
SEQ Bias Current	I_{SEQ}	V_{SEQ} = 1V	9.4	10	10.5	µA
TFT FAULT PROTECTION						
HVINP Undervoltage Fault		Before the end of POS soft-startup, V_{HVINP} falling, I²C mode	75	80	85	%
POS Undervoltage-Fault Threshold		After POS soft startup, V_{POS} falling, I²C mode	75	80	85	%
NEG Undervoltage-Fault Threshold		V_{NEG} rising (% of POS setting)	75	80	85	%
FBP Undervoltage-Fault Threshold		V_{FBP} falling, stand-alone mode	0.95	1	1.05	V
FBPG Undervoltage-Fault Threshold		V_{FBPG} falling, stand-alone mode	0.95	1	1.05	V
FBNG Undervoltage-Fault		V_{FBNG} rising, standalone mode.	160	210	260	mV
DGVDD Undervoltage Fault		I²C mode, DGVDD falling	75	80	85	%
DGVEE Undervoltage Fault		I²C mode, DGVEE rising	75	80	85	%
Undervoltage-Fault Timer				50		ms
HVINP Short-Circuit Fault		Before end of POS soft-start, HVINP falling, I²C mode	30	40	50	%
FBP Short-Circuit Fault Threshold		V_{FBP} falling, stand-alone mode	30	40	50	%
POS Overload Fault Threshold	POS_OL	POS falling (% of V_{HVINP})	70	73	76	%
NEG Short-Circuit Fault Threshold		V_{NEG} rising (% of POS setting)	30	40	50	%
LED BACKLIGHT DRIVER						
Input Voltage Range	V_{BATT}		4.5		42	V
		V_{BATT} = V_{CC}	4.5		5.5	
Quiescent Supply Current	BATT_IQ	V_{DIM} = 5V, V_{OVP} = 1.3V, OUT1–OUT4 open		5	8	mA
Standby Supply Current	BATT_ISHDN	Backlight block disabled			1	µA
Undervoltage Lockout	$UVLO_{BATT}$	V_{BATT} rising, V_{DIM} = 5V	3.7	4.15	4.45	V
Undervoltage-Lockout Hysteresis	$UVLO_{BATTHYS}$			500		mV

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} REGULATOR						
Output Voltage	V_{CC}	5.75V < V_{BATT} < 36V, I_{VCC} = 1mA to 10mA, C_{VCC} = 2.2µF	4.8	5	5.2	V
Dropout Voltage	VCC_{DROP}	V_{BATT} = 4.5V, I_{VCC} = 5mA		0.05	0.12	V
V_{CC} Undervoltage Lockout, Rising	UVLOVCCR		4.05	4.2	4.35	V
V_{CC} Undervoltage Lockout, Falling	UVLOVCCF		3.75	3.9	4.04	V
Short-Circuit Current Limit	I_{VCC_SC}	V_{CC} shorted to GND		50		mA
BOOST/SEPIC CONTROLLER						
Switching Frequency	f_{SW}	Dither disabled	1980	2200	2420	kHz
Minimum Off-Time	t_{OFF_MIN}	Switching frequency 2.2MHz		40		ns
Frequency Dither	f_{DITH}			±6		%
SLOPE COMPENSATION						
Peak Slope-Compensation Current Ramp Per Cycle	I_{SLOPE}	Current ramp added to CS	42	50	60	µA
CS LIMIT COMPARATOR						
CS Threshold Voltage	V_{CS_MAX}		380	410	440	mV
CS Input Current	I_{CS}		-1		+1	µA
ERROR AMPLIFIER						
OUT_ Regulation High Threshold	V_{OUT_UP}	$V_{OUT_}$ falling	0.9	0.97	1.05	V
OUT_ Regulation Low Threshold	V_{OUT_DOWN}	$V_{OUT_}$ rising	0.65	0.72	0.8	V
Transconductance	g_M		400	700	880	µS
COMP Sink Current	I_{COMP_SINK}	V_{COMP} = 2V	200	480	800	µA
COMP Source Current	I_{COMP_SRC}	V_{COMP} = 1V	200	480	800	µA
MOSFET DRIVER						
NDRV On-Resistance	R_{NDRV_LS}	I_{NDRV} = -20mA		1.2	2	Ω
	R_{NDRV_HS}	I_{NDRV} = +20mA		1.5	3	
LED CURRENT SINK						
ISET Resistance Range	R_{ISET}		10		75	kΩ
Full-Scale OUT_ Output Current	$I_{OUT_}$	R_{ISET} = 10kΩ	143.5	150	156.5	mA
	I_{OUT100}	R_{ISET} = 15kΩ	96	100	104	
	I_{OUT50}	R_{ISET} = 30kΩ	47.5	50	52.5	
	I_{OUT20}	R_{ISET} = 75kΩ	17.5	20	22.5	
ISET Output Voltage	V_{ISET}		1.22	1.25	1.28	V

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Regulation Between Strings	$I_{OUT_MATCH150}$	$I_{OUT_}$ = 150mA	-2.2		+2.2	%
	$I_{OUT_MATCH50}$	$I_{OUT_}$ = 50mA	-2.5		+2.5	
Current-Setting Resolution	I_{OUT_LSB}			0.5		%
OUT_ Leakage Current	I_{OUT_LEAK}	$V_{OUT_}$ = 48V, DIM = 0, all OUT_ pins shorted together		8	12	µA
$I_{OUT_}$ Rise Time	I_{OUT_TR}	10% to 90% $I_{OUT_}$		150		ns
$I_{OUT_}$ Fall Time	I_{OUT_TF}	90% to 10% $I_{OUT_}$		50		ns
LED FAULT DETECTION						
LED Short-Detection Threshold	V_{THSHRT}	I²C mode, bit configuration = 11 (00: short detection disabled), default value in stand-alone mode	7.3	7.8	8.3	V
		I²C mode, led_short_th[1:0] = 10	5.6	6	6.4	
		I²C mode, led_short_th[1:0] = 01	2.8	3	3.2	
LED Short-Detection Disable Threshold	V_{THSHRT_DIS}	All active OUT_s rising		2.8		V
OUT_ Check-LED-Source Current	I_{OUT_CKLED}		45	60	70	µA
OUT_ Short-to-GND Detection Threshold	V_{OUT_GND}		250	300	350	mV
OUT_ Unused-Detection Threshold	V_{OUT_UN}		1.15	1.25	1.35	V
OUT_ Open-LED-Detection Threshold	V_{OUT_OPEN}		250	300	350	mV
Shorted-LED-Detection Flag Delay	t_{SHRT}			7		µs
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
Overvoltage-Trip Threshold	V_{OVPTH}	V_{OVP} rising	1.18	1.23	1.28	V
Overvoltage Hysteresis	V_{OVPHYS}			70		mV
OVP Input Bias Current	I_{OVP}	0 < V_{OVP} < 1.3V	-500		+500	nA
Undervoltage-Trip Threshold	$V_{OVPUVLO}$	V_{OVP} falling	0.405	0.425	0.44	V
Boost Undervoltage-Detection Delay	OVPUVLO_BLK			10		µs
Boost Undervoltage-Blanking Time		After soft-startup		60		ms
LOGIC INPUTS and OUTPUTS (EN, SCL, ADD, SDA, DIM)						
EN Blanking Time	EN_BLK			10		µs
DIM Input, Logic-High	V_{DIM_IH}		2.1			V
DIM Input, Logic-Low	V_{DIM_IL}				0.8	V

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIM Input Hysteresis	V_{DIM_HYS}			300		mV
DIM Pullup Current	I_{DIM_PUP}			5		µA
EN, ADD Input, Logic-High			2.1			V
EN, ADD Input, Logic-Low					0.8	V
SCL, SDA Input, Logic-High			0.38 x V_{IN}			V
SCL, SDA Input, Logic-Low					0.11 x V_{IN}	V
Input Current			-1		+1	µA
SEQ Level to Set I2C Mode				0.92 x V_{IN}		V
FLTB, SDA Output Low Voltage	V_{OL}	Sinking 5mA			0.4	V
FLTB, SDA Output Leakage Current	I_{LEAK}	5.5V	-1		+1	µA
FLTB Frequency for Fault Detection	f_{FLTB}		0.84	0.97	1.08	kHz
FLTB Pin Duty Cycle on LED String Fault	FLTB_DLED	Stand-alone mode		25		%
FLTB Pin Duty Cycle on TFT-Rail Fault	FLTB_DTFT	Stand-alone mode; fault on at least one of the POS, NEG, DGVDD, or DGVEE pins		75		%
FLTB Pin Duty Cycle on LED String and TFT-Rail Fault	FLTB_D	Stand-alone mode, fault on at least one of the POS, NEG, DGVDD, or DGVEE pins, and LED driver		50		%
FLTB Duty Cycle on Thermal-Shutdown Event		FLTB continuously low		0		%
THERMAL WARNING/SHUTDOWN						
Thermal-Warning Threshold	T_{WARN}	Backlight only, T_{RISING}		125		°C
Thermal-Warning Hysteresis	T_{WARN_HYS}	Backlight only		10		°C
Thermal-Shutdown Threshold	T_{SHDN}	T_{RISING}		160		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			15		°C
I2C INTERFACE						
Clock Frequency	f_{SCL}				1	MHz
Setup Time (Repeated) START	$t_{SU:STA}$	(Note 2)	260			ns
Hold Time (Repeated) START	$t_{HD:STA}$	(Note 2)	260			ns

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, Typical operating circuit, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Low Time	t_{LOW}	(Note 2)	500			ns
SCL High Time	t_{HIGH}	(Note 2)	260			ns
Data Setup Time	$t_{SU:DAT}$	(Note 2)	50			ns
Data Hold Time	$t_{HD:DAT}$	(Note 2)	0			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 2)	260			ns
Spike Suppression		(Note 2)		50		ns

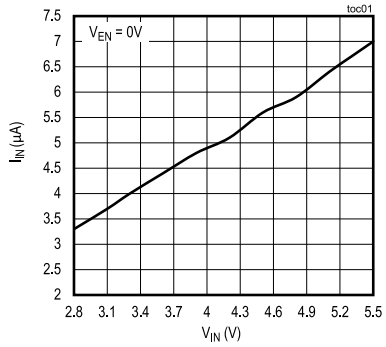
Note 1: Limits are 100% tested at TA = +25°C, TA = +105°C and TA = -40°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design. Not production tested.

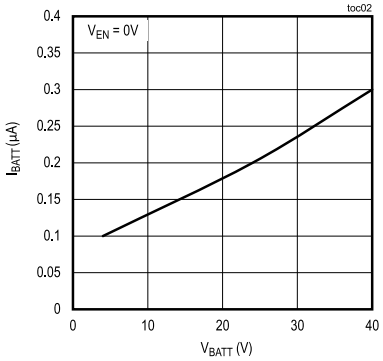
Typical Operating Characteristics

(T_A = 25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 14V unless otherwise noted.)

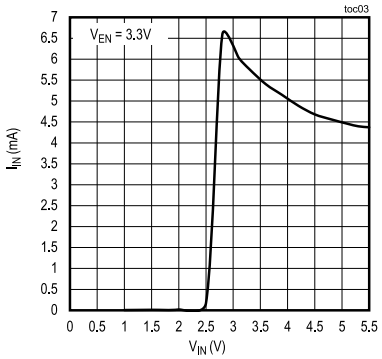
TOTAL IN SUPPLY STANDBY CURRENT vs. IN SUPPLY VOLTAGE



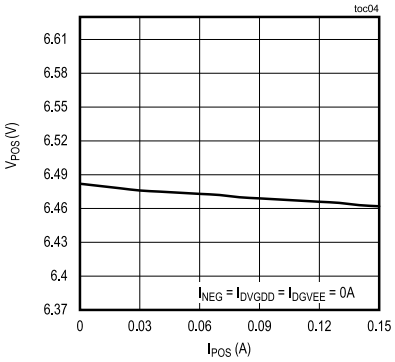
TOTAL BATT SUPPLY STANDBY CURRENT vs. BATT SUPPLY VOLTAGE



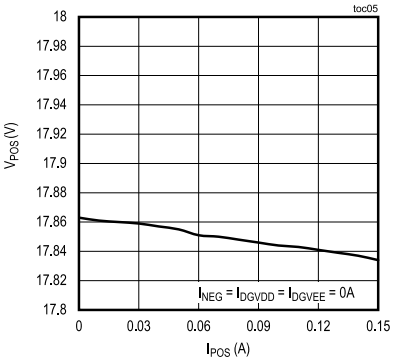
IN SUPPLY CURRENT vs. IN SUPPLY VOLTAGE



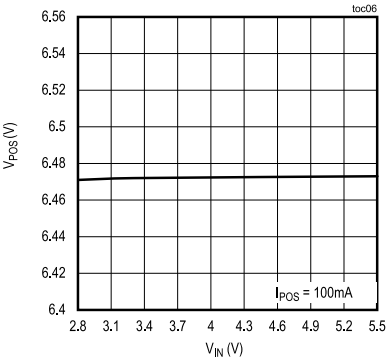
POS LOAD REGULATION AT 6.5V



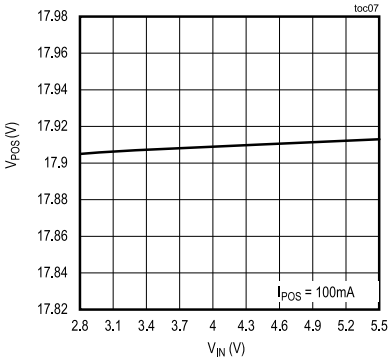
POS LOAD REGULATION AT 18V



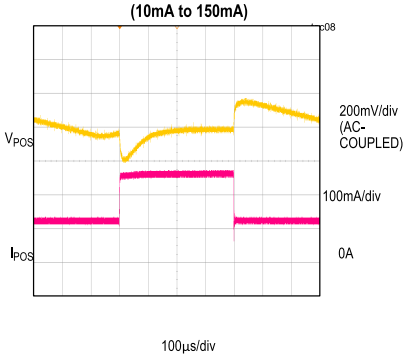
POS LINE REGULATION AT 6.5V



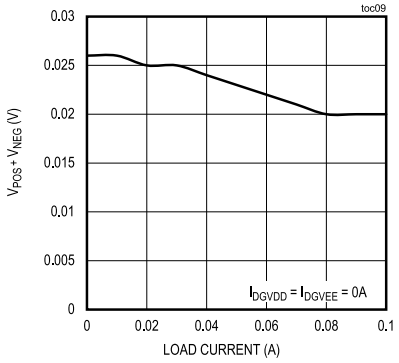
POS LINE REGULATION AT 18V



POS LOAD TRANSIENT RESPONSE (10mA to 150mA)



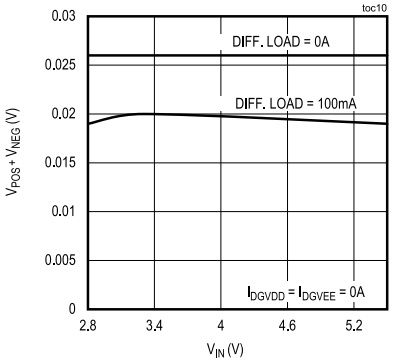
V_{POS} + V_{NEG} LOAD REGULATION



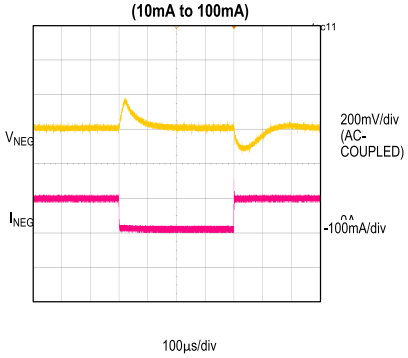
Typical Operating Characteristics (continued)

(T_A = 25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 14V unless otherwise noted.)

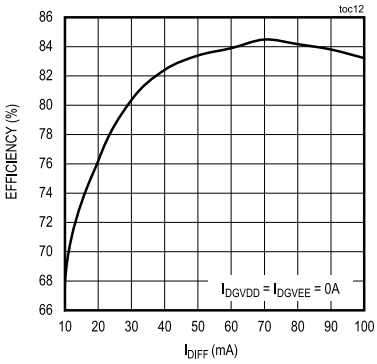
V_{POS} + V_{NEG} LINE REGULATION



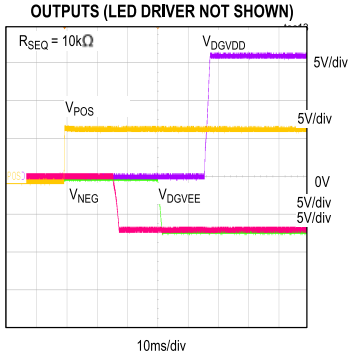
NEG LOAD TRANSIENT RESPONSE (10mA to 100mA)



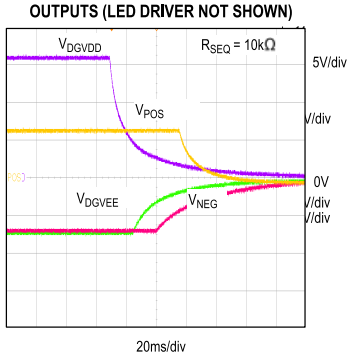
EFFICIENCY WITH DIFFERENTIAL LOAD FROM V_{POS} TO V_{NEG}



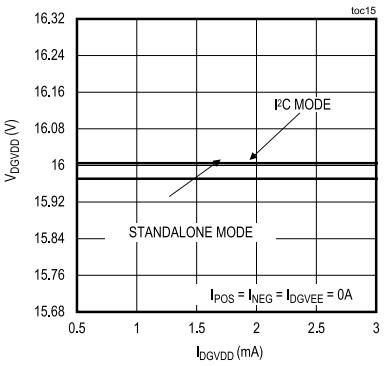
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS (LED DRIVER NOT SHOWN)



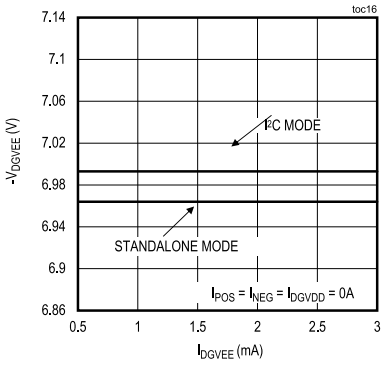
POWER-OFF SEQUENCE OF ALL SUPPLY OUTPUTS (LED DRIVER NOT SHOWN)



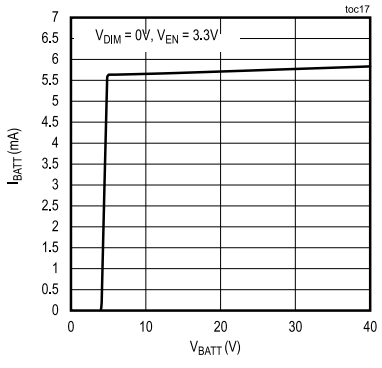
DGVDD LOAD REGULATION



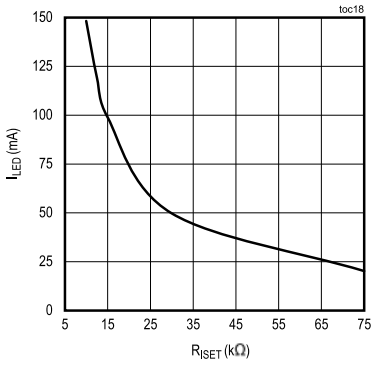
DGVEE LOAD REGULATION



BATT SUPPLY CURRENT vs. BATT SUPPLY VOLTAGE



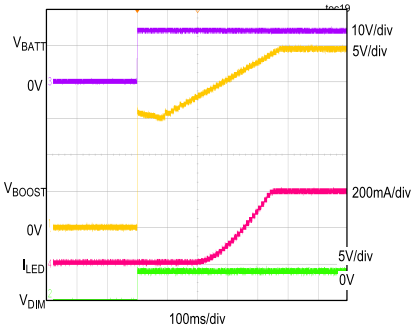
I_{LED} vs. R_{ISET}



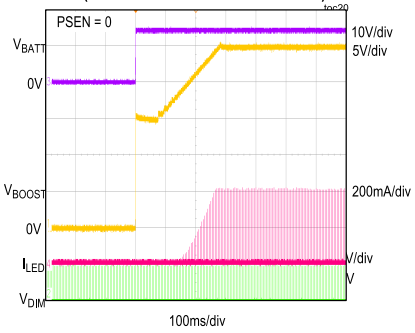
Typical Operating Characteristics (continued)

(T_A = 25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 14V unless otherwise noted.)

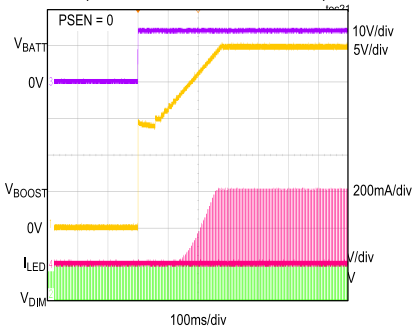
STARTUP WAVEFORM OF LED DRIVER AT DIM = 100% (SLOW MODE)



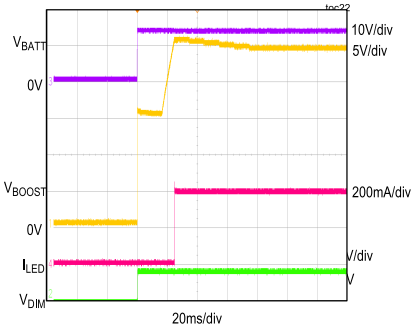
STARTUP WAVEFORM OF LED DRIVER WITH DIM PW = 25µs (SLOW MODE - DIM FREQ = 200Hz)



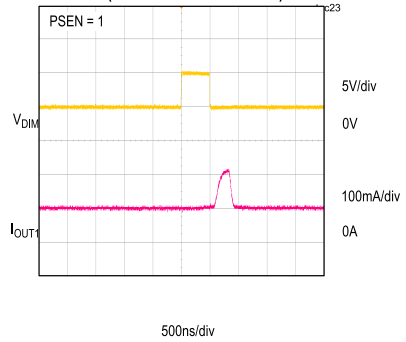
STARTUP WAVEFORM OF LED DRIVER WITH DIM DUTY = 25% (SLOW MODE - DIM FREQ = 200Hz)



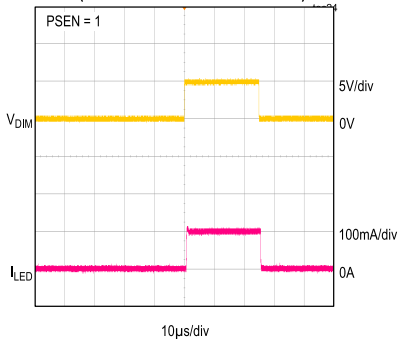
STARTUP WAVEFORM OF LED DRIVER AT DIM = 100% (FAST MODE)



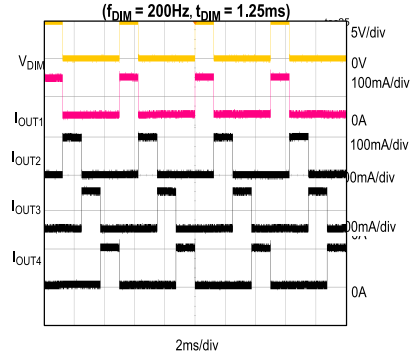
LED SWITCHING WITH DIMMING PULSE WIDTH OF 500ns (DIMMING FREQ = 200Hz)



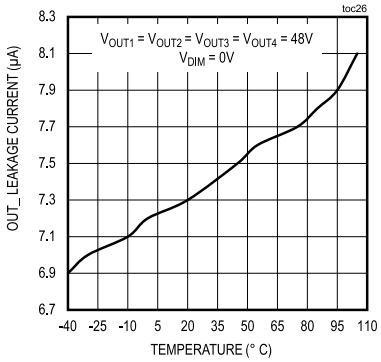
LED SWITCHING WITH DIMMING PULSE WIDTH OF 25µs (DIMMING FREQUENCY = 200Hz)



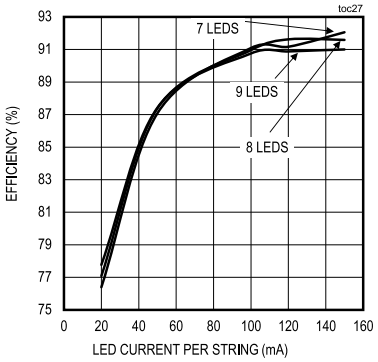
PHASE-SHIFTED LED OUTPUT CURRENTS (f_{DIM} = 200Hz, t_{DIM} = 1.25ms)



OUT_ LEAKAGE CURRENT vs. TEMPERATURE



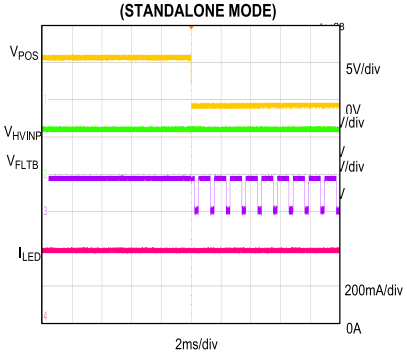
EFFICIENCY vs. LED CURRENT FOR LED DRIVER



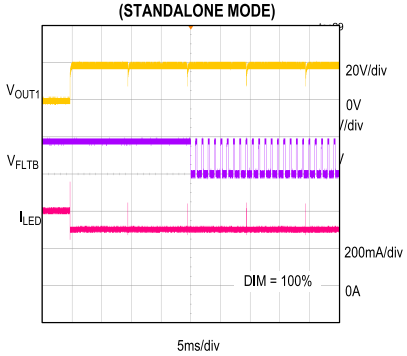
Typical Operating Characteristics (continued)

(T_A = 25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 14V unless otherwise noted.)

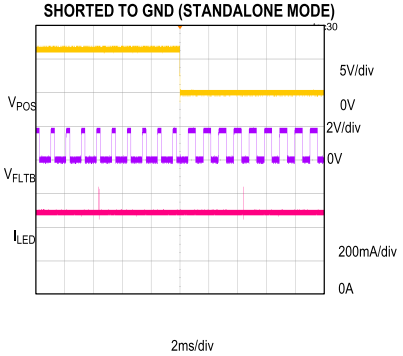
TFT FAULT
POS SHORTED TO GROUND
(STANDALONE MODE)



LED FAULT CREATED
BY SHORTING 3 LEDS IN STRING 1
(STANDALONE MODE)

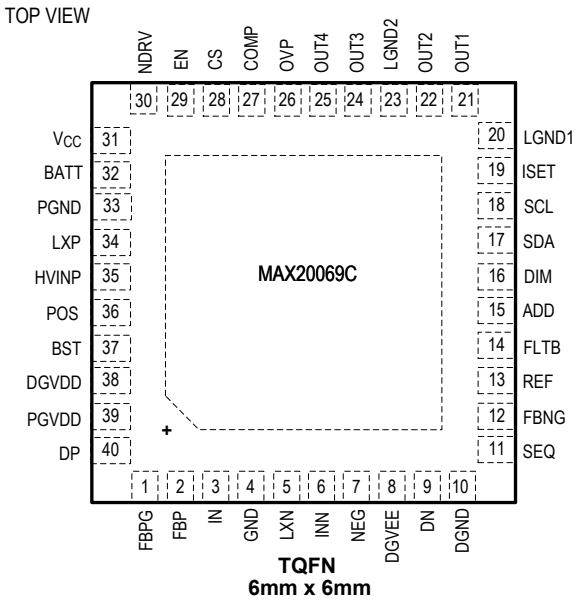


LED FAULT AND TFT FAULT
3 LEDS SHORTED IN STRING 1 AND POS
SHORTED TO GND (STANDALONE MODE)



Pin Configuration

MAX20069C



Pin Description

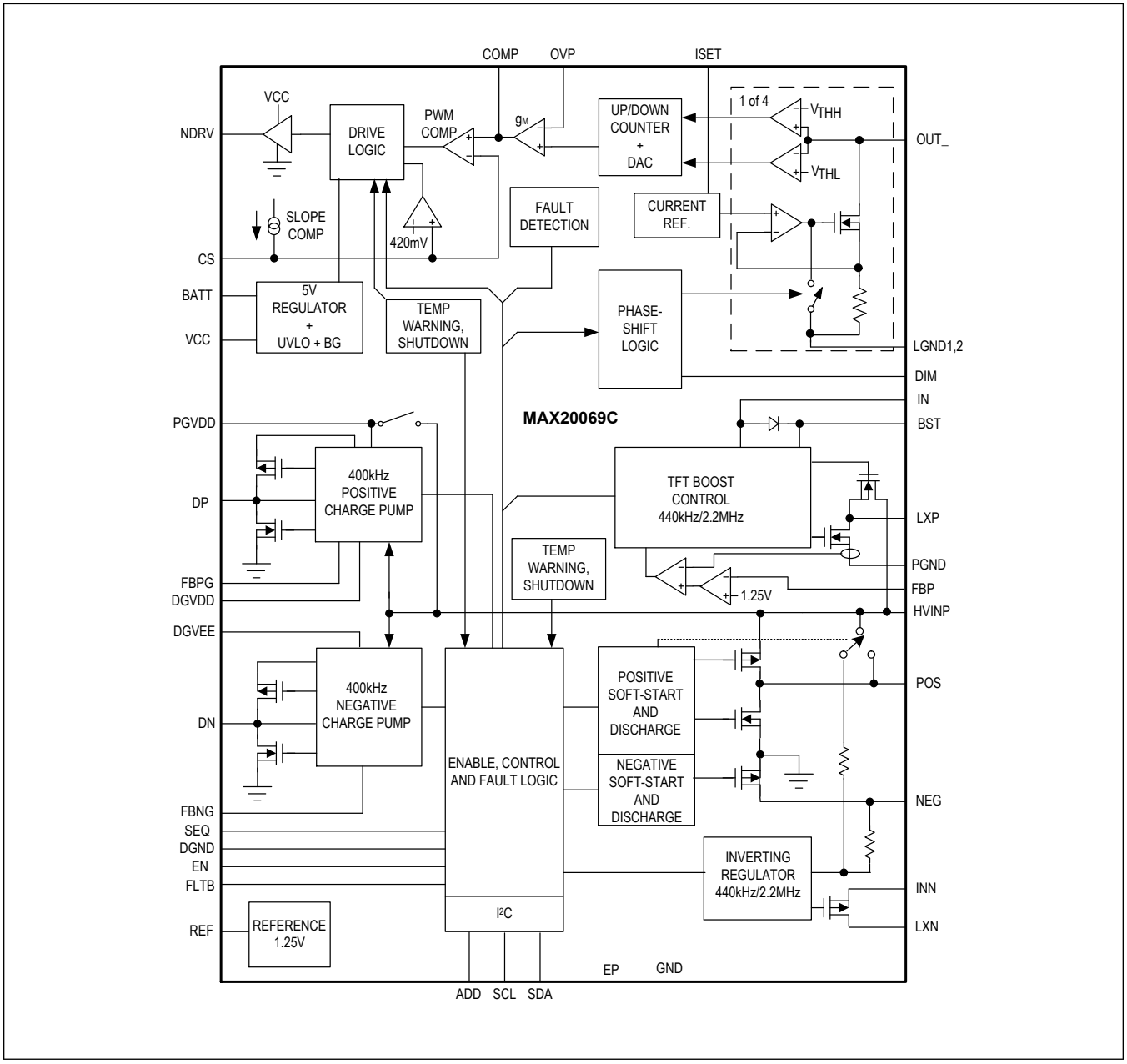
PIN	NAME	FUNCTION
1	FBPG	Feedback Input for DGVDD. In stand-alone mode, connect a resistor-divider between DGVDD and GND with its midpoint connected to the FBPG pin to set the DGVDD voltage. In I²C mode, connect FBPG to GND.
2	FBP	Feedback Input for HVINP. In stand-alone mode, connect a resistor-divider from the boost output to GND with its midpoint connected to the FBP pin to set the HVINP voltage. In I²C mode, connect FBP to GND.
3	IN	Supply Input. Connect a 1µF ceramic capacitor from IN to GND for proper operation.
4	GND	Ground Connection
5	LXN	DC-DC Inverting Converter Inductor/Diode Connection
6	INN	Buck-Boost Converter Input. Connect a 1µF ceramic capacitor from INN to GND for proper operation.
7	NEG	Negative Source-Driver Output Voltage
8	DGVEE	Connects directly to the negative charge-pump output to facilitate DGVEE discharge through an internal switch connected between DGVEE and GND. In I²C mode, DGVEE is the regulator feedback pin.
9	DN	Regulated Charge-Pump Driver for the Negative Charge Pump. Connect to the external flying capacitor.
10	DGND	Digital Ground
11	SEQ	Sequencing Programming Pin. In stand-alone mode, connect an appropriate resistor from SEQ to GND to program the desired sequence. When using I²C control, connect SEQ to IN (see the description). When SEQ is connected to IN, it is still possible to adjust the OUT_ output current through I²C and read the fault registers.
12	FBNG	Feedback Input for the Negative Charge Pump. In stand-alone mode, connect a resistor-divider from REF to DGVEE, with its midpoint connected to FBNG to set the DGVEE voltage. In I²C mode, connect FBNG to GND.
13	REF	1.25V Reference Output. Connect a 220nF ceramic capacitor from REF to GND.
14	FLTB	Active-Low Open-Drain Fault Indication Output. Connect an external pullup resistor from FLTB to an external supply lower than 5V.
15	ADD	I²C Address Select (see Table 2). In stand-alone mode, this pin is used to select the startup speed of the backlight boost converter. Connect to GND for the standard startup. Connect to IN to select accelerated startup with a final voltage of 1.1V on OVP.
16	DIM	PWM Dimming Input. DIM has an internal pullup to V_{CC}.
17	SDA	I²C Data I/O. Connect SDA to GND in stand-alone mode.
18	SCL	I²C Clock Input. Connect SCL to ground in stand-alone mode.
19	ISET	Full-Scale LED Current-Adjustment Pin. The resistance from ISET to GND controls the current in each LED string.
20	LGND1	Power-Ground Connection for OUT1 and OUT2
21	OUT1	LED String 1 Cathode Connection
22	OUT2	LED String 2 Cathode Connection. Connect OUT2 to ground using a 12kΩ resistor if not used.
23	LGND2	Power-Ground Connection for OUT3 and OUT4
24	OUT3	LED String 3 Cathode Connection. Connect OUT3 to ground using a 12kΩ resistor if not used.
25	OUT4	LED String 4 Cathode Connection. Connect OUT4 to ground using a 12kΩ resistor if not used.
26	OVP	LED Driver Output-Voltage-Sensing Input. This voltage is used for overvoltage and undervoltage protection.
27	COMP	LED Driver Switching-Converter Compensation Input. Connect an RC network from COMP to GND to compensate the backlight boost converter (see the *Feedback Compensation* section).

Pin Description (continued)

PIN	NAME	FUNCTION
28	CS	LED Driver Current-Sense Connection. Connect a sense resistor from the MOSFET source to PGND and a further resistor from the MOSFET source to the CS pin to set the slope compensation (see the *Current-Sense Resistor and Slope Compensation* section).
29	EN	Enable Input. When EN is high, the device is enabled in stand-alone mode. When using I2C control, connect EN to GND.
30	NDRV	Switching nMOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching-power MOSFET. Typically, a small resistor (1Ω to 22Ω) is inserted between the NDRV output and nMOSFET gate to decrease the slew rate of the gate driver and reduce the switching noise.
31	V_{CC}	5V Regulator Output. Place a 2.2µF ceramic capacitor as close as possible to V_{CC} and GND.
32	BATT	LED Driver Supply Input. Connect BATT to a 4.75V–40V supply. Bypass BATT to ground with a ceramic capacitor.
33	PGND	Power-Ground Connection
34	LXP	Boost HVINP Converter Switching-Node Connection. Connect LXP to the external inductor.
35	HVINP	Input Power for the POS Voltage Rail
36	POS	Positive Source-Driver Output Voltage
37	BST	Boost Converter High-Side Driver Power Supply. Connect a 0.1µF capacitor from BST to LXP.
38	DGVDD	DGVDD connects directly to the positive charge-pump output to facilitate DGVDD discharge through an internal switch connected between DGVDD and GND. In I2C mode, DGVDD is the regulator feedback pin. In stand-alone mode, DGVDD is used for the discharge function.
39	PGVDD	Switched Version of HVINP Voltage for the Positive Charge Pump. Provides soft-start control of the DGVDD output.
40	DP	Regulated Charge-Pump Driver for Positive Charge Pump. Connect to an external flying capacitor.
—	EP	Exposed Pad. Connect to a large contiguous copper-ground plane for optimal heat dissipation. Do not use EP as the only electrical ground connection.

Functional Diagrams

Detailed Block Diagram



Detailed Description

The MAX20069C is highly integrated TFT power supply and LED backlight driver IC for automotive TFT-LCD applications. The IC integrates one buck-boost converter, one boost converter, two gate-driver supplies, and a boost/SEPIC converter that can power one to four strings of LEDs in the display backlight.

The source-driver power supplies consist of a synchronous boost converter and an inverting buck-boost converter that can generate voltages up to +18V and down to -7V. The positive source-driver can deliver up to 120mA, while the negative source driver is capable of 100mA. The positive source-driver-supply regulation voltage (V_{POS}) is set by connecting an external resistor-divider on FBP or through I^2C. The negative source-driver-supply voltage (V_{NEG}) is always tightly regulated to $-V_{POS}$ (down to a minimum of -7V). The source-driver supplies operate from an input voltage between 2.8V and 5.5V.

The gate-driver-power supplies consist of regulated charge pumps that generate between +28V and -21.5V and can deliver up to 3mA each.

The IC features a quad-string LED driver that operates from a separate input voltage (BATT) and can power up to four strings of LEDs with 150mA (max) of current per string. The IC features logic-controlled pulse-width modulation (PWM) dimming, with minimum pulse widths as low as 500ns and the option of phase shifting the LED strings with respect to one another. When phase shifting is enabled, each string is turned on at a different time, reducing the input and output ripple, as well as audible noise. With phase shifting disabled, each current sink turns on at the same time and allows parallel connection of current sinks.

The startup and shutdown sequences for all power domains are controlled using one of the seven preset modes that are selectable through a resistor on SEQ. If the SEQ pin is connected to IN (I^2C control), any sequence can be controlled using the individual regulator-enable bits. When a regulator other than HVINP is enabled, the HVINP boost is automatically enabled (if not previously active). In this case, the second regulator is enabled when the soft-start of HVINP has completed.

TFT Power Section

Source-Driver Power Supplies

The source-driver power supplies consist of a boost converter with output switch and an inverting buck-boost converter that generates up to +18V (max) and down to -7V (min), respectively, and can deliver up to 120mA on the positive regulator and -100mA on the negative regulator. The positive source-driver power supply's regulation voltage (V_{POS}) can be set by the resistor-divider on FBP or through the I^2C interface.

The negative source-driver supply voltage (V_{NEG}) is automatically tightly regulated to $-V_{POS}$. V_{NEG} cannot be adjusted independently of V_{POS}. In I^2C mode, V_{POS} (and V_{NEG}) is set by writing to the appropriate register. When HVINP is set to a voltage greater than 7V in I^2C mode, the NEG converter should be disabled to avoid damage to the device. If the NEG output is not needed, the external components can be omitted and INN should be connected to IN; LXN should be left open and NEG should be connected to GND.

Gate-Driver Power Supplies

The positive gate-driver power supply (DGVDD) generates +28V (max) and the negative gate-driver power supply (DGVEE) generates -21.5V (min). Both can supply up to 3mA output current. The DGVDD and DGVEE regulation voltages are set independently using external resistor networks or through the I^2C interface.

Fault Protection

The IC has robust fault and overload protection. In stand-alone mode, if any of the DGVEE, NEG, POS, or DGVDD outputs fall to less than 80% (typ) of their intended regulation voltage for more than 50ms (typ), or if a short-circuit condition occurs on any output for any duration, then all outputs latch off (at the same time without any power-down sequence) and a fault condition is set. In I^2C mode, only the output at fault is automatically disabled.

In stand-alone mode, the fault condition is cleared when the EN pin or IN supply are cycled. In I^2C mode, the fault condition is cleared when the EN bit of the affected rail is set to 0 or the IN supply is cycled.

Both sections (TFT and WLED) have thermal-fault detection; only the section causing the thermal overload is turned off.

Thermal faults are cleared when the die temperature drops by 15°C.

When a fault is detected, FLTB goes low in I²C mode, while in stand-alone mode the FLTB output pulses at a duty cycle that indicates the source of the fault.

Output Sequencing Control

The IC's source-driver and gate-driver outputs (DGVEE, NEG, POS, and DGVDD) can be controlled by the resistor value on the SEQ pin (stand-alone mode), or by the I²C interface if SEQ is connected to IN (I²C mode). In I²C mode, the EN pin does not have any function; the IC is turned on once one of the rails is activated by the appropriate I²C command, and the sequence is controlled by the I²C commands.

All outputs are brought up with soft-start control to limit the inrush current.

In stand-alone mode, toggling the EN pin from low to high initiates an adjustable preset power-up sequence (see Table 1). Toggling the EN pin from high to low initiates an adjustable preset power-down sequence. The EN pin has an internal deglitching filter of 7µs (typ).

Note that a glitch in the EN signal with a period of less than 7µs is ignored by the internal enable circuitry. After all the TFT outputs have exceeded their power-good levels, the backlight block is turned on.

Table 1. Sequencing Options

SEQ PIN RESISTOR (kΩ ±1%)	POWER-ON SUPPLY SEQUENCING (t_1–t_4* IS TIME FROM THE EXPIRATION OF SOFT-START PERIOD)				POWER-OFF SEQUENCING (REVERSE ORDER OF POWER-UP) (t_5–t_8 IS TIME FROM THE INSTANT WHEN EN IS DRIVEN LOW)			
	1st AFTER t_1 (ms)	2nd AFTER t_2 (ms)	3rd AFTER t_3 (ms)	4th AFTER t_4 (ms)	1st AFTER t_5 (ms)	2nd AFTER t_6 (ms)	3rd AFTER t_7 (ms)	4th AFTER t_8 (ms)
10	POS	NEG	DGVEE	DGVDD	DGVDD	DGVEE	NEG	POS
30	POS	NEG	DGVDD	DGVEE	DGVEE	DGVDD	NEG	POS
51	NEG	POS	DGVEE	DGVDD	DGVDD	DGVEE	POS	NEG
68	POS	DGVEE	DGVDD	No NEG output	DGVDD	DGVEE	POS	No NEG output
91	POS	DGVDD	DGVEE	No NEG output	DGVEE	DGVDD	POS	No NEG output
110	POS NEG	—	—	DGVDD DGVEE	DGVDD DGVEE	—	—	POS NEG
150	DGVEE	DGVDD	NEG	POS	POS	NEG	DGVDD	DGVEE

*$t_1 = t_5$ = 15ms

$t_2 = t_6$ = 30ms

$t_3 = t_7$ = 45ms

$t_4 = t_8$ = 60ms

TFT Sequence with RSEQ = 10k

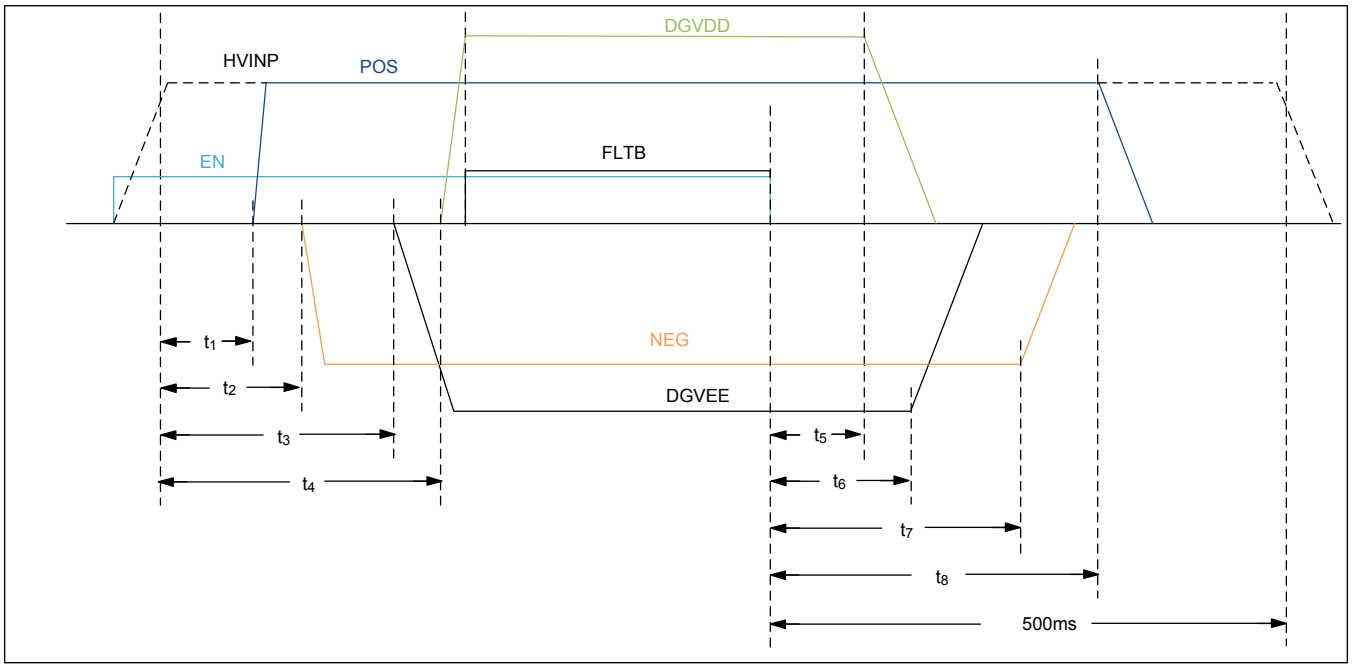


Figure 1. TFT Sequence with R_{SEQ} = 10kΩ

Description of the LED Driver Section

The IC also includes a high-efficiency, high-brightness LED driver that integrates all the necessary features to implement a high-performance backlight driver to power LEDs in medium-to-large-sized displays for automotive and general applications. The IC provides load-dump voltage protection up to 52V in automotive applications and incorporates two major blocks: a DC-DC controller with peak current-mode control to implement a boost, or a SEPIC-type switched-mode power supply and a 4-channel LED driver with 20mA to 150mA constant-current-sink capability per channel.

The IC features constant-frequency, peak current-mode control with programmable slope compensation to control the duty cycle of the PWM controller. The DC-DC converter implemented using the controller generates the required supply voltage for the LED strings from a wide input-supply range. Connect LED strings from the DC-DC converter output to the 4-channel constant-current-sink drivers (OUT1–OUT4) to control the current through the LED strings. A single resistor connected from the ISET input to ground adjusts the forward current through all four LED strings. Fine adjustment can be made to the LED current using the I2C interface, even in stand-alone mode.

The IC features adaptive voltage control that adjusts the converter output voltage depending on the forward voltage of the LED strings. This feature minimizes the voltage drop across the constant-current-sink drivers and reduces power dissipation in the device. The backlight boost and current sinks are enabled when the complete sequence of the TFT bias section is completed.

The IC provides a very wide (10,000:1) PWM dimming range at 200Hz dimming frequency (with a dimming pulse as narrow as 500ns possible). The internal dimming signal is derived from the DIM signal or from the phase-shift dimming logic. Phase shifting of the LED strings can be disabled in I2C mode by writing to the psen bit in the enable (0x02) register.

Other advanced features include detection and string disconnect for open-LED strings, partially or fully shorted strings, and unused strings. Overvoltage protection clamps the converter output voltage to the programmed OVP threshold in the event of an open-LED condition.

The shorted-LED string threshold is programmable using the led_short_th[1:0] bits in the cnfg_gen (0x01 register (in

stand-alone mode, the threshold is fixed at 7.8V).

In I2C mode, the FLTB signal asserts low to indicate open-LED, shorted-LED, and overtemperature conditions if they are not masked. In stand-alone mode, a fault in the backlight section causes FLTB to pulse at 25% duty cycle. Disable individual current-sink channels by connecting the corresponding OUT_ to LGND_ through a 12kΩ resistor (starting with OUT4). In this case, FLTB will not indicate an open-LED condition for the disabled channel. The IC also features overtemperature warning and protection that shuts down the controller if the die temperature exceeds +160°C.

Current-Mode DC-DC Controller

The IC backlight boost is a constant-frequency, current-mode controller designed to drive the LEDs in a boost or SEPIC configuration. The IC features multiloop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks to minimize power dissipation.

The default switching frequency is 2.2MHz but this can be reduced to 440kHz by setting the bl_swfreq bit in the cnfg_gen (0x01) register. Programmable slope compensation is used to avoid subharmonic oscillation that can occur at > 50% duty cycles in continuous-conduction mode.

The external nMOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (R_{CS}) connected from the source of the external nMOSFET to PGND.

The IC features leading-edge blanking to suppress the external nMOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the external nMOSFET when the voltage at CS exceeds the error amplifier's output voltage (at the COMP pin). This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the IC has two other feedback loops for control. The converter output voltage is sensed through the OVP input, which goes to the inverting input of the error amplifier.

The OVP gain (A_{OVP}) is defined as V_{OUT}/V_{OVP}, or (R17 + R16)/R16. The other feedback comes from the OUT_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation, while still ensuring accurate LED current matching. Each current sink has a window comparator with a low threshold of 0.68V and a high threshold of 0.93V. These comparators drive logic that controls an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives an 8-bit digital-to-analog converter (DAC), which sets the reference to the error amplifier.

8-Bit DAC

The error amplifier's reference input is controlled with an 8-bit DAC. The DAC output is ramped up during startup to implement a soft-start function (see the *Startup Sequence* section). During normal operation, the DAC output range is limited to between 0.6V and 1.25V. The DAC LSB determines the minimum output-voltage step according to the following equation.

Equation 1:

$$V_{STEP_MIN} = V_{DAC_LSB} \times A_{OVP}$$

where V_{STEP_MIN} is the minimum output-voltage step, V_{DAC_LSB} is 2.5mV (typ), and A_{OVP} is the OVP resistor-divider gain.

PWM Dimming

The DIM input accepts a pulse-width modulation (PWM) signal to control the luminous intensity of the LEDs and modulate the pulse width of the LED current. This allows for changing the brightness of the LEDs without the color temperature shift that sometimes occurs with analog dimming. The DIM input detects the dimming frequency based on the first two pulses applied to the DIM input after EN goes high. The dimming frequency cannot be changed during normal operation. If a change of dimming frequency is desired, disable the backlight block, change the DIM frequency, and then re-enable the backlight block. The DIM signal can be applied before or after the device is enabled, but must power on smoothly (no high-frequency pulses). If the DIM signal turn-on is inconsistent, the DIM signal should be applied first; once the DIM signal is stable, the backlight block can be enabled. In normal dimming mode, if at least one of the LED current sinks is turned on, the boost converter switches. If none of the current sinks are on (each current-sink DIM signal is low), the boost converter stops switching, and the COMP node is disconnected from the error amplifier until one of the LED current

sinks is turned on again.

Low-Dim Mode

The IC's operation mode changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. The IC checks the pulse width of the signal being applied to the DIM input, and if the dimming on-time is lower than 25µs (typ) for the 2.2MHz switching frequency (f_{SW}), the IC enters low-dim mode. In this state, the converter switches continuously and the LED short detection is disabled. When the DIM input is greater than 26µs (typ) for 2.2MHz, the IC goes back into normal dim mode, enabling the short-LED detection and switching the power FET only when the DIM signal is high. When the switching frequency is set to 440kHz the low-dim thresholds become 50µs and 51µs.

Phase Shifting

The IC offers phase shifting of the LED strings. To achieve this, the DIM signal is sampled internally by a 10MHz clock.

When phase shifting is enabled, the sampled DIM input is used to generate separate dimming signals for each LED string that is shifted in phase. The resolution with which the DIM signal is captured degrades at higher DIM input frequencies; therefore, dimming frequencies between 100Hz and 3kHz are recommended, although higher dimming frequencies are technically possible. The phase shift between strings is determined by the following equation.

Equation 2:

$$\Theta = \frac{360}{n}$$

where n is the total number of strings being used and θ is the phase shift in degrees. The order of the sequence is fixed, with OUT1 as the first in the sequence and OUT4 as the last. See Figure 2 for a timing diagram example with phase shifting enabled.

The phase-shifting feature is enabled or disabled with the psen bit. In stand-alone mode (no I2C), the psen bit in register 0x02 is set high by default (phase shifting enabled). When phase shifting is disabled, all strings turn on/off at the same time. If multiple current sinks are being connected in parallel to achieve greater than 150mA per string, phase shifting should be disabled.

If a fault is detected, resulting in a string being disabled during normal operation, the phase shifting does not adjust. For example, if all four strings are used, each string is 90° out-of-phase. If the 4th string is disabled due to a fault, there will still be 90° phase difference between each string.

When disabling unused strings, disable the higher-numbered OUT_ current sinks first.

Figure 2 Phase-Shifted Outputs

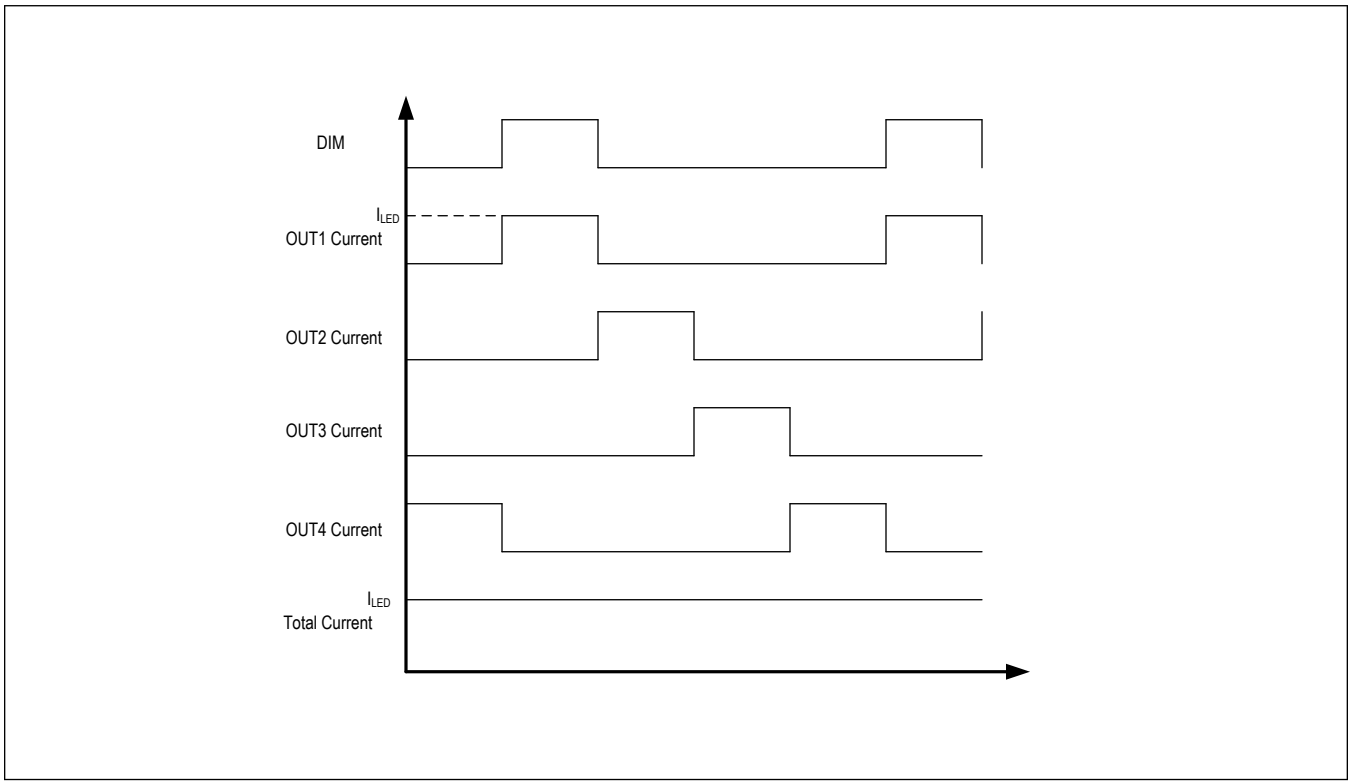


Figure 2. Phase-Shifted Outputs

Undervoltage Lockout

The WLED section features two UVLOs that monitor the input voltage at BATT and the output of the internal LDO regulator at V_{CC}. The backlight boost is active only when both BATT and V_{CC} exceed their respective UVLO thresholds.

Startup Sequence

The WLED section startup sequence occurs in two stages, as described in the Stage 1 and Stage 2 sections. The overall startup time can be selected as either slow or fast using the ADD pin in stand-alone mode or the wled_ss_time bit in the fault_masks1 (0x0B) register when using the I2C interface. The final boost output voltage differs between the slow and fast startup modes: when the slow-startup mode is selected, the final voltage on the OVP pin is 0.6V, while in the fast mode and the final voltage on OVP is 1.1V.

Stage 1

Assuming the BATT input is above its UVLO and the TFT has completed the startup sequence, the V_{CC} regulator begins to charge up its output capacitor. Once the V_{CC} regulator output rises above the V_{CC} UVLO threshold, the IC goes through its power-up checks, including unused string detection and OUT_ short-to-ground detection. To avoid possible damage, the converter does not start if any OUT_ is detected as shorted to ground.

Any current sinks detected as unused are disabled to prevent a false fault-flag assertion during normal operation. After these checks have been performed, the converter begins to operate and the output voltage begins to ramp up. The DAC reference to the error amplifier is stepped upwards until the OVP pin reaches 0.6V (or 1.1V in fast startup mode).

This stage duration is fixed at approximately 50ms (22ms in fast startup mode).

Stage 2

The second stage begins once the first stage is complete and the DIM input goes high. During Stage 2, the output of the converter is adjusted until the minimum OUT_ voltage falls within the window comparator limits of 0.68V (typ) and 0.93V (typ). The output ramp is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input. If the DIM input is a 100% duty cycle (DIM = high), then the DAC output is updated once every 10ms.

The total soft-start time can be calculated using the following equation in slow-startup mode.

Equation 3:

$$t_{SS} = 50ms + \frac{V_{LED} + 0.81 - \left(0.6 \times A_{OVP}\right)}{f_{DIM} \times 0.01 \times A_{OVP}}$$

where t_{SS} is the total soft-start time, 50ms is the fixed Stage 1 duration, V_{LED} is the total forward voltage of the LED strings, 0.81V is midpoint of the window comparator, A_{OVP} is the gain of the OVP resistor-divider, f_{DIM} is the dimming frequency (use 100Hz if the DIM input duty cycle is 100%), and 0.01V is the maximum voltage step per clock cycle of the DAC.

In fast-startup mode (with ADD connected to IN or the wled_ss_time bit in the fault_masks1 (0x0B) register set to 1), the following equation should be used.

Equation 4:

$$t_{SS} = 22ms + \frac{1.1 \times A_{OVP} - (V_{LED} + 0.81)}{f_{DIM} \times 0.01 \times A_{OVP}}$$

Open-LED Management and Overvoltage Protection (OVP)

On power-up, the IC detects and disconnects any unused current-sink channels before entering the DC-DC converter soft-start. Disable the unused current-sink channels by connecting the corresponding OUT_ to LGND_ through a 12kΩ resistor. This avoids asserting the FLTB output for the unused channels. After soft-start, the IC detects open strings and disconnects them from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency.

If any LED string is open, the voltage at the open OUT_ goes to GND. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, OVP input, and GND (the threshold at which the PWM controller is switched off, holding NDRV low). At that point, any current-sink output with $V_{OUT_}$ < 300mV (typ) is disconnected from the minimum-voltage detector. Select V_{OUT_OVP} (which will be the maximum voltage that the boost converter can produce) according to the following equation.

Equation 5:

$$V_{OUT_OVP} > 1.1 \times (V_{LED_MAX} + 1)$$

where V_{LED_MAX} is the maximum expected LED string voltage. V_{OUT_OVP} should also be chosen such that the voltage at the OUT_ pins does not exceed the absolute maximum rating.

The upper resistor in the OVP resistor-divider (R17) can be selected using the following formula.

Equation 6:

$$R17 = R16 \times \left(\frac{V_{OUT_OVP}}{1.23} - 1\right)$$

where 1.23V is the typical OVP threshold. Ensure that the minimum voltage on the OVP pin is always greater than 0.6V to avoid the boost converter latching off due to undervoltage by checking the following.

Equation 7:

$$(V_{LED_MIN} + 0.6) \times \frac{R16}{R16 + R17} > 0.6V$$

where V_{LED_MIN} is the worst-case minimum LED string voltage.

When an open-LED condition occurs, FLTB is asserted low in I2C mode or switches at 25% in stand-alone mode.

For boost-circuit applications, the OVP resistor-divider always dissipates power from the battery, through the inductor and switching diode. If ultra-low shutdown current is needed in stand-alone mode, a general-purpose MOSFET can be added between the bottom OVP resistor and ground, with the EN of the device controlling the gate of the MOSFET. This additional MOSFET disconnects the OVP resistor-divider path when the device is disabled.

Short-LED Detection

The IC checks for shorted LEDs at each rising edge of DIM. An LED short is detected at OUT_ if the OUT_ voltage is greater than the value programmed using the led_short_th bits in register 0x01 (or 7.8V in stand-alone mode). Once a short is detected on any of the strings, the LED strings with the short are disconnected and the FLTB output flag asserts (unless the fault is masked) until the device detects that the shorts are removed on any of the following rising edges of DIM. Short-LED detection is disabled in low-dimming mode. If the DIM input is connected high, short-LED detection is performed continuously.

Short-LED detection is also disabled in cases where all active OUT_ channels rise above 2.8V (typ). This can occur in a boost-converter application when the input voltage becomes higher than the total LED string voltage drop, such as during a battery load dump. If a short-LED fault occurs during a load dump, the fault flag does not assert until the load dump is over and the minimum OUT_ voltage has fallen below 2.8V. If a load dump occurs after a short LED is detected, the fault flag deasserts until the load dump is over and the minimum OUT_ voltage has fallen below 2.8V, at which point, the fault flag reasserts.

LED Current Control

The IC features four identical constant-current sources used to drive multiple high-brightness LED strings. The current through each one of the four channels is adjustable between 20mA and 150mA using an external resistor (R_{ISET}) connected between ISET and GND.

Select R_{ISET} using the formula below.

Equation 8:

$$R_{ISET} = \frac{1500}{I_{OUT_}}$$

where $I_{OUT_}$ is the desired output current for each of the four channels. All four channels can be paralleled together for string currents exceeding 150mA. When I2C control is used, the current in the strings can be reduced in steps by writing to the diout (0x06) register. The resolution of this setting is 0.5% of the value set by the resistor on ISET.

FLTB Output

The FLTB output pin is an active-low, open-drain output that can be used to signal various device faults (for operation in stand-alone mode (see the *Stand-Alone Mode* section). When the I2C interface is used, the FLTB output can flag any or all of the following conditions:

- Open fault on any of the OUT_ pins
- Shorted-LED fault on any of the OUT_ pins
- Any OUT_ shorted to GND
- LED boost converter undervoltage or overvoltage
- Undervoltage on HVINP, POS, NEG, DGVDD, or DGVEE
- Thermal warning on LED drive section
- Thermal shutdown on either LED drive or TFT bias section

The above conditions can be masked from causing FLTB to go low by using the corresponding mask bit in the bl_fault_masks (0x0A), fault_masks1 (0x0B), and fault_masks2 (0x0C) registers, if available.

In standalone mode, the duty.cycle output on the FLTB pin indicates the type of fault according to the following scheme:

- FLTB continuously low: Thermal-shutdown fault
- 25% duty cycle on FLTB: Fault in LED section
- 50% duty cycle on FLTB: Fault in TFT section
- 75% duty cycle on FLTB: Faults in both LED and TFT sections

Serial Interface

The MAX20069C IC features an I2C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 1MHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus.

The Slave ID of the MAX20069C depends on the connection of the ADD pin and the selected device version (see Table 2).

Table 2. I2C Addresses

ADD PIN CONNECTION	DEVICE VERSION	DEVICE ADDRESS							WRITE ADDRESS	READ ADDRESS	NOTES
		A6	A5	A4	A3	A2	A1	A0			
GND	MAX20069CGTL	1	1	0	0	0	0	0	0xC0	0xC1	
IN	MAX20069CGTL	1	1	0	0	1	0	0	0xC8	0xC9	
GND	MAX20069CGTLA	0	1	0	0	0	0	0	0x40	0x41	Future device, contact factory
IN	MAX20069CGTLA	0	1	0	0	1	0	0	0x48	0x49	Future device, contact factory

A master device communicates with the MAX20069C by transmitting the correct Slave ID followed by the register address and data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition, and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The IC's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus. In general, the resistor has to be selected as a function of bus capacitance such that the rise time on the bus is not greater than 120ns. The IC's SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. In general, for the SCL-line resistor selection, the same SDA recommendations apply. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

Register Map

Reg Map

Register Map of the AP74

ADDRESS	NAME	MSB							LSB
bank 0									
0x00	nop[7:0]	rev_id[3:0]				dev_id[3:0]			
0x01	cnfg_gen[7:0]	lxp_lim_low	neg_lim_low	led_short_th[1:0]		bl_swfreq	ssoff_bl	swfreq_tft	ssoff_tft
0x02	enable[7:0]	–	enbst	enpos	enneg	engvdd	engvee	enblight	psen
0x03	vpos_set[7:0]	vpos[7:0]							
0x04	dgvdd_set[7:0]	–	–	dgvdd[5:0]					
0x05	dgvee_set[7:0]	–	–	–	dgvee[4:0]				
0x06	diout[7:0]	–	diout[6:0]						
0x07	bl_fault[7:0]	led_open[3:0]				led_short[3:0]			
0x08	fault[7:0]	boostuv	boostov	led_shortgnd	hvinpuv	pos_ol	neguv	dgvdduv	dgveeuv
0x09	dev_status[7:0]	–	–	–	–	hw_rst	wled_th_shdn	wled_th_warn	tft_th_shdn
0x0A	bl_fault_masks[7:0]	led_open_mask[3:0]				led_short_mask[3:0]			
0x0B	fault_masks1[7:0]	boostuv_mask	boostov_mask	led_shortgnd_mask	hvinpuv_mask	wled_ss_time	neguv_mask	dgvdduv_mask	dgveeuv_mask
0x0C	fault_masks2[7:0]	–	–	–	–	–	–	wled_th_warn_mask	–

Register Details

nop (0x00)

Device identification register

BIT	7	6	5	4	3	2	1	0
Field	rev_id[3:0]				dev_id[3:0]			
Reset	0x4				0x9			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
rev_id	7:4	Revision ID.	0000: Revision ID
dev_id	3:0	Device identification.	1001: Device ID for the device

cnfg_gen (0x01)

Configuration register

BIT	7	6	5	4	3	2	1	0
Field	lxp_lim_low	neg_lim_low	led_short_th[1:0]		bl_swfreq	ssoff_bl	swfreq_tft	ssoff_tft
Reset	0b0	0b0	0x3		0b0	0b0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
lxp_lim_low	7	When set to 1, the LXP switch current limit is reduced.	
neg_lim_low	6	When set to 1, the NEG switch current limit is reduced.	
led_short_th	5:4	LED fault-detection threshold.	00: Fault disabled 01: Fault threshold is 3V 10: Fault threshold is 6V 11: Fault threshold is 7.8V
bl_swfreq	3	Sets backlight boost switching frequency. Default value is 2.2MHz.	0: 2.2MHz 1: 440kHz
ssoff_bl	2	When 1, spread-spectrum modulation is disabled on the backlight boost; when 0, spread spectrum is enabled.	0: SS enabled 1: SS disabled
swfreq_tft	1	Sets TFT section switching frequency (note that the charge-pump operating frequency is always 400kHz). Default value is 2.2MHz.	0: 2.2MHz 1: 420kHz
ssoff_tft	0	When 1, spread-spectrum modulation is disabled on the TFT section; when 0, spread spectrum is enabled.	0: Enabled 1: Disabled

enable (0x02)

Block enables register

BIT	7	6	5	4	3	2	1	0
Field	–	enbst	enpos	enneg	engvdd	engvee	enblight	psen
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
enbst	6	Boost converter enable bit.	0: Disabled 1: Enabled
enpos	5	POS output enable bit. When POS is enabled, the HVINP boost converter is automatically enabled if not already active.	0: Disabled 1: Enabled
enneg	4	NEG converter enabled bit. When NEG is enabled, the HVINP boost converter is automatically enabled if not already active.	0: Disable 1: Enable
engvdd	3	DGVDD regulator enable bit. When DGVDD is enabled, the HVINP boost converter is automatically enabled if not already active.	0: Disabled 1: Enabled
engvee	2	DGVEE regulator enable bit. When DGVEE is enabled, the HVINP boost converter is automatically enabled if not already active.	0: Disabled 1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
enblight	1	Backlight boost converter and current sinks enable bit. If 1, they are enabled when the TFT section has completed soft-start.	0: Disabled 1: Enabled
psen	0	LED string phase-shift enable. When 0, phase shifting between the strings is disabled. Read only at backlight startup; thereafter, this bit has no effect.	0: Direct dimming 1: Phase shift

vpos_set (0x03)

BIT	7	6	5	4	3	2	1	0
Field	vpos[7:0]							
Reset	0x14							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
vpos	7:0	Sets POS output voltage.	0xA: 5 0xB: 5.1 0xC: 5.2 0xD: 5.3 0xE: 5.4 0xF: 5.5 0x10: 5.6 0x11: 5.7 0x12: 5.8 0x13: 5.9 0x14: 6 0x15: 6.1 0x16: 6.2 0x17: 6.3 0x18: 6.4 0x19: 6.5 0x1A: 6.6 0x1B: 6.7 0x1C: 6.8 0x1D: 6.9 0x1E: 7 0x1F: 7.1 0x20: 7.2 0x21: 7.3 0x22: 7.4 0x23: 7.5 0x24: 7.6 0x25: 7.7 0x26: 7.8 0x27: 7.9 0x28: 8 0x29: 8.1 0x2A: 8.2 0x2B: 8.3 0x2C: 8.4 0x2D: 8.5 0x2E: 8.6 0x2F: 8.7 0x30: 8.8 0x31: 8.9 0x32: 9 0x33: 9.1 0x34: 9.2 0x35: 9.3 0x36: 9.4 0x37: 9.5 0x38: 9.6 0x39: 9.7 0x3A: 9.8 0x3B: 9.9 0x3C: 10 0x3D: 10.1 0x3E: 10.2 0x3F: 10.3 0x40: 10.4 0x41: 10.5 0x42: 10.6 0x43: 10.7 0x44: 10.8

BITFIELD	BITS	DESCRIPTION	DECODE
			0x45: 10.9 0x46: 11 0x47: 11.1 0x48: 11.2 0x49: 11.3 0x4A: 11.4 0x4B: 11.5 0x4C: 11.6 0x4D: 11.7 0x4E: 11.8 0x4F: 11.9 0x50: 12 0x51: 12.1 0x52: 12.2 0x53: 12.3 0x54: 12.4 0x55: 12.5 0x56: 12.6 0x57: 12.7 0x58: 12.8 0x59: 12.9 0x5A: 13 0x5B: 13.1 0x5C: 13.2 0x5D: 13.3 0x5E: 13.4 0x5F: 13.5 0x60: 13.6 0x61: 13.7 0x62: 13.8 0x63: 13.9 0x64: 14 0x65: 14.1 0x66: 14.2 0x67: 14.3 0x68: 14.4 0x69: 14.5 0x6A: 14.6 0x6B: 14.7 0x6C: 14.8 0x6D: 14.9 0x6E: 15 0x6F: 15.1 0x70: 15.2 0x71: 15.3 0x72: 15.4 0x73: 15.5 0x74: 15.6 0x75: 15.7 0x76: 15.8 0x77: 15.9 0x78: 16 0x79: 16.1 0x7A: 16.2 0x7B: 16.3 0x7C: 16.4 0x7D: 16.5 0x7E: 16.6 0x7F: 16.7

BITFIELD	BITS	DESCRIPTION	DECODE
			0x80: 16.8 0x81: 16.9 0x82: 17 0x83: 17.1 0x84: 17.2 0x85: 17.3 0x86: 17.4 0x87: 17.5 0x88: 17.6 0x89: 17.7 0x8A: 17.8 0x8B: 17.9 0x8C: 18 0x8D-0xFF: 18

dgvdd_set (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	dgvdd[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
dgvdd	5:0	Sets DGVDD output voltage.	0x0: 8 0x1: 8.5 0x2: 9 0x3: 9.5 0x4: 10 0x5: 10.5 0x6: 11 0x7: 11.5 0x8: 12 0x9: 12.5 0xA: 13 0xB: 13.5 0xC: 14 0xD: 14.5 0xE: 15 0xF: 15.5 0x10: 16 0x11: 16.5 0x12: 17 0x13: 17.5 0x14: 18 0x15: 18.5 0x16: 19 0x17: 19.5 0x18: 20 0x19: 20.5 0x1A: 21 0x1B: 21.5 0x1C: 22 0x1D: 22.5 0x1E: 23 0x1F: 23.5 0x20: 24 0x21: 24.5 0x22: 25 0x23: 25.5 0x24: 26 0x25: 26.5 0x26: 27 0x27: 27.5 0x28: 28 0x29- 0x3F: Unused

dgvee_set (0x05)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	dgvee[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
dgvee	4:0	Sets DGVEE output voltage.	0x0: -6 0x1: -6.5 0x2: -7 0x3: -7.5 0x4: -8 0x5: -8.5 0x6: -9 0x7: -9.5 0x8: -10 0x9: -10.5 0xA: -11 0xB: -11.5 0xC: -12 0xD: -12.5 0xE: -13 0xF: -13.5 0x10: -14 0x11: -14.5 0x12: -15 0x13: -15.5 0x14: -16 0x15: -16.5 0x16: -17 0x17: -17.5 0x18: -18 0x19: -18.5 0x1A: -19 0x1B: -19.5 0x1C: -20 0x1D: -20.5 0x1E: -21 0x1F: -21.5

diout (0x06)

BIT	7	6	5	4	3	2	1	0
Field	–	diout[6:0]						
Reset	–	0x7F						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
diout	6:0	The value in this register sets the percentage of LED current, with respect to the value dictated by the resistor on the ISET pin.	0x0: 36.5 0x1: 37 0x2: 37.5 0x3: 38 0x4: 38.5 0x5: 39 0x6: 39.5 0x7: 40 0x8: 40.5 0x9: 41 0xA: 41.5 0xB: 42 0xC: 42.5 0xD: 43 0xE: 43.5 0xF: 44 0x10: 44.5 0x11: 45 0x12: 45.5 0x13: 46 0x14: 46.5 0x15: 47 0x16: 47.5 0x17: 48 0x18: 48.5 0x19: 49 0x1A: 49.5 0x1B: 50 0x1C: 50.5 0x1D: 51 0x1E: 51.5 0x1F: 52 0x20: 52.5 0x21: 53 0x22: 53.5 0x23: 54 0x24: 54.5 0x25: 55 0x26: 55.5 0x27: 56 0x28: 56.5 0x29: 57 0x2A: 57.5 0x2B: 58 0x2C: 58.5 0x2D: 59 0x2E: 59.5 0x2F: 60 0x30: 60.5 0x31: 61 0x32: 61.5 0x33: 62 0x34: 62.5 0x35: 63 0x36: 63.5 0x37: 64 0x38: 64.5 0x39: 65 0x3A: 65.5

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3B: 66 0x3C: 66.5 0x3D: 67 0x3E: 67.5 0x3F: 68 0x40: 68.5 0x41: 69 0x42: 69.5 0x43: 70 0x44: 70.5 0x45: 71 0x46: 71.5 0x47: 72 0x48: 72.5 0x49: 73 0x4A: 73.5 0x4B: 74 0x4C: 74.5 0x4D: 75 0x4E: 75.5 0x4F: 76 0x50: 76.5 0x51: 77 0x52: 77.5 0x53: 78 0x54: 78.5 0x55: 79 0x56: 79.5 0x57: 80 0x58: 80.5 0x59: 81 0x5A: 81.5 0x5B: 82 0x5C: 82.5 0x5D: 83 0x5E: 83.5 0x5F: 84 0x60: 84.5 0x61: 85 0x62: 85.5 0x63: 86 0x64: 86.5 0x65: 87 0x66: 87.5 0x67: 88 0x68: 88.5 0x69: 89 0x6A: 89.5 0x6B: 90 0x6C: 90.5 0x6D: 91 0x6E: 91.5 0x6F: 92 0x70: 92.5 0x71: 93 0x72: 93.5 0x73: 94 0x74: 94.5 0x75: 95

BITFIELD	BITS	DESCRIPTION	DECODE
			0x76: 95.5 0x77: 96 0x78: 96.5 0x79: 97 0x7A: 97.5 0x7B: 98 0x7C: 98.5 0x7D: 99 0x7E: 99.5 0x7F: 100

bl_fault (0x07)

Backlight LED string faults

BIT	7	6	5	4	3	2	1	0
Field	led_open[3:0]				led_short[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
led_open	7:4	Each bit of this field corresponds to a string. If a bit is set to 1, then an open fault has been detected on the corresponding string and the string was disabled.	0: Corresponding string is not open 1: Corresponding string is open or the string is unused or shorted to GND.
led_short	3:0	Each bit of this field corresponds to a string. If a bit is set to 1, then one or more LEDs in that string are shorted. This bit is updated at the beginning of each DIM cycle.	0: Corresponding string has no LED shorted 1: Corresponding string has one or more LEDs shorted

fault (0x08)

TFT fault register

BIT	7	6	5	4	3	2	1	0
Field	boostuv	boostov	led_shortgnd	hvinpuv	pos_ol	neguv	dgvdduv	dgveeuv
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
boostuv	7	Backlight boost undervoltage status/flag. When an undervoltage is detected, the boost is disabled.	0: Not detected so far 1: Event detected
boostov	6	Backlight boost overvoltage status flag. When the overvoltage level is reached, switching stops but the converter is not disabled.	0: Not detected so far 1: Event detected
led_shortgnd	5	LED string shorted to GND status flag. When this bit is detected, the converter does not start and the condition is latched.	0: No LED strings shorted to GND 1: One or more LED strings shorted to GND

BITFIELD	BITS	DESCRIPTION	DECODE
hvinpuv	4	Undervoltage on FBP (external feedback) or POS (internal feedback). Set immediately if an undervoltage is detected. If the undervoltage persists for 50ms, the output is turned off.	0: No undervoltage detected so far 1: Undervoltage detected
pos_ol	3	When 1, signals an overload or overcurrent fault on the POS output.	0: No error detected so far 1: Error detected
neguv	2	NEG output undervoltage status flag. Set immediately when an undervoltage is detected. If the condition persists for 50ms, the output is turned off.	0: No undervoltage detected 1: Undervoltage detected
dgvdduv	1	DGVDD undervoltage status flag. This bit is set immediately when an undervoltage is detected. If the condition persists for 50ms, the output is turned off.	0: No undervoltage detected 1: Undervoltage detected
dgveeuv	0	DGVEE undervoltage status/flag. This bit is set immediately when an undervoltage is detected. If the condition persists for 50ms, the output is turned off.	0: No undervoltage detected 1: Undervoltage detected

dev_status (0x09)

Device status bits

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	hw_rst	wled_th_shdn	wled_th_warn	tft_th_shdn
Reset	–	–	–	–	0x1	0x0	0x0	0x0
Access Type	–	–	–	–	Read Clears All	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
hw_rst	3	This flag reports if a POR took place since the last time this bit was reset. It is reset when this register is read.	0: No POR since last read 1: This is the first read of this register after a POR.
wled_th_shdn	2	LED driver thermal-shutdown status flag.	0: No thermal shutdown 1: Backlight driver is in thermal shutdown
wled_th_warn	1	LED driver thermal-warning status flag.	0: Device junction temperature is below 125°C 1: Device junction temperature is equal to or greater than 125°C
tft_th_shdn	0	TFT section thermal-shutdown status flag.	0: No thermal shutdown 1: TFT section is in thermal shutdown

bl_fault_masks (0x0A)

Backlight LED string masks for fault bits

BIT	7	6	5	4	3	2	1	0
Field	led_open_mask[3:0]				led_short_mask[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
led_open_mask	7:4	This field contains masks for the corresponding led_open flags. A bit set to 1 in this field implies that the corresponding status flag will not casue the FLTB pin to assert.	0: Status flag causes FLTB pin assertion 1: Status flag does not cause FLTB pin assertion
led_short_mask	3:0	This field contains masks for the corresponding led_short flags. A bit set to 1 in this field implies that the corresponding status/flag will not contribute to fault-pin assertion.	0: Status flag causes FLTB pin assertion 1: Status flag does not cause FLTB pin assertion

fault_masks1 (0x0B)

TFT masks for fault bits

BIT	7	6	5	4	3	2	1	0
Field	boostuv_mask	boostov_mask	led_shortgnd_mask	hvinpuv_mask	wled_ss_time	neguv_mask	dgvdduv_mask	dgveeuv_mask
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
boostuv_mask	7	Mask for backlight boost undervoltage status flag.	0: Boost UV will cause FLTB pin assertion 1: Boost UV will not cause FLTB pin assertion
boostov_mask	6	Mask for backlight boost overvoltage status flag.	0: Boost OV will cause FLTB pin assertion 1: Boost OV will not cause FLTB pin assertion
led_shortgnd_mask	5	Mask for led_shortgnd status flag.	0: A short-to-ground fault will cause FLTB pin assertion 1: A short-to-ground fault will not cause FLTB pin assertion
hvinpuv_mask	4	Mask for HVINP undervoltage status flag.	0: A HVINP UV fault will cause FLTB pin assertion 1: A HVINP UV fault will not cause FLTB pin assertion
wled_ss_time	3	Backlight boost soft-start and final voltage setting.	0: Standard 50ms soft-start with final value of 0.6V on OVP. 1: Accelerated start-up (22ms) with final value of 1.1V on OVP.
neguv_mask	2	Mask for NEG undervoltage status flag.	0: A NEG UV fault will cause FLTB pin assertion 1: A NEG UV fault will not cause FLTB pin assertion
dgvdduv_mask	1	Mask for DGVDD undervoltage status flag.	0: A DGVDD UV fault will cause FLTB pin assertion 1: A DGVDD UV fault will not causeFLTB pin assertion
dgveeuv_mask	0	Mask for DGVEE undervoltage status flag.	0: A DGVEE UV fault will cause FLTB pin assertion 1: A DGVEE UV fault will not cause FLTB pin assertion

fault_masks2 (0x0C)

Masks for ofaults contained in register dev_status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	wled_th_warn_mask	–
Reset	–	–	–	–	–	–	0x0	–
Access Type	–	–	–	–	–	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
wled_th_warn_mask	1	Mask for wled_th_warn status flag.	0: Status flag will cause FLTB pin assertion 1: Status flag will not cause FLTB pin assertion

Applications Information

TFT Power Section

Boost Converter

Boost Converter Inductor Selection

Three key inductor parameters must be specified for operation with the device: Inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). To determine the inductance value, first select the ratio of inductor peak-to-peak ripple current to average output current (LIR). Higher LIR values mean higher RMS inductor current and therefore, higher I^2R losses. To achieve a lower LIR value, a high-valued inductor, which may be physically larger, must be used. A good compromise between size and loss is to select a 30% to 60% peak-to-peak ripple current to average-current ratio (LIR from 0.3 to 0.6). If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best LIR may lie between 0.5 and 1.0. The value of the inductor is determined by the following equations.

Equation 9:

$$L = \frac{V_{INA} \times D}{LIR \times I_{IN} \times f_{SW}}$$

using:

Equation 10:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{INA}}$$

$$D = 1 - \frac{V_{INA}}{V_{OUT}}$$

where V_{INA} is the input voltage, V_{OUT} is the output voltage, I_{OUT} is the output current, I_{IN} is the calculated average boost input current, η is the efficiency of the boost converter, D is the duty cycle, and f_{SW} is either 440kHz or 2.2MHz (the selected switching frequency of the boost converter). The efficiency of the boost converter can be estimated from the *Typical Operating Characteristics* and accounts for losses in the internal switch, inductor, and capacitors.

The inductor's saturation rating must exceed the maximum current limit of 1.7A or 0.74A, depending on the setting of the lxp_lim_low bit in the cnfg_gen (0x01) register.

Boost Output-Filter Capacitor Selection

The primary criterion for selecting the output-filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determine the amplitude of the high-frequency ripple seen on the output voltage. For stability, the boost output-filter capacitor should have a value of 10µF or greater.

To avoid a large drop on HVINP when POS is enabled, the capacitance on the HVINP node should be at least three times larger than that on POS.

Setting the POS Voltage

In stand-alone mode, the POS output voltage is set by connecting FBP to a resistive voltage divider between HVINP and GND. Select the lower feedback resistor value and calculate the upper resistor value using the following formula.

Equation 11:

$$R_{UPPER} = \frac{(V_{HVINP} - 1.25) \times R_{LOWER}}{1.25}$$

In I^2C mode, the POS output is set by writing an 8-bit value to the vpos_set (0x03) register.

The NEG converter outputs a negative voltage whose absolute value is the same as POS. The most negative voltage the NEG can output is -7V.

NEG Inverting Regulator

NEG Regulator Inductor Selection

The inductor value for the NEG regulator can be selected using the following formula.

Equation 12:

$$L = \frac{V_{NEG} \times (1 - D)^2}{LIR \times I_{NEG} \times f_{SW}}$$

where V_{NEG} is the output voltage, I_{NEG} the output current, LIR the desired inductor ripple ratio, and f_{SW} is the the switching frequency.

Calculate the duty-cycle D using:

Equation 13:

$$D = \frac{V_{NEG}}{V_{IN} + V_{NEG}}$$

The inductor's saturation current rating must exceed the maximum current-limit setting of 1.2A or 0.6A, depending on the setting of the neg_lim_low bit in the cnfg_gen (0x01) register.

NEG External Diode Selection

Select a diode with a peak current rating of at least the selected LXN current limit (1.8A or 1.1A) for use with the NEG output. The diode breakdown-voltage rating should exceed the sum of the maximum INN voltage and the absolute value of the NEG voltage. A Schottky diode improves the overall efficiency of the converter.

NEG Output Capacitor Selection

The primary criterion for selecting the output filter capacitor is low ESR and capacitance value, as the NEG capacitor provides the load current when the internal switch is on. The voltage ripple on the NEG output has two components:

- Ripple due to ESR, which is the product of the peak inductor current and the output filter capacitor's ESR
- Ripple due to bulk capacitance that can be determined as follows.

Equation 14:

$$\Delta V_{BULK} = \frac{I_{NEG} \times \frac{D}{f_{SW}}}{C_{NEG}}$$

For stability, the NEG output capacitor should have a value of 10µF or greater.

Setting the DGVDD and DGVEE Output Voltages

For most applications, a single charge-pump stage is sufficient for both the positive and negative charge pumps. In the case of DGVDD, the maximum output voltage is then twice the HVINP voltage. For DGVEE, the most negative voltage is $-V_{HVINP}$. If necessary, add further stages while maintaining the DGVDD and DGVEE voltages within their permitted operating ranges.

The DGVDD output voltage is set in stand-alone mode with a resistor-divider from DGVDD to GND, with its center connected to the FBPG pin. After a value for R_{LOWER} is selected, R_{UPPER} can be calculated using the following formula.

Equation 15:

$$R_{UPPER} = \frac{(DGVDD - 1.25) \times R_{LOWER}}{1.25}$$

The DGVEE output voltage is set by connecting a resistor-divider from REF to DGVEE, with its center connected to FBNG. The control loop forces FBNG to 0V. Select the resistor connected to REF (R_{REF}) so that less than 100µA is drawn from REF (i.e., the value of R_{REF} shall be greater than 12.5kΩ). After selecting R_{REF}, calculate R_{DGVEE} using Equation 16.

Equation 16:

$$R_{DGVEE} = \frac{R_{REF} \times |DGVEE|}{1.25}$$

In I2C mode, the DGVDD and DGVEE voltages are set by writing a 6-bit value to the dgvdd_set (0x04) register and a 5-bit value to the dgvee_set (0x05) register, respectively.

LED Driver Section

DC-DC Converter for LED Driver

Two different converter topologies are possible with the DC-DC controller in the device, which has the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string forward voltage is always higher than the input supply voltage range, use the boost-converter topology. If the LED string forward voltage falls within the supply-voltage range, use the SEPIC topology.

Note that the boost converter topology provides the highest efficiency.

Power-Circuit Design

First select a converter topology based on the above factors. Determine the required input supply-voltage range, the maximum voltage needed to drive the LED strings, including the worst-case 1V across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}) as shown below.

Equation 17:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

where I_{STRING} is the LED current per string in amperes and N_{STRING} is the number of strings used. Calculate the maximum duty cycle (D_{MAX}) using the following equations:

Equation 18 (for the boost configuration):

$$D_{MAX} = \frac{\left(V_{LED} + V_{D1} - V_{IN_MIN}\right)}{\left(V_{LED} + V_{D1} - V_{DS} - 0.42\right)}$$

Equation 18 (for the SEPIC configuration):

$$D_{MAX} = \frac{\left(V_{LED} + V_{D1}\right)}{\left(V_{IN_MIN} - V_{DS} - 0.42 + V_{LED} + V_{D1}\right)}$$

where V_{D1} is the forward drop of the rectifier diode in volts (approximately 0.6V), V_{IN_MIN} is the minimum input supply voltage in volts, V_{DS} is the drain-to-source voltage of the external MOSFET in volts when it is on, and 0.42V is the peak current-sense voltage. Initially, use an approximate value of 0.2V for V_{DS} to calculate D_{MAX}. Calculate a more accurate value of D_{MAX} after the power MOSFET is selected based on the maximum inductor current.

Boost Configuration

The average inductor current varies with the line voltage, and the maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔIL). The recommended peak-to-peak ripple is 60% of the average inductor current.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (IL_P) in amperes.

Equation 20:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple ΔIL to be ±30% of the average inductor current:

Equations 21:

$$\Delta I_L = IL_{AVG} \times 0.3 \times 2$$

and

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

Calculate the minimum inductance value (L_{MIN}), in henries with the inductor-current ripple set to the maximum value.

Equation 22:

$$L_{MIN} = \frac{\left(V_{IN_MIN} - V_{DS} - 0.42\right) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

where 0.42V is the peak current-sense voltage. Choose an inductor that has a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design, with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts (see *Typical Application Circuits*). One of the inductors (L2) has the LED current as the average current, and the other inductor (L1) has the input current as its average current. Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL2_{AVG}$) and peak inductor currents ($IL1_P$, $IL2_P$) in amperes:

Equation 23:

$$IL1_{AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a 10% margin to account for the converter losses:

Equation 24:

$$IL2_{AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple ΔIL is ±30% of the average inductor current:

Equations 25:

$$\Delta I_{L1} = IL1_{AVG} \times 0.3 \times 2$$

and

$$IL1_P = IL1_{AVG} + \frac{\Delta I_{L1}}{2}$$

$$\Delta I_{L2} = IL2_{AVG} \times 0.3 \times 2$$

and

$$IL2_P = IL2_{AVG} + \frac{\Delta I_{L2}}{2}$$

Calculate the minimum inductance values $L1_{MIN}$ and $L2_{MIN}$ in henries with the inductor current ripples set to the maximum value as follows:

Equations 26:

$$L1_{MIN} = \frac{\left(V_{IN_MIN} - V_{DS} - 0.42\right) \times D_{MAX}}{f_{SW} \times \Delta I_{L1}}$$

$$L2_{MIN} = \frac{\left(V_{IN_MIN} - V_{DS} - 0.42\right) \times D_{MAX}}{f_{SW} \times \Delta I_{L2}}$$

where 0.42V is the peak current-sense voltage. Choose inductors that have a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$, and current ratings greater than $IL1_P$ and $IL2_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

For simplifying further calculations, consider L1 and L2 as a single inductor with L1/L2 connected in parallel. The combined inductance value and current is calculated as follows:

Equations 27:

$$L_{MIN} = \frac{L1_{MIN} \times L2_{MIN}}{L1_{MIN} + L2_{MIN}}$$

and

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where IL_{AVG} represents the total average current through both the inductors, connected together for SEPIC configuration. Use these values in the calculations for the SEPIC configuration in the following sections.

Select coupling capacitor CS so that the peak-to-peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series resonant circuit comprising L1, CS, and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of CS.

Equation 28:

$$CS \geq \frac{I_{LED} \times D_{MAX}}{V_{IN_MIN} \times 0.02 \times f_{SW}}$$

where CS is the minimum value of the coupling capacitor in farads, I_{LED} is the LED current in amperes, and the factor 0.02 accounts for 2% ripple.

Current-Sense Resistor and Slope Compensation

The MAX20069C backlight boost generates a current ramp for slope compensation. This ramp current is in sync with the switching frequency, starting from zero at the beginning of every clock cycle and rising linearly to reach 50µA at the end of the clock cycle. The slope-compensating resistor (R_{SC}) is connected between the CS input and the source of the external MOSFET. This adds a programmable ramp voltage to the CS input voltage to provide slope compensation.

Use the following equation to calculate the value of slope-compensation resistance (R_{SC}):

Equation 29: (for boost configuration):

$$R_{SC} = \frac{(V_{LED} - 2 \times V_{IN_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

Equation 30: (for SEPIC and coupled-inductor configurations):

$$R_{SC} = \frac{(V_{LED} - V_{IN_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

where V_{LED} and V_{IN_MIN} are in volts, R_{SC} and R_{CS} are in ohms, L_{MIN} is in henries, and f_{SW} is in hertz. The value of the switch current-sense resistor (R_{CS}) can be calculated as follows:

Equation 31: (for the boost configuration):

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.39 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times \left(V_{LED} - 2 \times V_{IN_MIN}\right) \times 3}$$

Equation 32: (for SEPIC and coupled-inductor configurations):

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.39 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times \left(V_{LED} - V_{IN_MIN}\right) \times 3}$$

where 0.39 is the minimum value of the peak current-sense threshold. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold of 0.4 is multiplied by 0.9 to take tolerances into account.

Output Capacitor Selection

For all converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears

across the constant-current sink outputs because the LED string voltages are stable due to the constant current. For the MAX20069C, limit the peak-to-peak output-voltage ripple to 200mV to get stable output current.

The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects, connecting multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming however, it may be desirable to limit the use of ceramic capacitors on the boost output. In such cases, an additional electrolytic or tantalum capacitor can provide the majority of the bulk capacitance.

External Switching-MOSFET Selection

The external switching MOSFET should have a voltage rating sufficient to withstand the maximum boost output voltage, together with the rectifier diode drop and any possible overshoot due to ringing caused by parasitic inductance and capacitance. The recommended MOSFET V_{DS} voltage rating is 30% higher than the sum of the maximum output voltage and the rectifier diode drop.

The continuous-drain current rating of the MOSFET (ID), when the case temperature is at the maximum operating ambient temperature, should be greater than that calculated below.

Equation 33:

$$ID_{RMS} = \left(\sqrt{IL_{AVG}^2 \times D_{MAX}}\right) \times 1.3$$

The MOSFET dissipates power due to both switching losses and conduction losses. Use the following equation to calculate the conduction losses in the MOSFET.

Equation 34:

$$P_{COND} = IL_{AVG}^2 \times D_{MAX} \times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the on-state drain-to-source resistance of the MOSFET. Use the following equation to calculate the switching losses in the MOSFET.

Equation 35:

$$P_{SW} = \frac{IL_{AVG} \times V_{LED}^2 \times C_{GD} \times f_{SW}}{2} \times \left(\frac{1}{I_{GON}} + \frac{1}{I_{GOFF}}\right)$$

where I_{GON} and I_{GOFF} are the gate currents of the MOSFET in amperes when it is turned on and turned off, respectively. C_{GD} is the gate-to-drain MOSFET capacitance in farads.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than that calculated in the following equation.

Equation 36:

$$I_D = IL_{AVG} \times \left(1 - D_{MAX}\right) \times 1.2$$

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to fall within the window comparator limits of 0.8V and 1.1V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the steady-state condition in the form of capacitor voltages, primarily the output filter-capacitor voltage and compensation-capacitor voltage. When the PWM dimming pulses are less than 24 switching-clock cycles, the feedback loop regulates the converter output voltage to 95% of the OVP threshold.

The worst-case condition for the feedback loop is when the LED driver is in normal mode regulating the minimum OUT_ voltage. The switching converter small-signal transfer function has a right-half plane (RHP) zero for boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain and a 90° phase lag,

which is difficult to compensate.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Equation 37 (for boost configuration):

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED}}$$

Equation 38 (for SEPIC configuration):

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries, and I_{LED} is in amperes. A simple way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/ decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f_{P1}), calculated as follows:

Equation 39 (for boost configuration):

$$f_{P1} = \frac{I_{LED}}{2\pi \times V_{LED} \times C_{OUT}}$$

Equation 40 (for SEPIC configuration):

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{2\pi \times V_{LED} \times C_{OUT}}$$

where f_{P1} is in hertz, V_{LED} is in volts, I_{LED} is in amperes, and C_{OUT} is in farads. Compensation components (R_{COMP} and C_{COMP}) perform two functions: C_{COMP} introduces a low-frequency pole that presents a -20dB/ decade slope to the loop gain, and R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this zero is placed at the output pole frequency (f_{P1}), so it provides a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP} needed to fix the total loop gain at f_{P1}, so the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency, is calculated as follows.

Equation 41 (for boost configuration):

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times \left(1 - D_{MAX}\right)}$$

Equation 42 (for SEPIC configuration):

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times D_{MAX}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times \left(1 - D_{MAX}\right)}$$

where R_{COMP} is the compensation resistor in ohms, f_{ZRHP} and f_{P2} are in hertz, R_{CS} is the switch current-sense resistor in ohms, and GM_{COMP} is the transconductance of the error amplifier (700µS).

The value of C_{COMP} is calculated as follows.

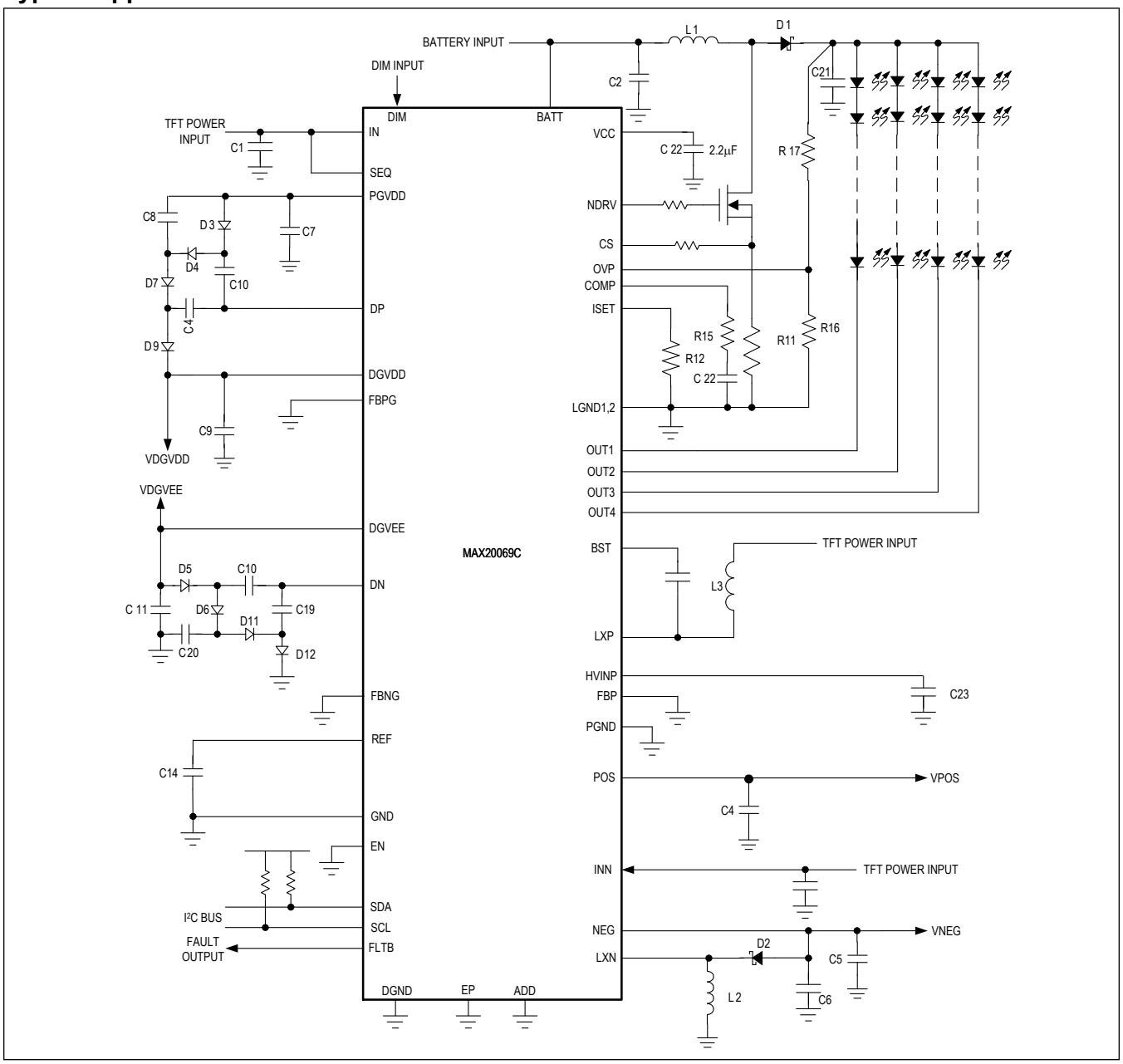
Equation 43:

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times f_{Z1}}$$

where f_{Z1} is the compensation zero placed at 1/5 of the crossover frequency that is, in turn, set at 1/5 of the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency may fall within the 0dB crossover frequency. An additional pole may be required to cancel out this pole placed at the same frequency. This is usually implemented by connecting a capacitor in parallel with C_{COMP} and R_{COMP}.

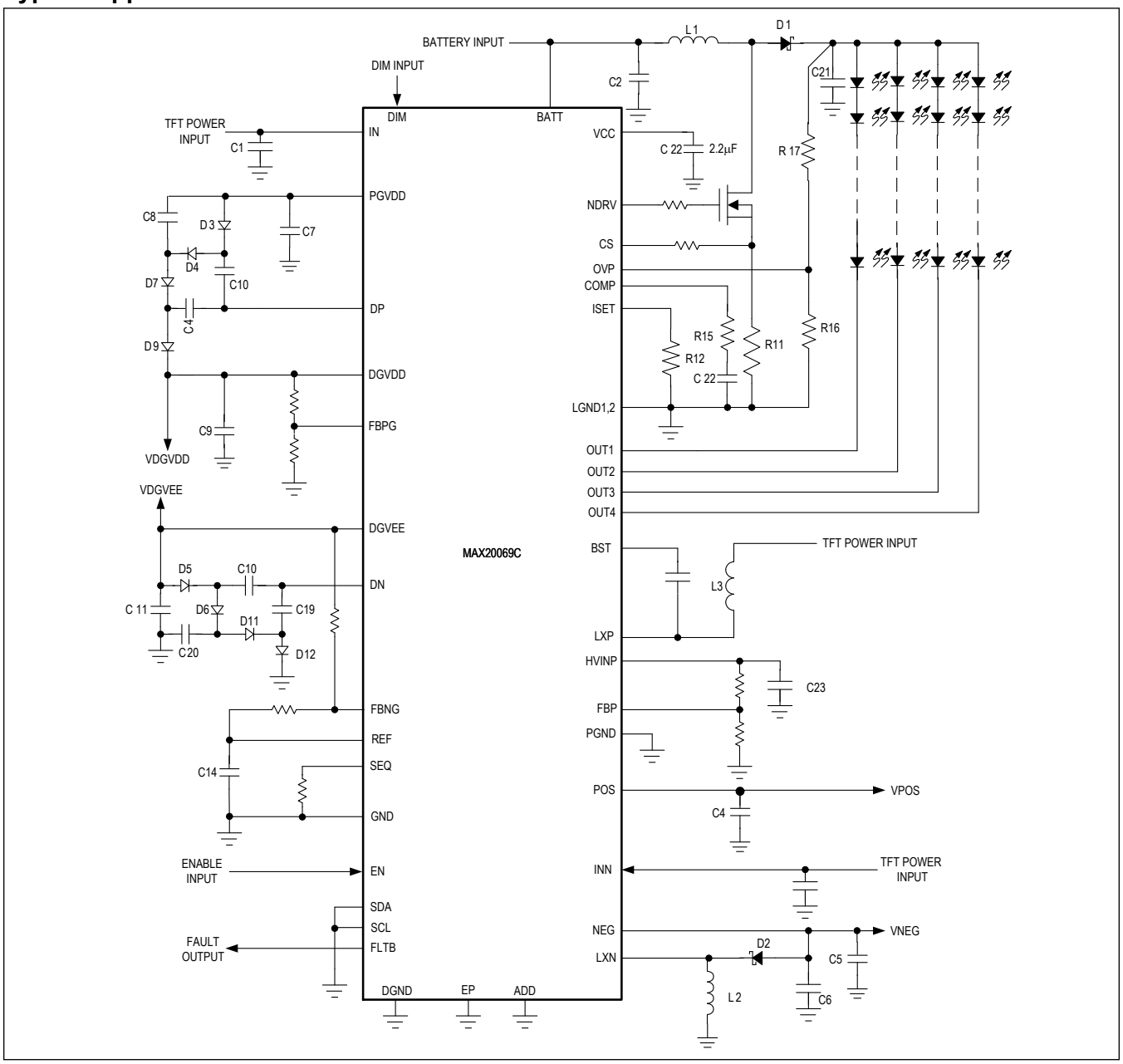
Typical Application Circuits

Typical Application Circuit for I²C Mode



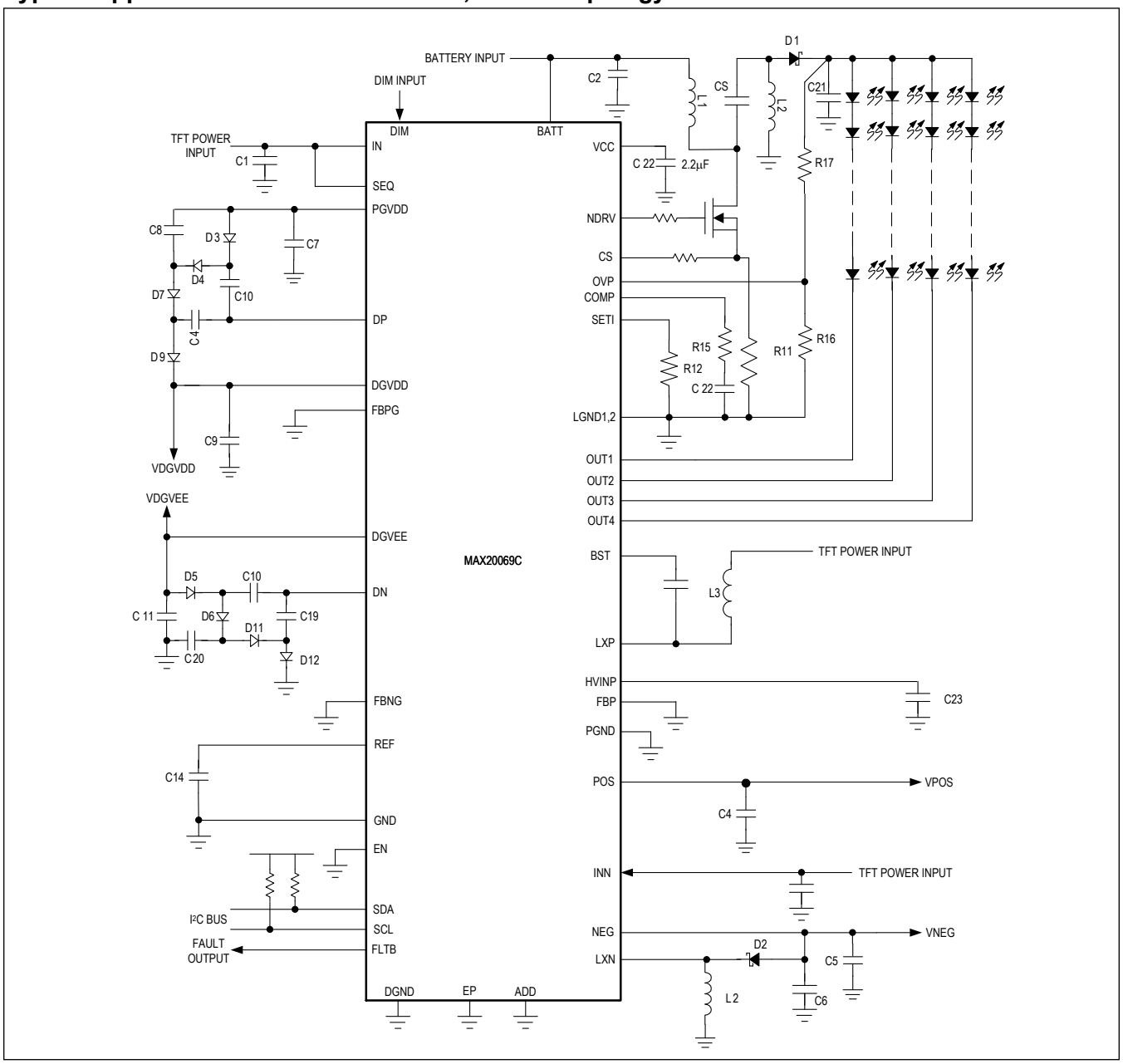
Typical Application Circuits (continued)

Typical Application Circuit for Stand-Alone Mode



Typical Application Circuits (continued)

Typical Application Circuit for I²C Mode, SEPIC Topology



Ordering Information

PART	TEMP RANGE	PACKAGE CODE	PIN-PACKAGE	7b I2C ADDRESS
MAX20069CGTL/V+	-40°C to +105°C	T4066-5C	40 TQFN-EP*	0x60/0x64
MAX20069CGTL/V+T	-40°C to +105°C	T4066-5C	40 TQFN-EP*	0x60/0x64
MAX20069CGTL/VY+	-40°C to +105°C	T4066Y-6C	40 TQFN-EP*	0x60/0x64
MAX20069CGTL/VY+T	-40°C to +105°C	T4066Y-6C	40 TQFN-EP*	0x60/0x64
MAX20069CGTLA/V+**	-40°C to +105°C	T4066-5C	40 TQFN-EP*	0x20/0x24
MAX20069CGTLA/V+T**	-40°C to +105°C	T4066-5C	40 TQFN-EP*	0x20/0x24
MAX20069CGTLA/VY+**	-40°C to +105°C	T4066Y-6C	40 TQFN-EP*	0x20/0x24
MAX20069CGTLA/VY+T**	-40°C to +105°C	T4066Y-6C	40 TQFN-EP*	0x20/0x24

/V Denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Y = Side-wettable (SW) package

***Potential future product*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/19	Initial release	—
1	11/21	Added Simplified Block Diagram, added 40 TQFN-SW in *Package Information*, changed $V_{NEG_POS_REG}$ minimum limit in the *Electrical Characteristics* table, corrected I2C addresses in the *Detailed Description* and *Ordering Information* table, updated *NEG Inverting Regulator* section, removed future product notation from MAX20069CGTL in *Ordering Information* table	2, 7, 9, 31, 47, 56
2	4/25	Corrected I2C addresses in the *Detailed Description* and *Ordering Information* tables	31, 56

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