SilentMOS Smart Power Stage in 5 mm × 8 mm LQFN

FEATURES

- 140 A Peak Output Current
- SilentMOS™ Smart Power Stage
  - Utilizes Low EMI/EMC Silent Switcher®2 Architecture
  - Ultra-Low SW-Voltage Overshoot
  - Frequency Up to 2 MHz
- V_{IN} Up to 14 V
- Up to 94% Efficiency at 1 MHz with 1.8 V_{OUT}
- Integrated Boost Diode and Capacitors and Power Switches
- Accurate Switch Current Monitoring
- Power MOSFET Overcurrent Protection
- Input Overvoltage and Bias Undervoltage Protection
- 3.3 V/5 V Compatible Tri-State PWM Input Thermal Monitor with Overtemperature Flag
- 5 mm × 8 mm LQFN Package

APPLICATIONS

- High Current Servers and Workstations
- Networking/Telecom Microprocessor Supplies
- Small Form-Factor POL Converter

GENERAL DESCRIPTION

The LTC7051[1] monolithic power stage fully integrates high speed drivers with low resistance half-bridge power switches plus comprehensive monitoring and protection circuitry in an electrically and thermally optimized package. With a suitable high frequency controller, this power stage forms a compact, high current voltage regulator system with state-of-the-art efficiency and transient response.

SilentMOS technology utilizes second generation Silent Switcher 2 architecture reducing both EMI and switch-node voltage overshoot while maximizing efficiency at high switching frequencies.

High speed current sensing provides low latency switch current information, enabling tight current balancing and immediate overcurrent protection.

Thermally-enhanced packaging provides 70 A rated output continuous current capability.

TYPICAL APPLICATION

Figure 1. 12 V_{IN}, 1 V/60 A_{OUT} 1 MHz POL Converter

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[1] Protected by U.S. patents, including 9,525,351.

Rev. C

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REVISION HISTORY

FUNCTIONAL BLOCK DIAGRAM
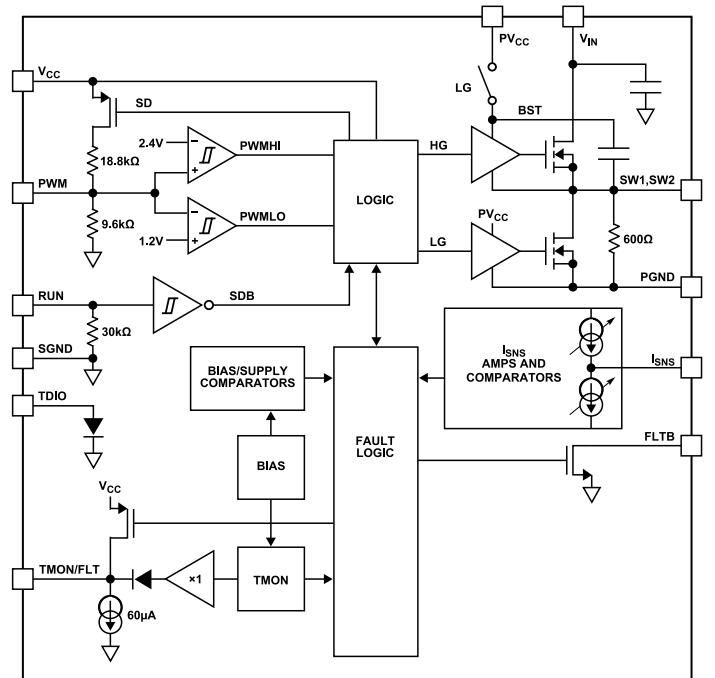
Figure 2.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

T_J = −40°C to +125°C for the minimum and maximum values, T_A = 25°C, V_{IN} = 12 V, PV_{CC} = V_{CC} = 5 V, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
V_{IN} SUPPLY						
Power Input Supply Range	V_{IN}				14	V
V_{IN} Overvoltage Lockout Threshold		V_{IN} Rising	14.9		15.7	V
V_{IN} Overvoltage Lockout Hysteresis				1		V
V_{IN} Overvoltage Lockout Delay[2]				1		µs
V_{IN} Shutdown Current		V_{IN} = 12 V, RUN = 0		25		µA
V_{CC} SUPPLY						
V_{CC} Input Supply Range	V_{CC}		4.5	5	5.5	V
V_{CC} Undervoltage Lockout Threshold	$V_{CC(UVLO)}$	V_{CC} Rising	4.05	4.2	4.25	V
V_{CC} Undervoltage Lockout Hysteresis	V_{UVLO_HYST}			0.2		V
V_{CC} Supply Current in Shutdown	$I_{VCC(SD)}$	RUN = 0 V		14		µA
V_{CC} Supply Current in Active	I_{VCC_active}	RUN = 5 V, PWM = Float		2.5		mA
PV_{CC} SUPPLY						
Driver Input Supply Range	PV_{CC}		4.5	5	5.5	V
PV_{CC} Undervoltage Lockout Threshold	$PV_{CC(UVLO)}$	PV_{CC} Rising	3.9	4.2	4.1	V
PV_{CC} Undervoltage Lockout Hysteresis	PV_{UVLO_HYST}			0.35		V
PV_{CC} Supply Current in Shutdown	$I_{PVCC(SD)}$	RUN = 0 V		300		µA
PV_{CC} and V_{CC} Supply Current in Active	I_{PVCC_active}	RUN = 5 V, PWM = Float		2.5		mA
UNDERVOLTAGE TIME LOCKOUT DELAY, FROM V_{CC} AND PV_{CC} TO SW LOW	t_{UVLO}	PV_{CC}, V_{CC} Rising, RUN = 5 V, PWM = 0[2]		1		µs
RUN INPUT						
RUN High Threshold	V_{IH_RUN}	RUN Rising	2.2	2.45	2.7	V
RUN Hysteresis	V_{RUN_HYS}			0.2		V
EN Pull-Down Resistor	R_{PD_RUN}			30		kΩ
Propagation Delay for RUN Low to High	T_{d_RUNH}	From RUN Low ≥ High to SW = 0, PWM = 0		12		µs
Propagation Delay for RUN High to Low	T_{d_RUNL}	From RUN High ≥ Low to SW High Z, PWM = 0[2]			0.1	µs
PWM INPUT						
PWM High Threshold	V_{IH_PWM}	V_{IN} = 1 V, PV_{CC} = 6 V			2.7	V
PWM Low Threshold	V_{IL_PWM}	V_{IN} = 5 V	0.8			V
PWM Tri-State Range	V_{TR_PWM}	V_{IN} = 1 V and 5 V	1.5		2.1	V
PWM Pull-Down Resistor	R_{PD_PWM}	To SGND, V_{IN} = 5 V		9.6		kΩ
PWM Pull-Up Resistor	R_{PU_PWM}	To V_{CC}, V_{IN} = 5 V		18.8		kΩ
Delay Time, PWM High to SW High	$t_{PWMHI-SW}$	No Fault Condition[2]		10		ns
Delay Time, PWM Low to SW Low	$t_{PWMLO-SW}$	No Fault Condition[2]		10		ns
Tri-State to Low Propagation Delay	$t_{Tri\_Lo\_Delay}$	PWM Going Low to SW Going Low, V_{IN} = 5 V		20		ns
Tri-State to High Propagation Delay	$t_{Tri\_Hi\_Delay}$	PWM Going High to SW Going High, V_{IN} = 5 V		30		ns
Active to Tri-State Delay Time	t_{Tri_Hold}	PWM Going to High Z to SW High Z[2]		20		ns
PWM Minimum ON-Time	t_{PWM_MINON}	V_{IN} = 5 V		20		ns
PWM Floating Voltage	V_{PWM_FLOAT}		1.6	1.7	1.8	V
I_{SNS} OUTPUT						
Current Sense Gain (I_{MON}/I_{OUT})	A_{IMON}	V_{ISNS} = 1.5 V, V_{IN} = 5 V, I_{OUT} = 10 A to 50 A, PWM = 0	8.5	10	11.5	µA/A
Overall Accuracy	I_{SNS}	I_{OUT} = 50 A, V_{ISNS} = 1.5 V, V_{IN} = 5 V, PWM = 0, Accuracy at Trim		500 ±40		µA
		I_{OUT} = −10 A, V_{ISNS} = 1.5 V, PWM = 0		100		µA

SPECIFICATIONS

Table 1. (Continued)

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
IMON Operational Voltage Range	V_{IMON}	V_{IN} = 5 V	1.2		2.0	V
FLTB OUTPUT						
Fault Bar Open-Drain Pull-Down Resistance	$R_{FLTB-PD}$	FLTB Low			1	kΩ
TMON/FLT OUTPUT						
Thermal Monitor Gain	A_{TMON}	0°C < T_J < 150°C[2]		8		mV/°C
Thermal Monitor Voltage	V_{TMON}	T_J = 0°C[2]		0.6		V
		T_J = 25°C, V_{IN} = 1 V	780	800	825	mV
		T_J = 125°C[2]		1.6		V
Overtemperature Protection Accuracy[2]	OTP			150		°C
Overtemperature Hysteresis[2]	OTP_Hys			40		°C
Thermal Monitor Maximum Source Current	I_{SOURCE_TMON}	T_J = 25°C, TMON Forced at 0 V, V_{IN} = 1 V		650		µA
Thermal Monitor Maximum Sink Current	I_{SINK_TMON}	T_J = 25°C, TMON Forced at 1.28 V, V_{IN} = 1 V		45		µA
Tdiode Forward Voltage Drop	V_{Tdiode}	T_J = 25°C, I_F = 0.1 mA, V_{IN} = 1 V		678		mV
Tdiode Voltage Drop Temperature Coefficient		I_F = 0.1 mA[2]		−1.8		mV/°C
SW NODE						
SW Floating Voltage	V_{SW_Float}	V_{IN} = 12 V		0.7		V
SW Pull-Down Resistance	$R_{SW-PGND}$	V_{IN} = 5 V		0.6		kΩ
OVERCURRENT LIMITS						
Positive Overcurrent Threshold	$I_{\_OCP}$	PWM = H, V_{IN} = 0.2 V	160	180	200	A
Negative Overcurrent Threshold	$I_{\_NCP}$	PWM = L, V_{IN} = 1 V		−90		A
Positive Overcurrent Blanking Time	t_{Blank_OC}	PWM = H[2]		22		ns
Negative Overcurrent Blanking Time	t_{Blank_NC}	PWM = L[2]		55		ns
Positive Zero Current Threshold	$I_{\_ZCP}$	V_{IN} = 0.2 V		10		A
Negative Zero Current Threshold	$I_{\_ZCN}$	V_{IN} = 1 V		−16		A

[1] All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

[2] This parameter is not tested but is guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{IN} DC Voltage	–0.3 V to +16 V
V_{IN} Transient Voltage	–0.3 V to +20 V
SW Voltage	–0.3 V to +16 V DC
SW Voltage (20 ns)	–2 V to +20 V
PV_{CC}, V_{CC} Voltage	–0.3 V to +6 V
PWM	–0.3 V to (V_{CC} + 0.3 V)
I_{SNS}	–0.3 V to (V_{CC} + 0.3 V)
FLTB	–0.3 V to (V_{CC} + 0.3 V)
TDIO Voltage/Current	–0.3 V/+5 mA
ABSMAX T_J[1, 2]	125°C
Storage Temperature	–55°C to +150°C
Maximum Reflow (Package Body) Temperature	260°C

[1] The LTC7051 is specified over the –40°C to +125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D × θ_{JA})$

where $θ_{JA}$ (in °C/W) is the package thermal impedance.

[2] The LTC7051 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

LTC7051
TOP VIEW
(Not to Scale)

NOTES
1. $T_{J(MAX\ OPER)}$ = 125°C, θ_{JA} = 10.8°C/W ON OPTIMIZED 6-LAYER 3.6 INCHES × 2.8 INCHES PCB.
2. θ_{JC_TOP} = 8.2°C/W; θ_{JC_BO}T = 0.9°C/W; θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
3. EXPOSED PADS (V_{IN}, PGND, SW) MUST BE SOLDERED TO PCB.
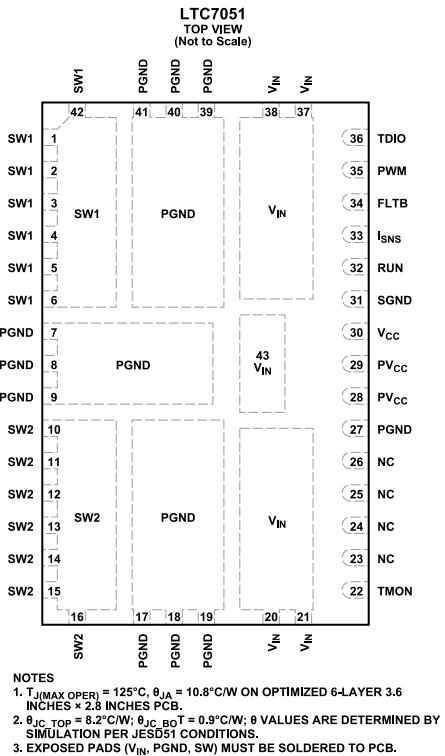
Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 6, 10 to 16, 42	SW1, SW2	Power Stage Switch Node. The output of the power stage, this node is connected to V_{IN} through the high side N-channel MOSFET and to PGND through the low side N-channel MOSFET. SW pins must be connected on the PCB.
7 to 9, 17 to 19, 27, 39 to 41	PGND	Power Stage Ground. This pin is connected to SW through the low side N-channel MOSFET. Also powers the drivers.
20 to 21, 37 to 38	V_{IN}	Power Stage Supply. This pin is connected to SW through the high side N-channel MOSFET.
22	TMON/FLT	Temperature Monitor/Fault Pin. This pin provides a voltage, referred to SGND, of 0.6 V to 1.8 V corresponding to die temperature of 0°C to 150°C for a gain of 8 mV/°C. Above 150°C, the pin is pulled high to indicate an overtemperature (OT) fault. The pin has limited current sinking capability, so multiple like pins can be tied together for highest temperature and single-OT-fault reporting.
28, 29	PV_{CC}	5 V Driver Supply. This pin powers the low side gate driver directly and the high side gate driver through an internal bootstrapped supply riding on SW. Bypass this pin with a 10 µF ceramic capacitor to PGND in close proximity to chip.
30	V_{CC}	5 V Supply. Bypass this pin with a 1 µF ceramic capacitor to SGND in close proximity to chip.
31	SGND	Circuit Ground.
32	RUN	Run Pin. When this pin is driven high, the channel is enabled. SW node is in Hi-Z state when RUN is low.
33	I_{SNS}	Current Sense Pin. This pin sources/sinks instantaneous current equal to 1/100,000 the SW node current, positive and negative.
34	FLTB	Fault Bar Pin. This open-drain pin pulls down when the chip/channel encounters a fault condition such as OC or OCN.
35	PWM	PWM Input Pin. With RUN driven high, SW will nominally follow this pin high, low, and Hi-Z. Nominal 3 V CMOS logic levels; can be driven with 3 V to 5 V CMOS signals. Resistor divider holds voltage at 1.7 V when in Hi-Z state.
36	TDIO	Temperature Diode Pin. This pin provides a reference diode to SGND for use in measuring die temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{IN} = 12 V$, $PV_{CC} = V_{CC} = 5 V$, unless otherwise noted.
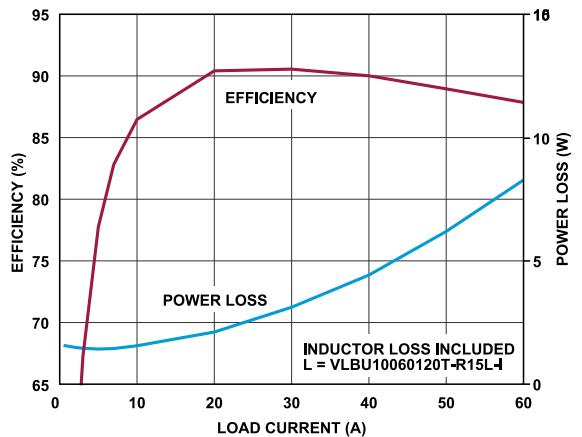
Figure 4. Efficiency vs. I_{OUT} at 1 MHz
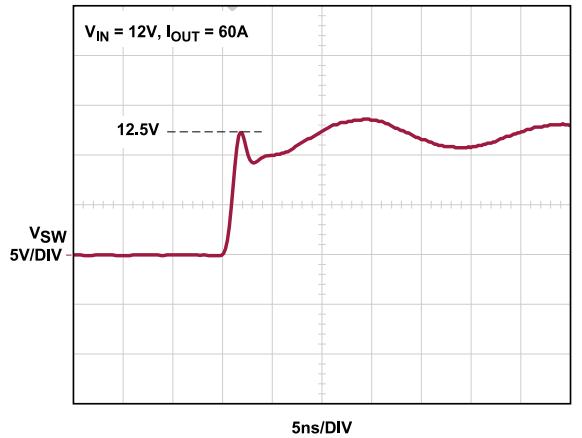
Figure 5. V_{SW} Waveform
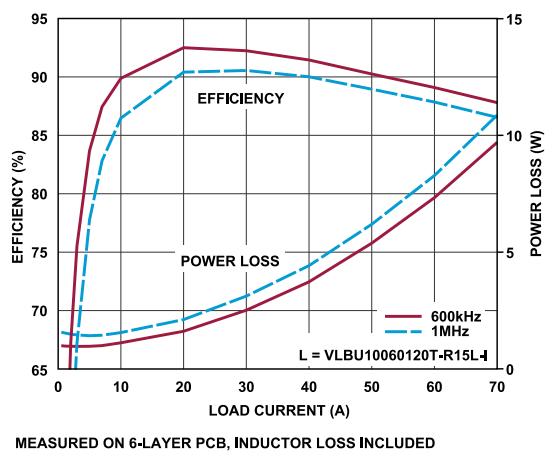
MEASURED ON 6-LAYER PCB, INDUCTOR LOSS INCLUDED

Figure 6. 12 V_{IN} to 1 V_{OUT} Efficiency
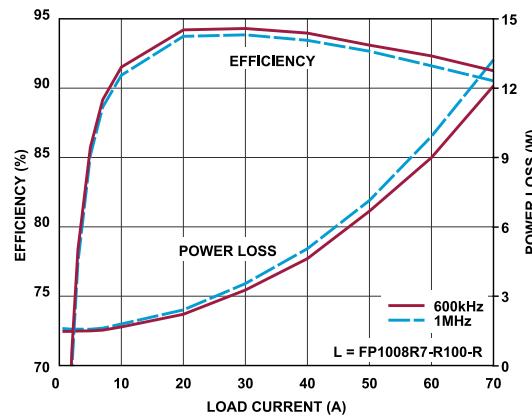
MEASURED ON 6-LAYER PCB, INDUCTOR LOSS INCLUDED

Figure 7. 12 V_{IN} to 1.8 V_{OUT} Efficiency
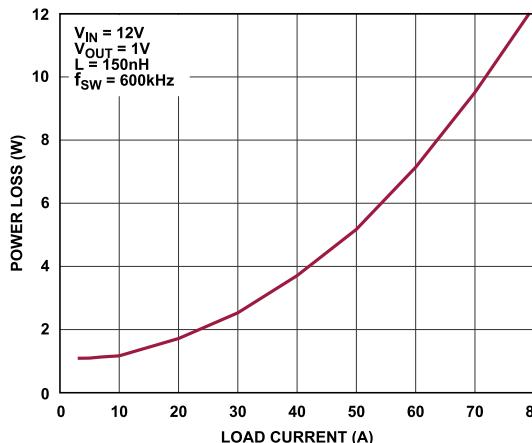

Figure 8. Power Dissipation vs. Load
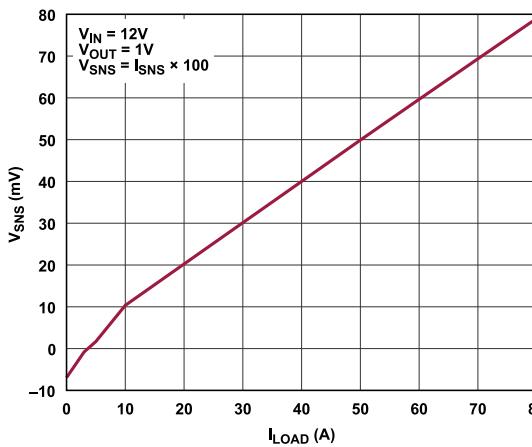
Figure 9. V_{SNS} vs. I_{LOAD}

TYPICAL PERFORMANCE CHARACTERISTICS
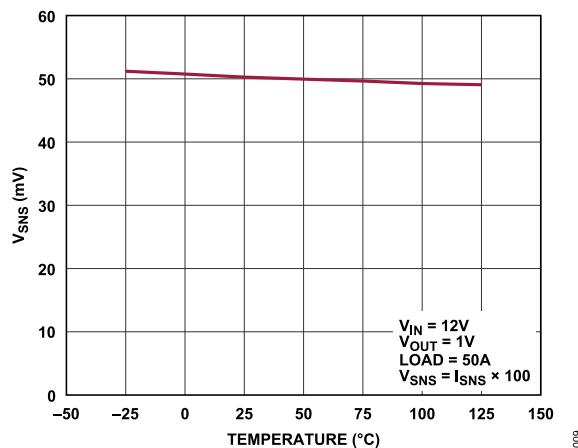
Figure 10. V_{SNS} vs. Temperature
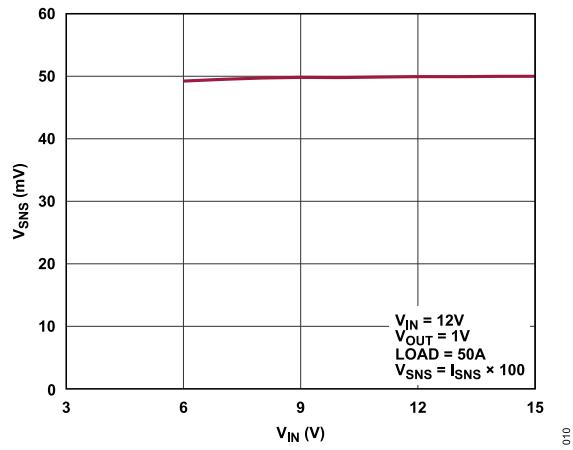
Figure 11. V_{SNS} vs. V_{IN}
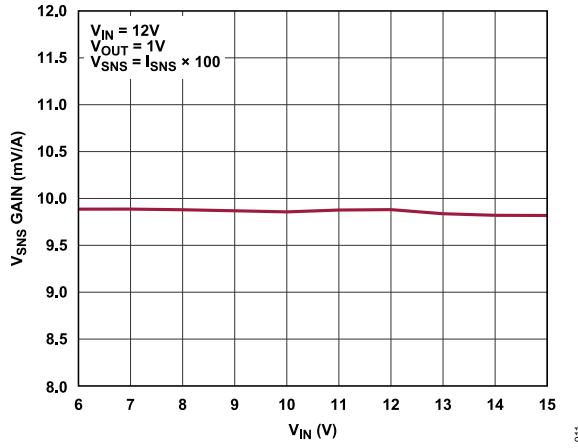
Figure 12. V_{SNS} Gain vs. V_{IN}
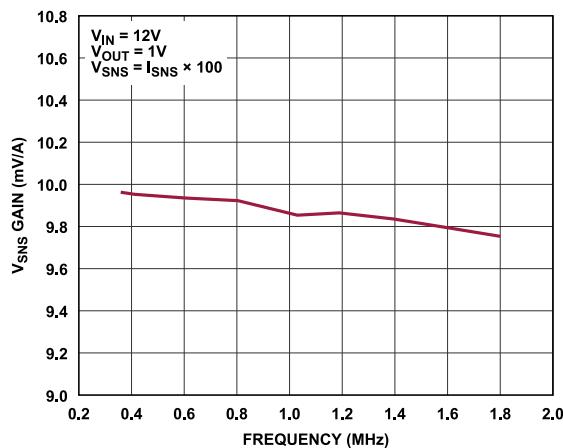
Figure 13. V_{SNS} Gain vs. Frequency
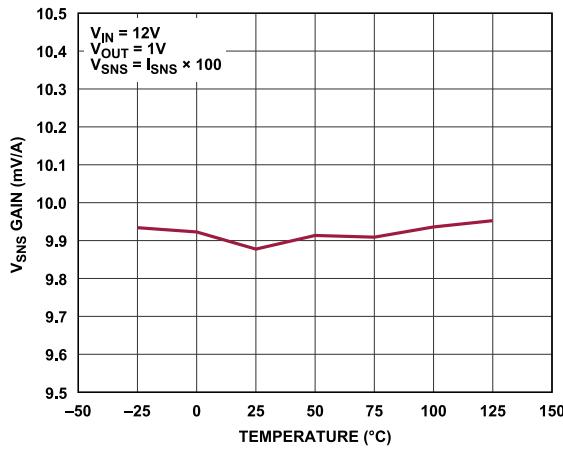
Figure 14. V_{SNS} Gain vs. Temperature
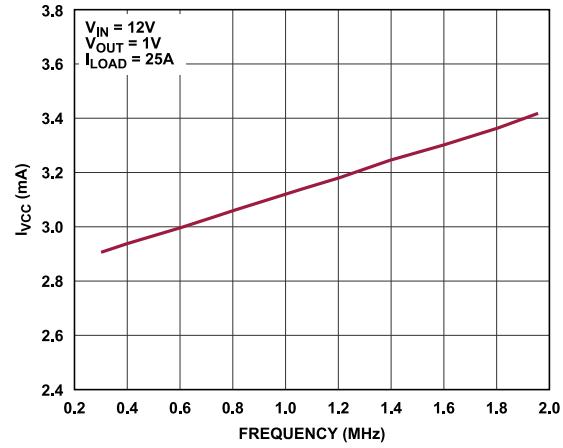
Figure 15. I_{VCC} vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS
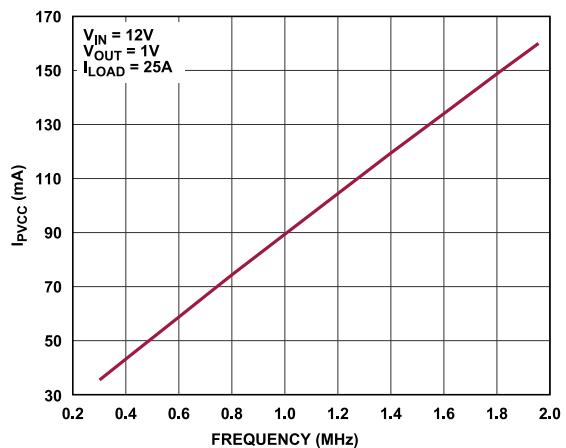
Figure 16. IPV_CC vs. Frequency
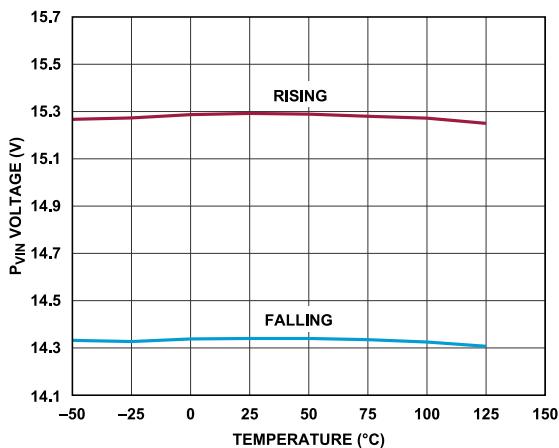

Figure 19. PV_IN OVLO vs. Temperature
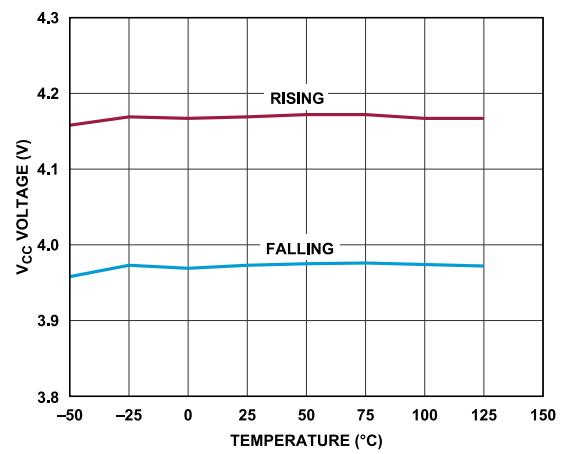
Figure 17. V_CC UVLO vs. Temperature
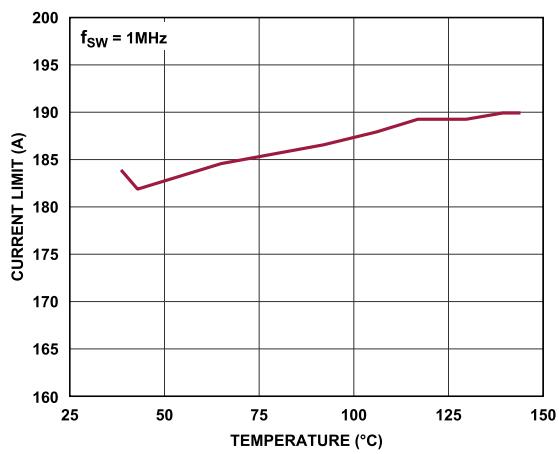

Figure 20. Current Limit vs. Temperature
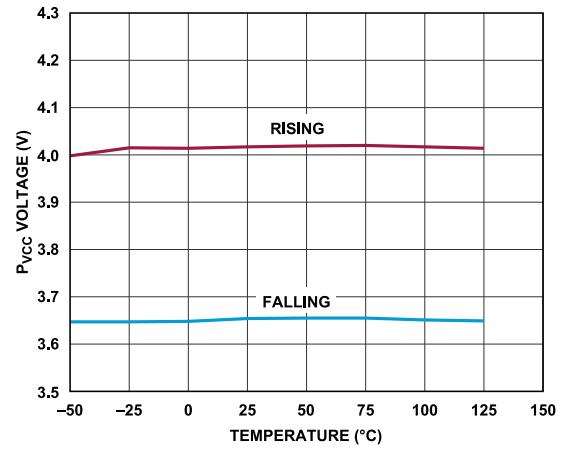
Figure 18. PV_CC UVLO vs. Temperature
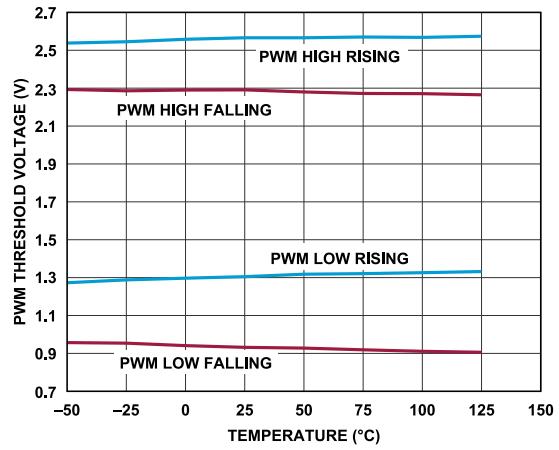
Figure 21. PWM Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS
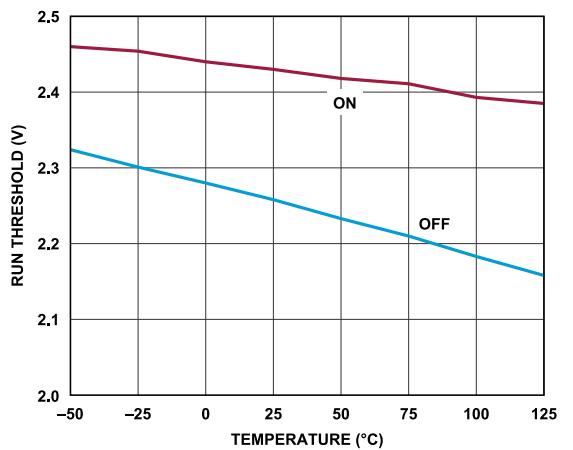
*Figure 22. RUN Threshold vs. Temperature*
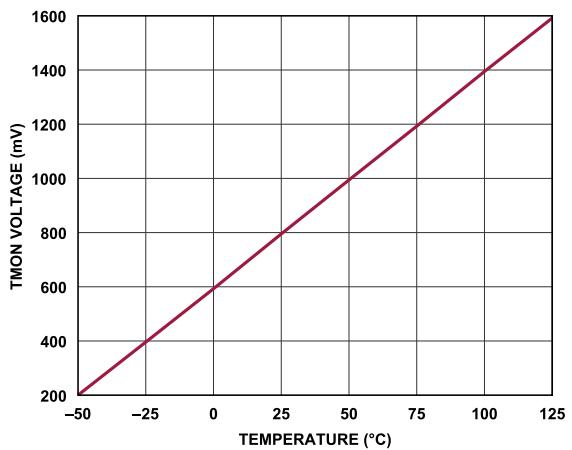

Figure 24. TMON vs. Temperature
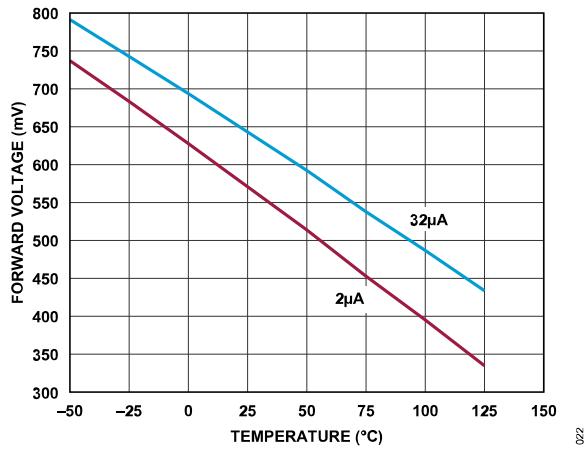
Figure 23. TDIO Forward Voltage vs. Temperature

THEORY OF OPERATION

MAIN CONTROL ARCHITECTURE

The LTC7051 is a single channel integrated-driver half-bridge power MOSFET stage for DC/DC step-down applications. It is designed to be used in a synchronous switching architecture with a controller utilizing 3.3 V or 5 V PWM three-state outputs. The relationship between the transition thresholds and the three input states of the LTC7051 is illustrated in Figure 25.
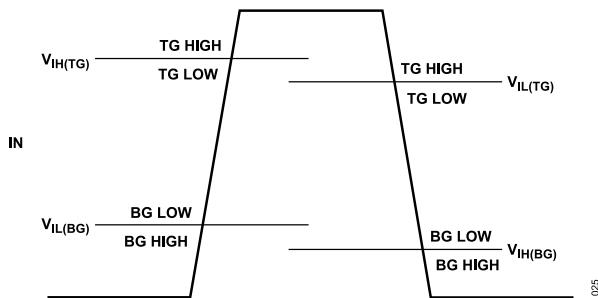
Figure 25. Three-State Input Operation

In normal operation, PWMHI turns on the high side MOSFET, and PWMLO turns on the low side MOSFET. SW node follows the PWM pin with a typical 10 ns delay. There is <1 ns dead time before SW rises from PGND to V_{IN} and a typical 3 ns dead time after SW falls.

The high side MOSFET driver is powered from the internal BST node to SW via an internal integrated switch and capacitor, which allows lower dropout than achievable with a typical diode as well as higher-frequency operation.

CURRENT SENSE

Real-time current sense amplifiers provide a scaled-down version of SW current. During PWMHI or PWMLO, the I_{SNS} pin sources or sinks, according to SW current direction, a current equal to 1/100,000 the instantaneous SW current.

Associated current comparators flag high side MOSFET positive overcurrent (OC) and low side MOSFET negative overcurrent (OCN) Zero-current of both MOSFETs are also detected by associated current comparators.

TEMPERATURE MONITOR AND OVERTEMPERATURE FAULT

Normally, TMON outputs a voltage from 0.6 V to 1.8 V, corresponding to a die temperature range of 0°C to 150°C. The TMON voltage is calculated by:

$$V_{TMON} \text{ (V)} = 800 \text{ mV} + (T_J \text{ (°C)} - 25°C) \times (8 \text{ mV/°C})$$

Figure 26 illustrates the relationship between V_{TMON} and die temperature.
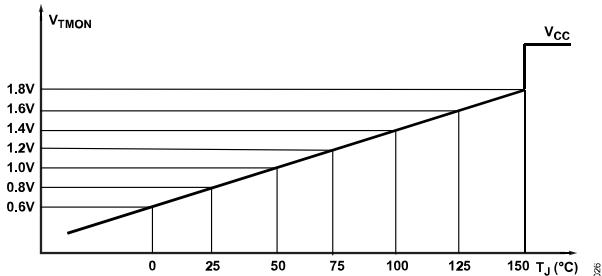
Figure 26. V_{TMON} vs. Die Temperature

TMON is driven by an amplifier that can source current but has limited sinking capacity. This allows multiple TMON pins to be paralleled, with the highest temperature being reported. Overtemperature is triggered at 150°C (typical), and it causes the TMON pin to be pulled high to V_{CC}. The overtemperature fault will be cleared once the internal temperature falls 20°C (typical) below the threshold.

TDIO pin is internally connected to the anode of a P/N junction diode while the cathode is connected to SGND. It provides an alternative measurement of die temperature for the controllers, such as LTC3884-1, to measure the die temperature using direct V_{BE} method or ΔV_{BE} method.

VOLTAGE FAULT CONDITIONS

When V_{CC} or PV_{CC} is in UVLO, or V_{IN} is in OVLO, SW will not respond to PWM and both top MOSFET and bottom MOSFET are off.

When BST-to-SW voltage is in UVLO, SW will not respond to a PWMHI until a PWMLO is provided such that BST-to-SW voltage is recharged sufficiently.

OVER CURRENT FAULT CONDITIONS

When the high side MOSFET is on, instantaneous SW current of >180 A (net current flowing out of SW) will trip the overcurrent (OC) comparator and set the internal OC state. When this happens, regardless of PWM pin state, the high side MOSFET will be turned off, and the low side MOSFET will be turned on until SW current decreases to 10 A, at which point OC state will be reset. Normal PWMHI-to-high-side-MOSFET and PWMLO-to-low-side-MOSFET operation resumes.

When the low side MOSFET is on, instantaneous SW current of <–90 A (net current flowing into SW) will trip the OCN comparator. When this happens, regardless of PWM pin state, the low side MOSFET will be turned off and the high side MOSFET will be turned on until SW current increase to –16 A, at which point OCN state will be reset. Normal PWMHI-to-high-side-MOSFET and PWMLO-to-low-side-MOSFET operation resumes. The trigger and reset of over current condition are illustrated in Figure 27.

In either OC or OCN condition, FLTB is pulled down.

THEORY OF OPERATION
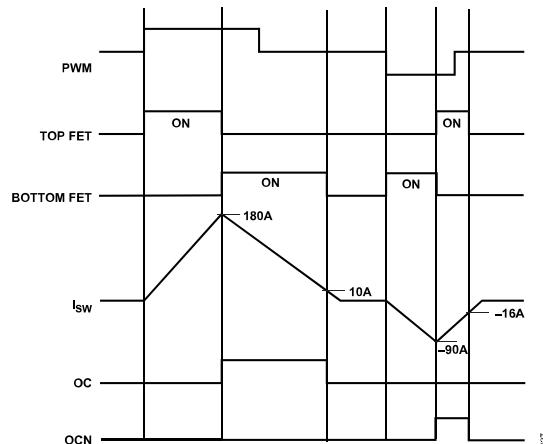
Figure 27. Over Current Conditions

ACTIVE DIODE MODE

If PWM goes from high to Hi-Z state while large (>10 A) currents are still flowing through the top MOSFET from V_{IN} to SW, the top at MOSFET will turn off and the bottom MOSFET will turn on to freewheel the current until it has been ramped down. If PWM goes from high to Hi-Z state while large (≥16 A) currents are still flowing through the top MOSFET from SW to V_{IN}, the top MOSFET will not turn off until the current has been ramped down.

Similarly, if PWM goes from low to Hi-Z state while large (≥16 A) currents are still flowing through the bottom MOSFET from SW to PGND, the bottom MOSFET will turn off, and the top MOSFET will turn on to freewheel the current until it has been ramped down. If PWM goes from low to Hi-Z state while large (>10 A) currents are still flowing through the bottom MOSFET from PGND to SW, the bottom MOSFET will not turn off until the current has been ramped down.

APPLICATIONS INFORMATION

POWER SEQUENCE

The LTC7051 requires the following input signals to operate normally: V_{IN}, V_{CC}/PV_{CC}, RUN, and PWM. Make sure that V_{IN} and V_{CC}/PV_{CC} are present and the RUN pin of LTC7051 is pulled up before enabling the PWM controller. Do not force RUN pin voltages above V_{CC} voltage.

FAULT MANAGEMENT

The fault management and shutdown mode of LTC7051 is summarized in Table 4. Connecting the open-drain output FLTB pin to the controller's RUN pin can prevent the controller from starting up and force the converter to restart once the LTC7051 runs into fault conditions, except BST-to-SW undervoltage fault.

Table 4. Fault Management and Shutdown Mode Summary

	FLTB	Respond to PWM	TMON
V_{IN} OVLO	Low	No, Both MOSFETs Off Until I_{SW} = 0	Report Temperature
V_{CC} UVLO	Low	No, Immediate Off	Floating
PV_{CC} UVLO	Low	No, MOSFETs Off Until I_{SW} = 0	Report Temperature
Positive OC	Low	No, Top MOSFET Immediate Off	Report Temperature
Negative OC	Low	No, Bottom MOSFET Immediate Off	Report Temperature
Overtemperature	Low	Yes	Pull Up to V_{CC}
BST-to-SW UV	High	Ignore PWMHI	Report Temperature
RUN Shutdown	Low	No, Both MOSFETs Off	Floating

CURRENT SENSE AND CURRENT LIMIT

I_{SNS} sources and sinks a current which is 1/100,000 of the SW current. According to the controller's maximum current sense signal range, select a proper resistor to convert the I_{SNS} current into a differential voltage signal reflecting the real-time SW current. The resistor should be biased at a low impedance common mode voltage, which has current sinking and sourcing capability. Make sure that at the maximum positive current and negative current, the I_{SNS} pin voltage is in the specified range so that the gain I_{SNS}/I_{SW} remains constant.

A general LTC7051 application circuit is shown in Figure 1. The LTC7051 is optimized for the application of high frequency high current voltage regulator. External component selection is largely driven by the load requirement and begins with the selection of the switching frequency f_{SW} and inductor L. Refer to Frequency Selection section and Inductor Selection section for the guidance. The I_{SNS} resistors are selected to set the current limit.

In high frequency high current applications, the switching spikes coupled to the I_{SNS} signal may result in a reading offset in heavy load range, but does not impact the ΔI_{SNS}/ΔI_{SW} gain. An optional resistor between I_{SNS} pin to GND can mitigate the offset. The resistor value R_{OS} is calculated by I_{SNS} pin voltage (referring to GND) divided by the offset current observed. The resistor value may

be different for a different switching frequency. This modification does not impact the internal overcurrent protection and negative overcurrent protection.
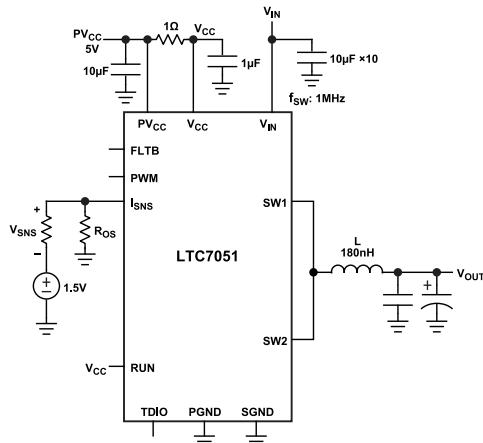

Figure 28.

FREQUENCY SELECTION

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. In the selection of switching frequency, make sure that the high side on-time at maximum input voltage is longer than LTC7051's minimum on-time, $t_{ON(MIN)}$, which is the smallest time duration that the LTC7051 is capable of turning on the top MOSFET. It is determined by internal timing delays, power stage timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit (see Equation 1).

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \times f_{SW}} \tag{1}$$

INPUT CAPACITORS

The LTC7051 should be connected to a V_{IN} supply through low impedance power planes. Ceramic input capacitors should be placed as close to the package as physically possible, with size and quantity appropriate for temperature rise with ripple current as calculated below.

For a buck converter, the switching duty cycle can be estimated by Equation 2.

$$D = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated by Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \times \sqrt{D \times (1 - D)} \tag{3}$$

where η is the estimated efficiency of the power section.

APPLICATIONS INFORMATION

INDUCTOR SELECTION

Given the desired input and output voltages, the inductor value and operating frequency, f_{SW}, directly determine the inductor's peak-to-peak ripple current (see Equation 4).

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times L}\right) \qquad (4)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to Equation 5.

$$L \geq \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times I_{RIPPLE}}\right) \times \frac{V_{OUT}}{V_{IN}} \qquad (5)$$

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

OUTPUT CAPACITORS

The LTC7051 is designed for high frequency switching and low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor, or ceramic capacitors. At 1 MHz, the typical output capacitance range is from 500 µF to 1000 µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required.

BYPASSING AND GROUNDING

The LTC7051 requires proper bypassing on the PV_{CC} and V_{CC} supplies due to its high speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot. Follow the following steps to obtain the optimum performance from the LTC7051.

▸ Mount the bypass capacitors as close as possible between the V_{CC} and SGND pins, and the PV_{CC} and PGND pins. The traces should be shortened as much as possible to reduce lead inductance.

▸ Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Any significant ground drop will degrade signal integrity.

▸ Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.

▸ Be sure to solder the Exposed Pad on the back side of the LTC7051 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in far greater thermal resistances.

PCB LAYOUT

Due to the LTC7051's high power density and high speed, high frequency operation, proper PCB layout and composition are critical to maximizing performance.

At a minimum, the PCB should be 4-layer with at least top and bottom layers 2 oz. copper. As much as possible, top and bottom layers should be continuous V_{IN} and PGND areas. At least one inner layer, preferably the second, should be a continuous PGND plane.

Copper-filled vias should be used under the package exposed pads to connect top and bottom PCB layers. $\theta_{JCbottom}$ is <1°C/W. Anything less than copper-filled vias will compromise θ_{JA} greatly.

The inductor pads should be placed as close as possible to the package, with traces as short and wide as possible. If possible, SW traces should be doubled up with the second layer, taking care not to couple to sensitive traces.

A recommended PCB layout is shown in Figure 29.

APPLICATIONS INFORMATION
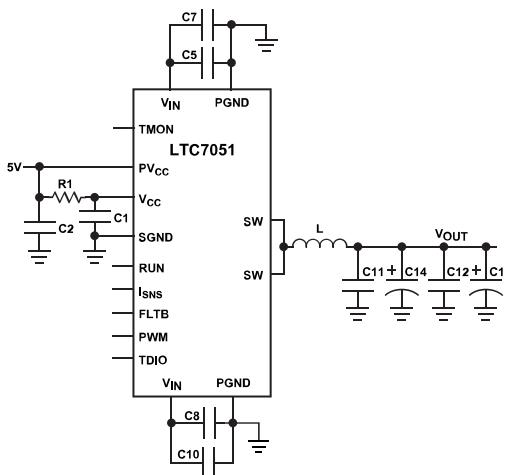
Figure 29. Schematic
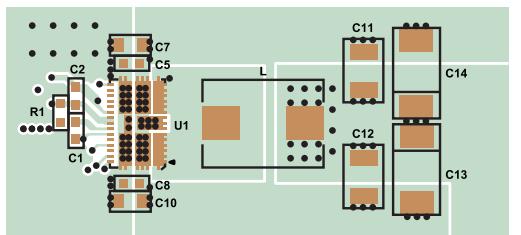
*Figure 30. Example PCB Layout*

TYPICAL APPLICATION
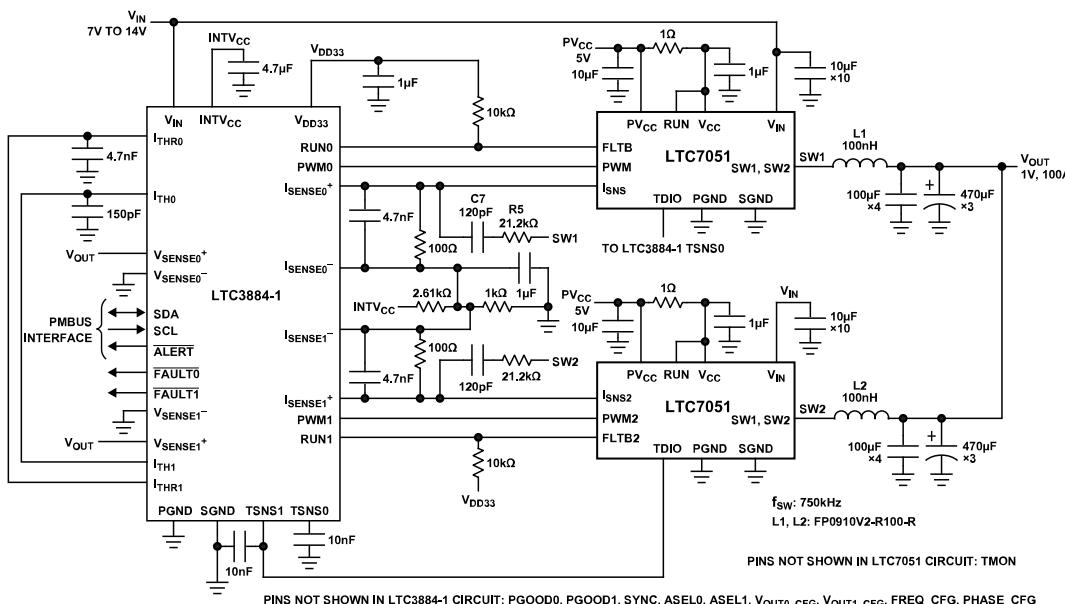
Figure 31. LTC7051 and LTC3884-1 Schematic

APPLICATIONS INFORMATION

Related Parts

Table 5.

Part Number	Description	Comments
LTC7051-1	SilentMOS Smart Power Stage in 5 mm × 8mm LQFN	140 A Peak Current, Silent Switcher 2 Architecture, V_{IN} Up to 16 V, 5 mm × 8mm LQFN Package
LTC7050	Dual SilentMOS Smart Power Stage in 5 mm × 8mm LQFN	70 A Peak Current per Channel, Silent Switcher 2 Architecture, V_{IN} Up to 14 V, 5 mm × 8mm LQFN Package
LTC7050-1	Dual SilentMOS Smart Power Stage in 5 mm × 8mm LQFN	70 A Peak Current Capable per Channel, Silent Switcher 2 Architecture, V_{IN} Up to 16 V, 5 mm × 8mm LQFN Package
LTC3888/LTC3888-1	Dual Output 8-Phase Step-Down DC/DC Controller with Digital Power System Management	4.5 V ≤ V_{IN} ≤ 26.5 V, 0.3 V ≤ V_{OUT} ≤ 3.45 V, I2C/PMBus, Programmable Loop Compensation, 5 mm × 8mm QFN-52
LTC3884/LTC3884-1	Dual Output PolyPhase Step-Down Controller with Sub-Milliohm DCR Sensing and Digital Power System Management	4.5 V ≤ V_{IN} ≤ 38 V, 0.5 V ≤ V_{OUT} ≤ 5.5 V, I2C/PMBus, Programmable Loop Compensation, 5 mm × 8mm QFN-52
LTC7851	Quad Output Multiphase Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with DrMOS, Power Blocks or External Drivers/MOSFETs, V_{IN} Range Depends on External Components, 4.5 V ≤ V_{CC} ≤ 5.5 V, 0.6 V ≤ V_{OUT} ≤ V_{CC} –0.5 V
LTC7852/LTC7252-1	Dual Output 6-Phase Current Mode Synchronous Buck Controller with Current Monitoring	Operates with DrMOS, Power Blocks, 0.5 V ≤ V_{OUT} ≤ 2 V, Hiccup Mode Overcurrent Protection, Flexible Phase Configuration
LTC3861	Dual, Multiphase Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with Power Blocks, DrMOS or External MOSFETs 3 V ≤ V_{IN} ≤ 24 V
LTC3882/LTC3882-1	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	3 V ≤ V_{IN} ≤ 38 V, 0.5 V ≤ $V_{OUT1,2}$ ≤ 5.25 V, ±0.5% V_{OUT} Accuracy I2C/PMBus Interface, uses DrMOS or Power Blocks
LTC3887/LTC3887-1	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management, 70 mS Start-Up	4.5 V ≤ V_{IN} ≤ 24 V, 0.5V ≤ $V_{OUT0,1}$ (±0.5%) ≤ 5.5 V, 70 mS Start-Up, I2C/PMBus Interface, –1 Version uses DrMOS or Power Blocks

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
05-08-1571	LQFN	42-Lead LQFN Package (Reference LTC DWG # 05-08-1571 Rev B)

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
LTC7051AV#PBF	−40°C to +125°C	42-Lead LQFN (8 mm × 5 mm × 0.95 mm w/ EP)	05-08-1571

[1] All models are RoHS compliant.

Updated: June 29, 2023