5.5V, 3A, Ultra-Low Noise, High PSRR, 85mV Dropout Ultra-Fast Linear Regulator

FEATURES

- **Ultra-low RMS Noise: 1.2μV_{RMS} (10Hz to 100kHz)**
- **Ultra-low Spot Noise: 3.5nV/√Hz at 10kHz**
- **Ultra-low 1/f Noise: 7μV_{P-P} from 0.1Hz to 10Hz**
- **High-Frequency PSRR: 50dB at 1MHz**
- **Ultra-fast Transient Response**
- **Dropout Voltage: 85mV Typical**
- **Digitally Programmable V_{OUT}: 0.5V to 4.2V**
- **Output Tolerance: ±1.5% Over Line, Load, and Temperature**
- Programmable Output Current Limit: ±10% at 3A
- Input Range: 0.6V to 5.5V
- Stable with Ceramic Output Capacitors (10μF Minimum)
- Parallel Multiple Devices for Higher Current
- Precision Enable/Undervoltage Lockout (UVLO)
- Power Good (PG) Flag
- 18-Lead (3mm × 3mm) LFCSP-RT Package

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- High Speed/High Precision Data Converters
- Low Noise Instrumentation
- Post-Regulator for Switching Supplies
- FPGA and DSP Power Supplies
- Medical Applications

GENERAL DESCRIPTION

The **LT®3077** is a low voltage, ultra-low noise, and ultra-fast transient response linear regulator. The device supplies up to 3A with a typical dropout voltage of 85mV. A 4.7μF reference bypass capacitor decreases output voltage noise to 1.2μV_{RMS}. The wide bandwidth and high PSRR permit the use of small ceramic capacitors, saving bulk capacitance and cost. The LT3077 is ideal for powering high-performance FPGAs, data converters, RF, and noise-sensitive signal chain applications.

The output voltage is digitally selectable in 50mV increments from 0.5V to 1.2V, 100mV increments from 1.2V to 1.8V, and discrete levels at 2V, 2.5V, 3V, 3.3V, and 4.2V. The LT3077's unity-gain operation provides virtually constant output noise, PSRR, and bandwidth independent of the programmed output voltage.

Precision current limiting allows users to minimize input power supply size and cost. Built-in protection includes UVLO, internal current limit, and thermal shutdown with hysteresis. The LT3077 is available in a compact 18-lead (3mm x 3mm) LFCSP-RT package.

SIMPLIFIED APPLICATION DIAGRAM

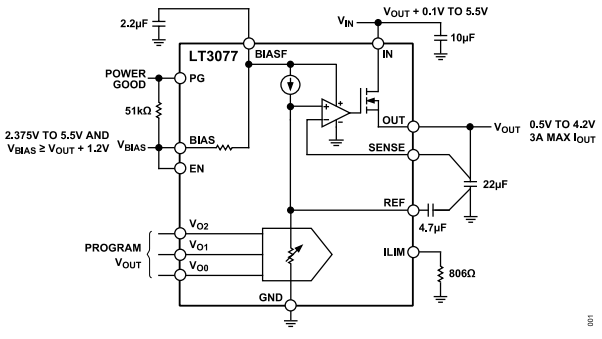

Figure 1. Simplified Application Diagram

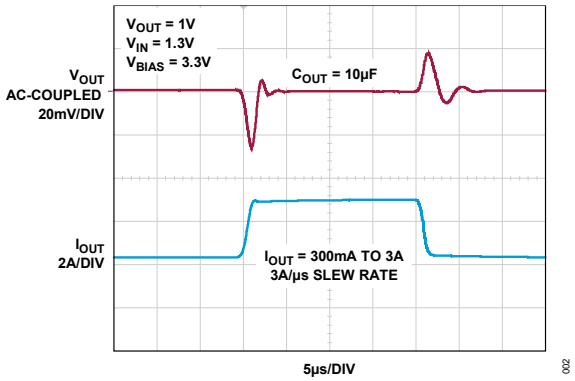

Figure 2. Transient Response

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SPECIFICATIONS

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(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{ILIM} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
IN Pin Voltage	V_{IN}	$V_{IN} \geq V_{OUT}$ + 190mV, I_{OUT} = 3A		0.6		5.5	V
BIAS Pin Voltage[1]	V_{BIAS}			2.375		5.5	V
Regulated Output Voltage	V_{OUT}	V_{OUT} = 0.5V, 50mA ≤ I_{OUT} ≤ 3A, 0.7V ≤ V_{IN} ≤ 0.9V		0.4925	0.500	0.5075	V
		V_{OUT} = 1.2V, 10mA ≤ I_{OUT} ≤ 3A, 1.4V ≤ V_{IN} ≤ 1.6V		1.182	1.200	1.218	
		V_{OUT} = 3.3V, 10mA ≤ I_{OUT} ≤ 3A, 3.5V ≤ V_{IN} ≤ 3.7V		3.2505	3.300	3.3495	
		V_{OUT} = 4.2V, 10mA ≤ I_{OUT} ≤ 3A, 4.4V ≤ V_{IN} ≤ 4.6V		4.137	4.200	4.263	
Line Regulation to V_{IN}	ΔV_{OUT} = $f(\Delta V_{IN})$	V_{OUT} = 0. 5V, ΔV_{IN} = 0.7V to 5.5V, V_{BIAS} = 2.375V, I_{OUT} = 50mA				0.5	mV
		V_{OUT} = 4.2V, ΔV_{IN} = 4.4V to 5.5V, V_{BIAS} = 5.5V, I_{OUT} = 10mA				0.6	
Line Regulation to V_{BIAS}	ΔV_{OUT} = $f(\Delta V_{BIAS})$	V_{OUT} = 0.5V, ΔV_{BIAS} = 2.375V to 5.5V, V_{IN} = 0.7V, I_{OUT} = 50mA				0.25	mV
		V_{OUT} = 3.3V, ΔV_{BIAS} = 4.5V to 5.5V, V_{IN} = 3.5V, I_{OUT} = 10mA				2	
Load Regulation[1]	ΔV_{OUT} = $f(\Delta I_{OUT})$	ΔI_{OUT} = 50mA to 3A	V_{BIAS} = 2.375V, V_{IN} = 0.7V, V_{OUT} = 0.5V			0.6	mV
		ΔI_{OUT} = 10mA to 3A	V_{BIAS} = 2.4V, V_{IN} = 1.4V, V_{OUT} = 1.2V			1.2	
			V_{BIAS} = 4.5V, V_{IN} = 3.5V, V_{OUT} = 3.3V			3.3	
			V_{BIAS} = 5.4V, V_{IN} = 4.4V, V_{OUT} = 4.2V			4.2	

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{ILIM} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Dropout Voltage[2]	V_{DO}	$V_{IN} = V_{OUT(NOMINAL)}$, $V_{BIAS} \geq V_{OUT} + 1.2V$, I_{OUT} = 1A	T_J = 25°C		30	44	mV
						65	
		$V_{IN} = V_{OUT(NOMINAL)}$, $V_{BIAS} \geq V_{OUT} + 1.2V$, I_{OUT} = 2A	T_J = 25°C		60	85	
						130	
		$V_{IN} = V_{OUT(NOMINAL)}$, $V_{BIAS} \geq V_{OUT} + 1.2V$, I_{OUT} = 3A	T_J = 25°C		85	105	
						190	
Minimum Load Current	$I_{OUT(MIN)}$	$V_{OUT} \geq 0.8V$				10	mA
		$V_{OUT} < 0.8V$				50	
Ground Pin Current	I_{GND}	V_{BIAS} = 5.5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, I_{OUT} = 10mA			4.3	6.5	mA
		V_{BIAS} = 5.5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, I_{OUT} = 3A			5.2	7	
BIAS Pin Current	I_{BIAS}	V_{IN} = 1.5V, V_{OUT} = 1.2V, V_{BIAS} = 3.3V, I_{OUT} = 10mA			4.3	6.5	mA
		V_{IN} = 1.5V, V_{OUT} = 1.2V, V_{BIAS} = 3.3V, I_{OUT} = 3A			5.8	8	
BIAS Pin Current in Dropout[2]	I_{BIAS_DO}	$V_{BIAS} = V_{OUT}$ +1.2V, $V_{IN} = V_{OUT(NOMINAL)}$, I_{OUT} = 3A			5.4	7.5	mA
		V_{BIAS} = 5.5V, $V_{IN} = V_{OUT(NOMINAL)}$, I_{OUT} = 3A			35	50	
BIAS Pin Nap Mode Current	I_{BIAS_NAP}	V_{BIAS} = 5.5V, EN = 0V				10	µA
IN Pin Nap Mode Current	I_{IN_NAP}	V_{IN} = 5.5V, EN = 0V			20	170	µA
I_{OUT}/I_{LIM} Ratio		I_{OUT} = 3A, $V_{IN} - V_{OUT}$ = 0.2V		3000			
		I_{OUT} = 1A, $V_{IN} - V_{OUT}$ = 0.2V		3000			
ILIM Shutdown Current		V_{BIAS} = 5.0V, EN = 0V				5	µA

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{ILIM} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Programmable Current Limit[3]	$I_{LIM(P)}$	R_{ILIM} = 1kΩ	2.7	3.0	3.3	A
		R_{ILIM} = 3kΩ	0.85	1.0	1.16	
Internal Current Limit[3]	$I_{LIM(I)}$	V_{IN} = 1.5V, ΔV_{OUT} = -5%, V_{BIAS} = 5.5V	3.3	4.5	5.5	A
V_{OUT} Threshold for Power Good		Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Rising	91	93	95	%
		Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Falling	88	90	92	
PG V_{OL}		I_{PG} = 200µA (Fault Condition)		60	100	mV
PG V_{OH} Leakage		V_{PG} = V_{BIAS} = 5V			1	µA
Fast Start-Up REF Pin Current				2		mA
Fast Start-Up Turn Off Threshold		Measured as percentage of nominal REF pin voltage	96	98.8	101.5	%
Thermal Shutdown		T_J Rising		168		°C
		Hysteresis		7		
V_{BIAS} Undervoltage Lockout		EN = V_{BIAS}, V_{IN} = 0V, V_{OUT} = 0V, V_{BIAS} Rising	2.16	2.2	2.24	V
		EN = V_{BIAS}, V_{IN} = 0V, V_{OUT} = 0V, V_{BIAS} Falling	2.03	2.07	2.11	
V_{IN} Undervoltage Lockout		V_{IN} Rising	450	462.5	475	mV
		V_{IN} Falling	400	412.5	425	
V_{IL} Input Threshold (Logic-0 State) V_{O0}, V_{O1}, V_{O2}		Input Falling	0.3			V
V_{IZ} Input Range (Logic-Z State) V_{O0}, V_{O1}, V_{O2}			0.95		1.15	V
V_{IH} Input Threshold (Logic-1 State) V_{O0}, V_{O1}, V_{O2}		Input Rising			1.97	V

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{ILIM} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Input Hysteresis V_{O0}, V_{O1}, V_{O2}		Rising and Falling			80		mV
Input Pin Sink Current V_{O0}, V_{O1}, V_{O2}		V_{IN} = 2.5V, V_{BIAS} = 2.375V, V_{EN} = 0V				50	µA
EN Pin Threshold		EN Trip Point Rising (Turn-On), V_{BIAS} = 2.375V		1.20	1.26	1.32	V
EN Pin Hysteresis		EN Trip Point Hysteresis, V_{BIAS} = 2.375V			80		mV
EN Pin Current	I_{EN}	V_{EN} = 0V, V_{BIAS} = 5.5V				±1	µA
		V_{EN} = 1.3V, V_{BIAS} = 5.5V			0.5		
		V_{EN} = 5.5V, V_{BIAS} = 0V			10	20	
V_{BIAS} Ripple Rejection	$PSRR_{BIAS}$	V_{BIAS} = 2.7V(Avg), V_{IN} = 1.5V, V_{OUT} = 1.2V	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{OUT} = 3A		106		dB
			V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 1MHz, I_{OUT} = 3A		70		
V_{IN} Ripple Rejection	$PSRR_{IN}$	V_{BIAS} = 5V, V_{IN} =1.5V(Avg), V_{OUT} = 1.2V	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 120Hz, I_{OUT} = 3A		96		dB
			V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{OUT} = 3A		50		
Output RMS Noise[4]	$V_{RMS(OUT)}$	V_{OUT} = 1V, I_{OUT} = 3A, V_{IN} = 1.3V, V_{BIAS} = 3.3V, C_{OUT} = 22µF	BW = 10Hz to 100kHz, C_{REF} = 4.7µF		1.2		$µV_{RMS}$
			BW = 10Hz to 100kHz, C_{REF} = 0.47µF		1.6		

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{ILIM} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Output Noise Spectral Density[4]	$V_{n(OUT)}$	V_{OUT} = 1V, I_{OUT} = 3A, V_{IN} = 1.3V, V_{BIAS} = 3.3V, C_{OUT} = 22µF	Frequency = 0.1Hz, C_{REF} = 4.7µF		2.5		µV/√Hz
			Frequency = 10Hz, C_{REF} = 4.7µF		40		nV/√Hz
			Frequency = 10Hz, C_{REF} = 0.47µF		650		
			Frequency = 10kHz, C_{REF} = 4.7µF		3.5		
			Frequency = 10kHz, C_{REF} = 0.47µF		3.5		
			Frequency = 100kHz, C_{REF} = 4.7µF		3.8		
			Frequency = 100kHz, C_{REF} = 0.47µF		3.8		

1 To maintain proper performance and regulation, the BIAS supply voltage must satisfy the following conditions: 2.375V ≤ V_{BIAS} ≤ 5.5V and V_{BIAS} ≥ (V_{OUT} + 1.2V).

2 Dropout voltage, V_{DO}, is the minimum input-to-output voltage differential at a specified output current. In dropout, the output voltage equals V_{IN} – V_{DO}.

3 Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply to all possible input and output current combinations. When operating at maximum output current, limit the input voltage range to V_{IN} ≤ V_{OUT} + 600mV.

4 Adding a capacitor at the REF pin decreases output voltage noise. Adding this capacitor bypasses the REF pin internal resistor's thermal noise and the reference current's noise. The output noise then equals the error amplifier noise. The use of a REF pin bypass capacitor also increases start-up time.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute maximum ratings

PARAMETER	RATING
IN Pin Voltage[1]	-0.3V to 6V
OUT Pin Voltage[1]	-0.3V to 6V
SENSE Pin Voltage[1]	-0.3V to 6V
BIAS, BIASF Pin Voltage[1]	-0.3V to 6V
V_{O0}, V_{O1}, V_{O2} Pin Voltage[1]	-0.3V to 5.5V
EN Pin Voltage[1]	-0.3V to 6V
ILIM Pin Voltage[1]	-0.3V to 6V
PG Pin Voltage[1]	-0.3V to 6V
REF Pin Voltage[1]	-0.3V to 6V
Output Short-Circuit Duration	Indefinite
Operating Junction Temperature[2]	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Maximum Reflow (Package Body) Temperature	260°C

[1] Parasitic diodes exist internally between IN, OUT, SENSE, BIAS, BIASF, V_{O0}, V_{O1}, V_{O2}, EN, ILIM, PG, REF pins, and GND. Do not drive these pins more than 0.3V below the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

[2] The LT3077A is tested and specified under pulse load conditions such that $T_J \approx T_A$ (ambient temperature). The LT3077A is tested at T_A = 25°C. Performance of the LT3077A over the full –40°C to 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3077A is guaranteed over the full –40°C to 125°C operating junction temperature range.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Therefore, close attention to PCB thermal design is required.

Table 3. Thermal Resistance

PACKAGE TYPE[1]	θ_{JA}	$\theta_{JC\ TOP}$	$\theta_{JC\ BOT}$	UNIT
18-Lead 3mm x 3mm LFCSP-RT	44	58	8	°C/W

[1] θ values are determined per JESD51 conditions.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001 Charged Device Model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 4. LT3077, 18-Lead 3mm x 3mm LFCSP-RT

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	2000	2
CDM	1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

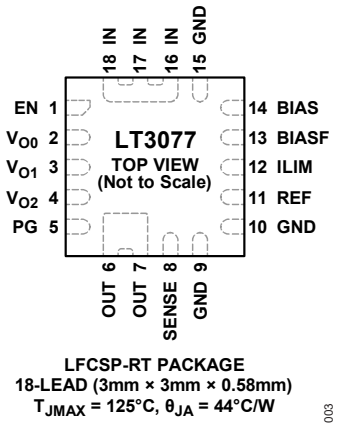


Figure 3. Pin Configuration

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1	EN	Device Enable. EN pin enables/disables the output. The LT3077 typically turns on when the EN voltage exceeds 1.26V on the rising edge, with an 80mV hysteresis on its falling edge. Pulling this pin low pulls down the reference, disables the output transistor, and disables auxiliary functions. Alternatively, the EN pin can set a BIAS-supply UVLO threshold by using a resistor-divider between BIAS, EN, and GND. If unused, connect EN to BIAS. Do not float the EN pin.
2, 3, 4	V_{O0}, V_{O1}, V_{O2}	Output Voltage Select. These tri-level pins combine to select a nominal output voltage from 0.5V to 4.2V. The input logic low threshold is less than 300mV referenced to GND, and the logic high threshold is greater than 1.97V referenced to GND. The range between 0.95V and 1.15V defines the logic Hi-Z state. See *Table 6* in the *Applications Information* section that defines the V_{OUT} versus V_{O0}, V_{O1}, and V_{O2} settings.
5	PG	Power Good. The PG pin is an open-drain NMOS output that actively pulls low if EN is low or if any one of these fault modes is detected: ▶ V_{OUT} is less than 93% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}. ▶ V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the falling edge of V_{OUT}. ▶ V_{BIAS} is less than its undervoltage lockout threshold. ▶ The OUT-over-IN voltage detector activates.
6, 7	OUT	Output. The exposed pad consisting of pins 6-7 of the LFCSP-RT package is the electrical connection to OUT. These pins supply power to the load. Connect the entire OUT exposed pad consisting of pins 6-7 for proper electrical and thermal performance. A minimum output capacitance of 10µF is required for stability. ADI recommends low ESR, X5R or X7R dielectric ceramic capacitors for best performance. Large load transient applications require larger output capacitors to limit peak voltage transients.

8	SENSE	Kelvin Sense for OUT. The SENSE pin is the inverting input to the error amplifier. Optimum regulation is obtained when the SENSE pin is connected to the OUT pins of the regulator. However, in critical applications, the resistance of PCB traces between the regulator and the load causes small voltage drops, creating a load regulation error at the point of load. Connecting the SENSE pin to the load instead of directly to OUT eliminates this voltage error.
9, 10, 15	GND	Ground. To ensure proper electrical and thermal performance, connect all GND pins of the package to the PCB ground.
11	REF	Reference Filter. Bypassing the REF pin to GND with a 4.7µF capacitor decreases output voltage noise and provides a soft-start function to the reference. ADI recommends the use of a high-quality, low-leakage capacitor.
12	ILIM	Programmable Current Limit. The ILIM pin sources a current typically equal to $I_{OUT}/3000$. As a result, the current limit programming factor is $3A \times k\Omega/R_{ILIM}$, where R_{ILIM} is the resistor from ILIM to GND.
13	BIASF	Bias Filter Pin. The LT3077 requires a minimum 2.2µF bypass capacitor on this pin.
14	BIAS	Bias Supply. This pin supplies current to the internal control circuitry and the output stage, driving the pass transistor. This pin doesn't require any bypass capacitor. To ensure proper operation, the BIAS voltage must satisfy the following conditions: $2.375V \le V_{BIAS} \le 5.5V$ and $V_{BIAS} \ge 1.2 + V_{OUT}$.
16, 17, 18	IN	Input Supply. The exposed pad consisting of pins 16-18 of the LFCSP-RT package are the electrical connection to IN. These pins supply power to the high-current pass transistor. Connect the entire IN exposed pad consisting of pins 16-18 for proper electrical and thermal performance. The LT3077 requires a bypass capacitor at IN to maintain stability and low input impedance over frequency. A 10µF input bypass capacitor suffices for most battery and power plane impedances. Minimizing input trace inductance optimizes performance. Applications with low V_{IN}-V_{OUT} differential voltage and large, fast load transients may require much higher input capacitor to prevent the input supply from drooping and allow the regulator to enter dropout.

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

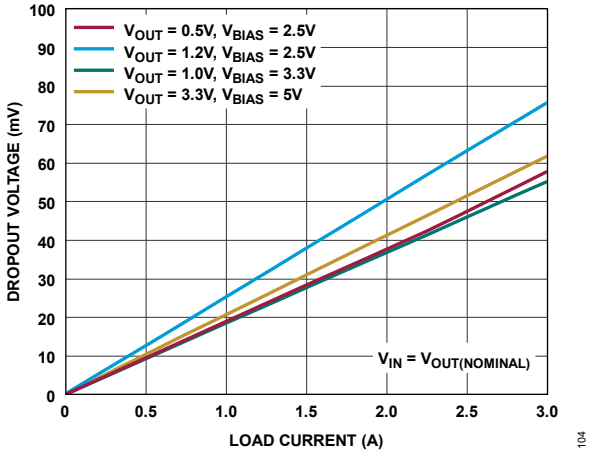


Figure 4. Dropout Voltage vs. Load

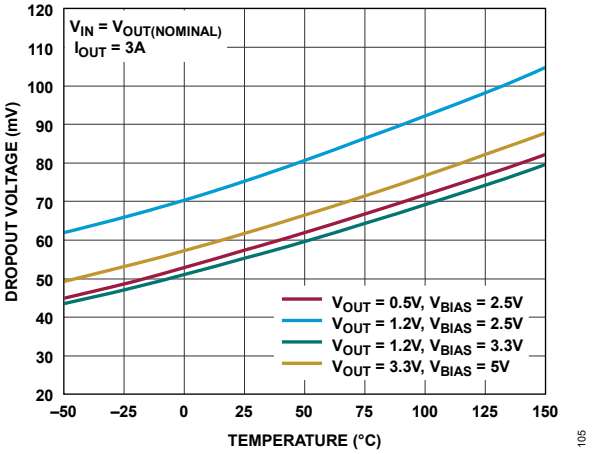


Figure 5. Dropout Voltage (3A)

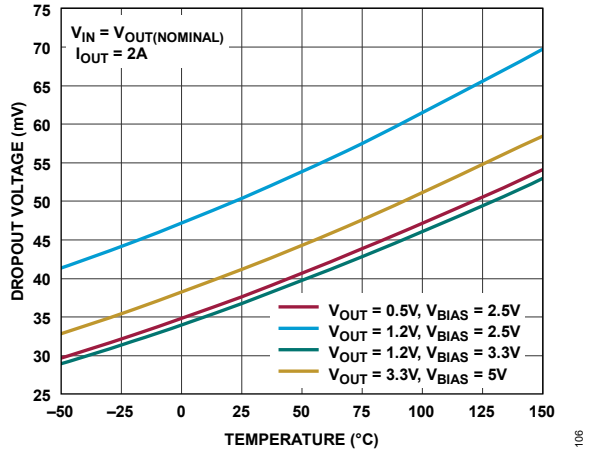


Figure 6. Dropout Voltage (2A)

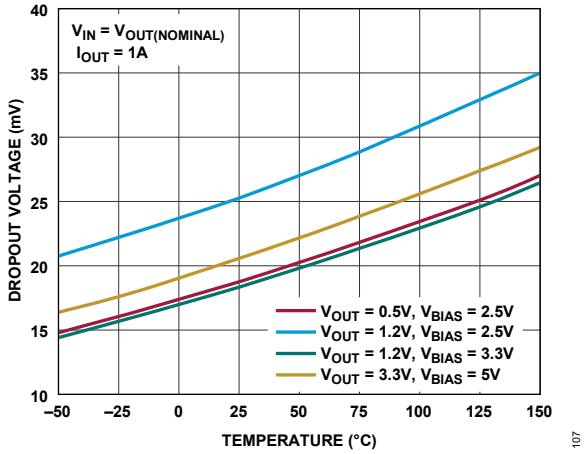


Figure 7. Dropout Voltage (1A)

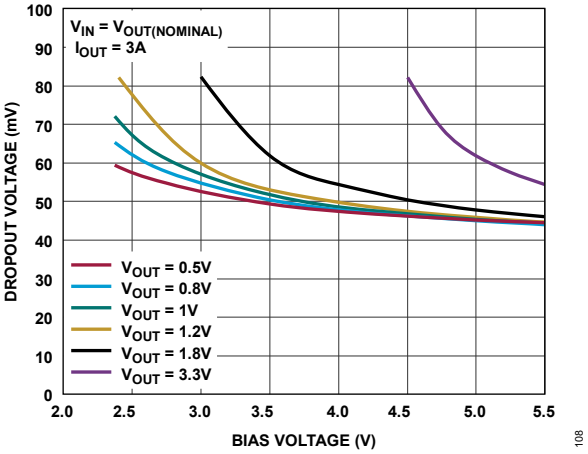


Figure 8. Dropout Voltage vs. V_{BIAS}

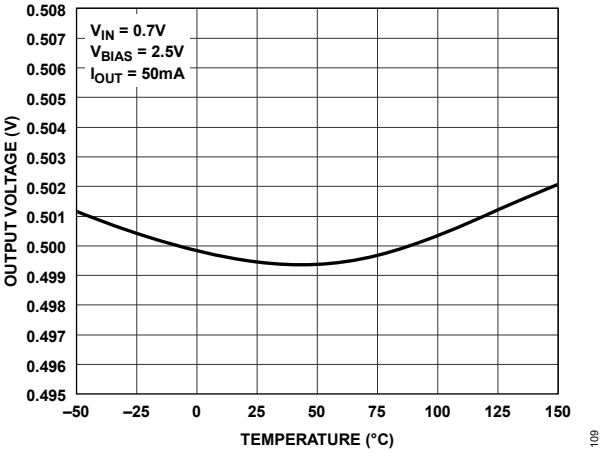


Figure 9. Output Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

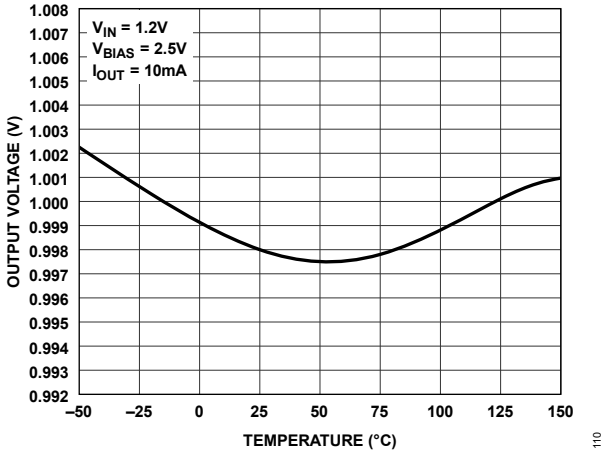


Figure 10. Output Voltage

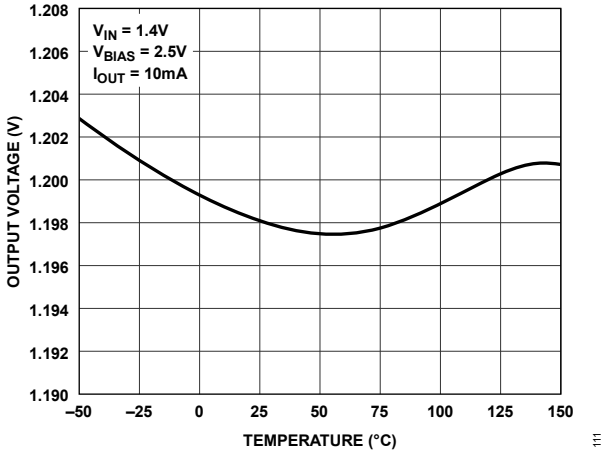


Figure 11. Output Voltage

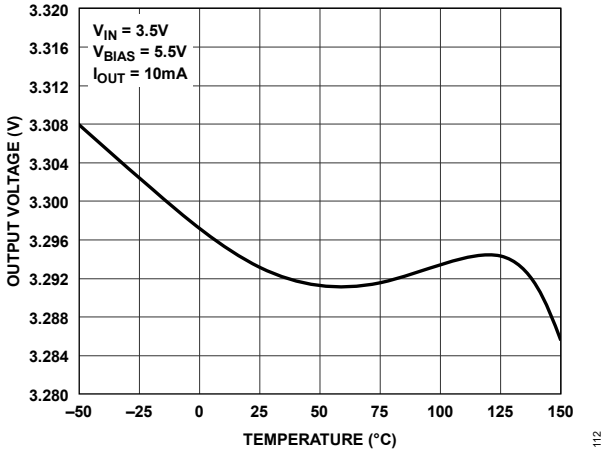


Figure 12. Output Voltage

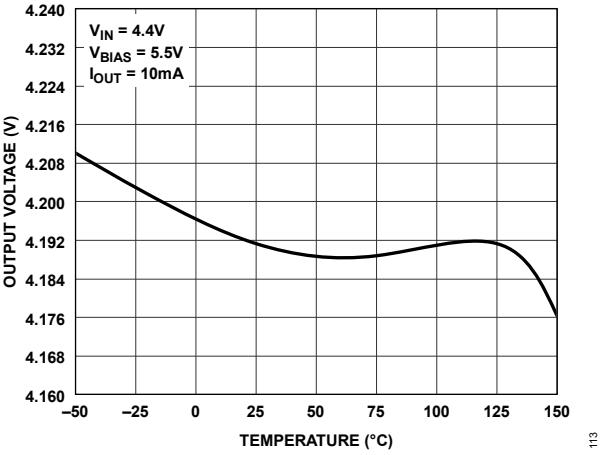


Figure 13. Output Voltage

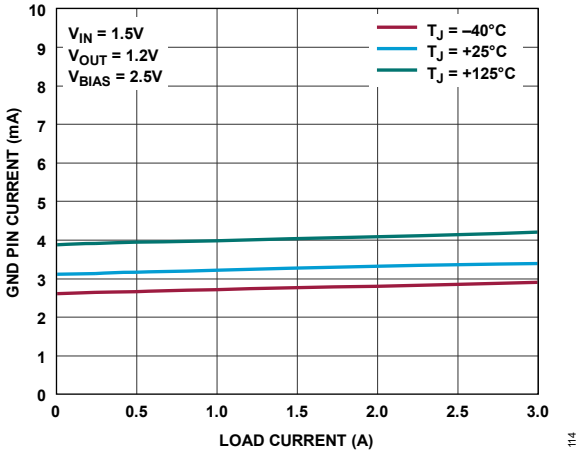


Figure 14. GND Pin Current

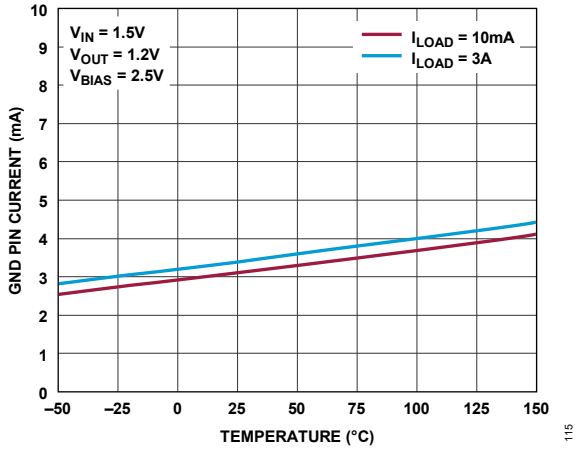


Figure 15. GND Pin Current

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

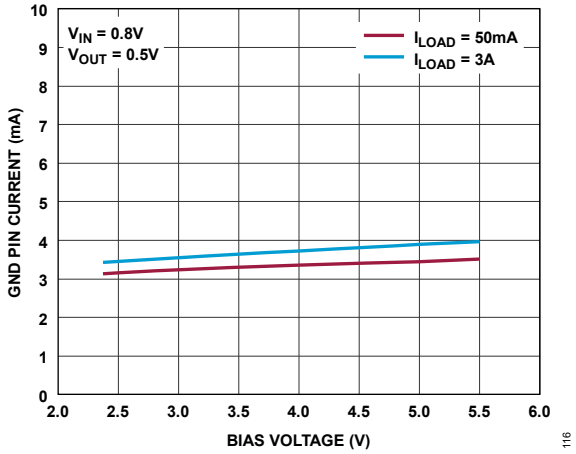


Figure 16. GND Pin Current

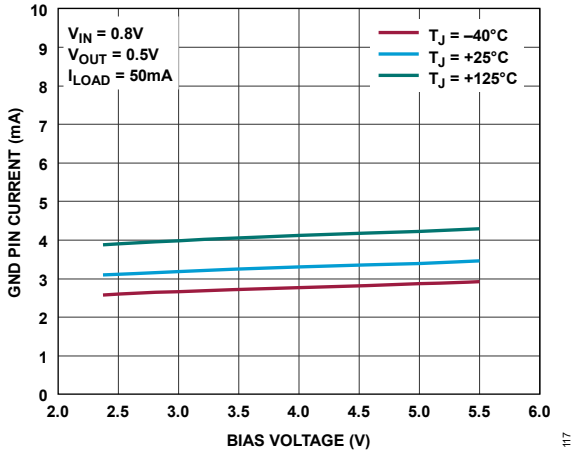


Figure 17. GND Pin Current

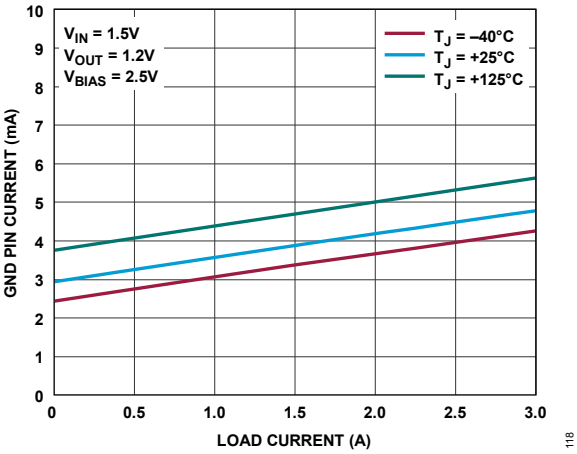


Figure 18. BIAS Pin Current

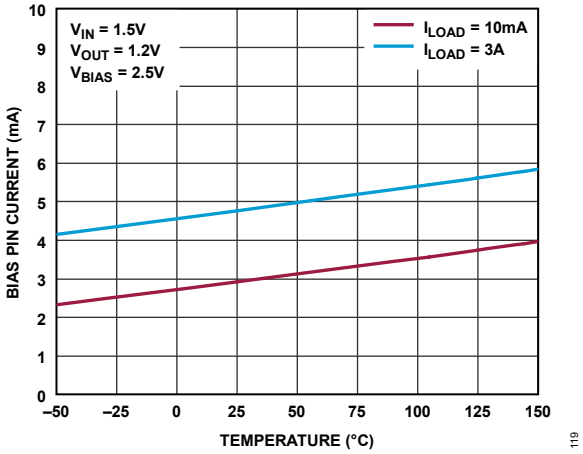


Figure 19. BIAS Pin Current

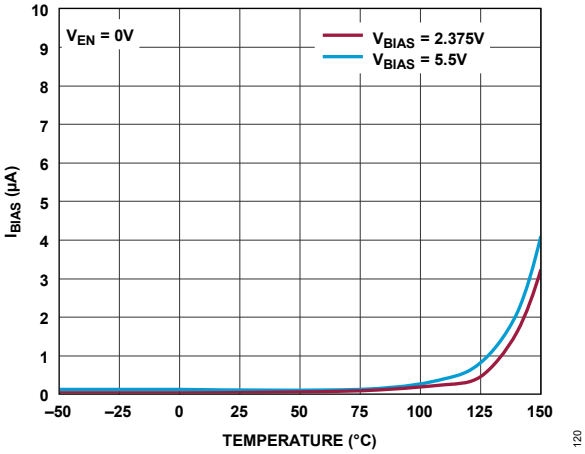


Figure 20. BIAS Pin Current in Nap Mode

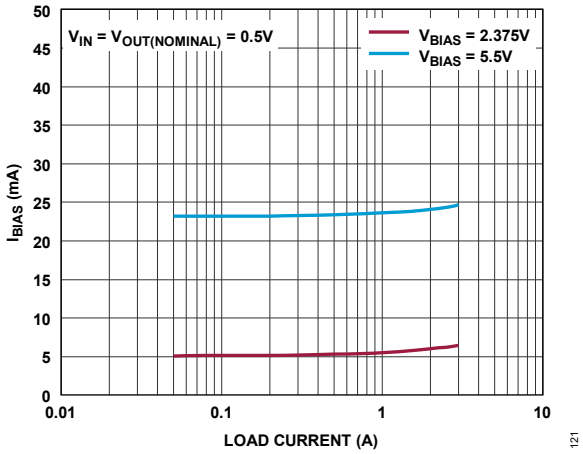


Figure 21. BIAS Pin Current in Dropout

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

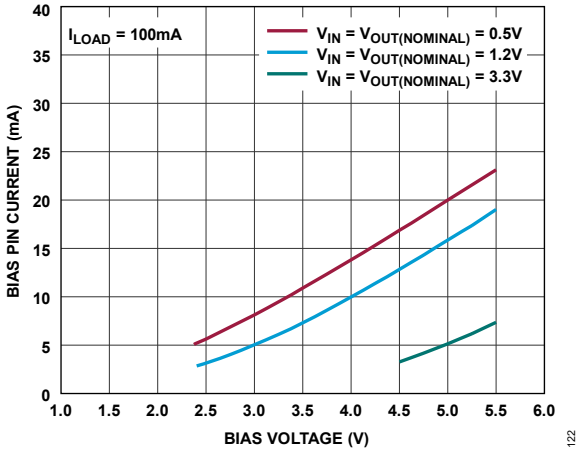


Figure 22. BIAS Pin Current in Dropout

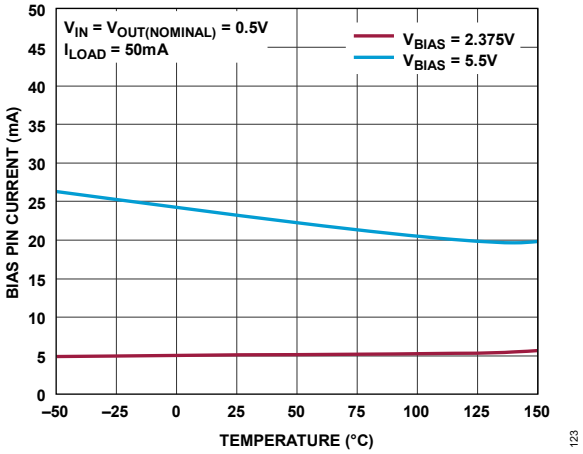


Figure 23. BIAS Pin Current in Dropout

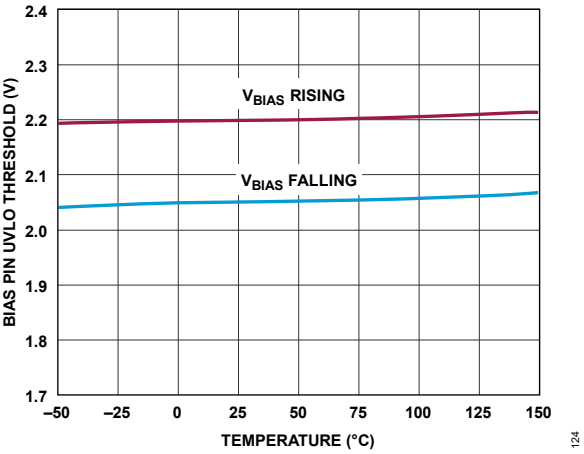


Figure 24. BIAS Pin UVLO Threshold

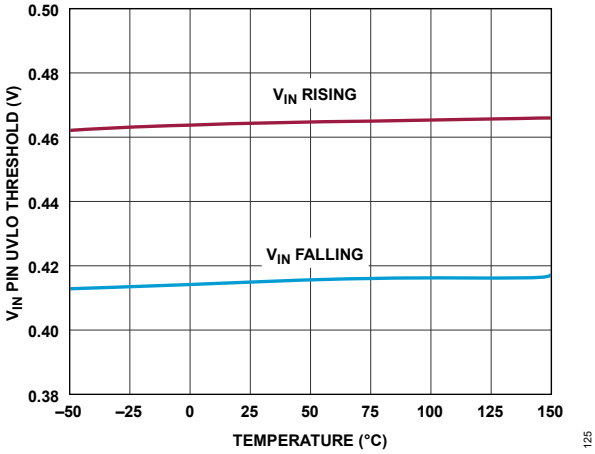


Figure 25. V_{IN} Pin UVLO Threshold

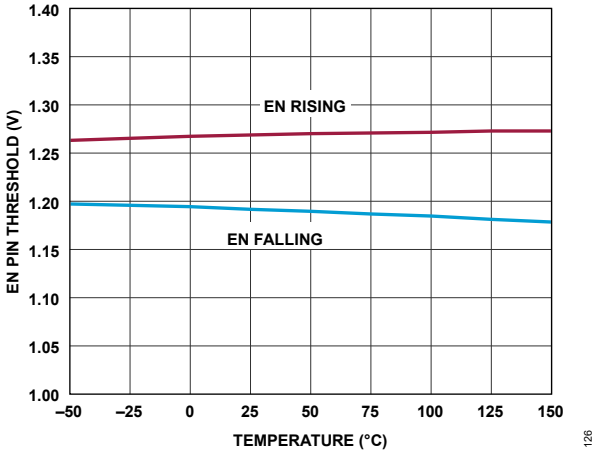


Figure 26. EN Pin Threshold

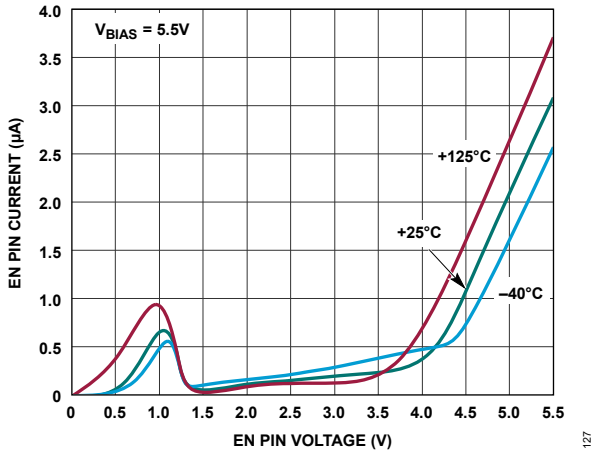


Figure 27. EN Pin Current

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

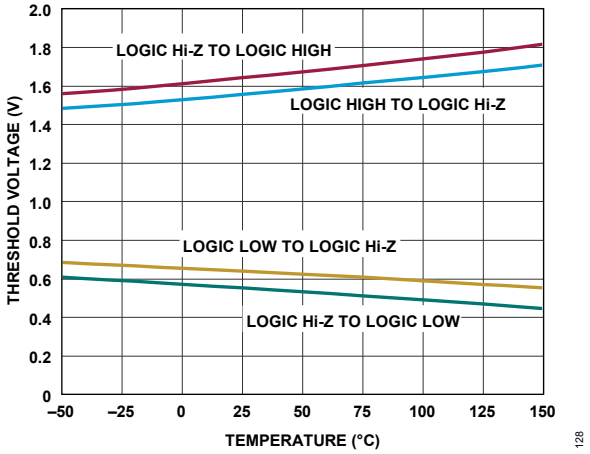


Figure 28. V_{00}, V_{01}, V_{02} Pin Threshold

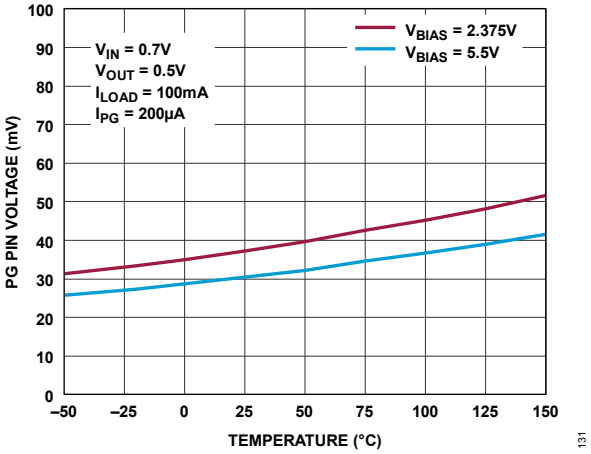


Figure 31. PG Pin Low Voltage

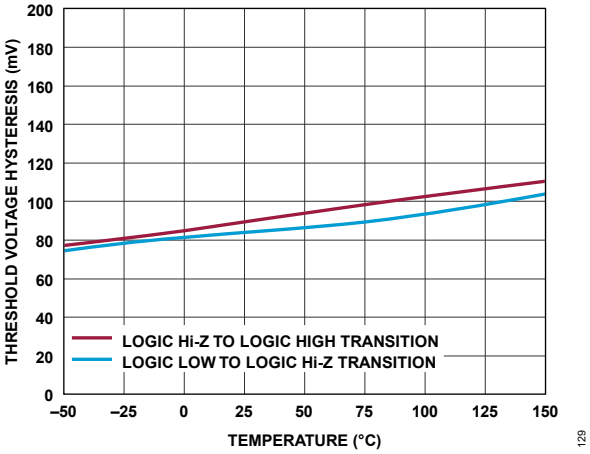


Figure 29. V_{00}, V_{01}, V_{02} Pin Hysteresis

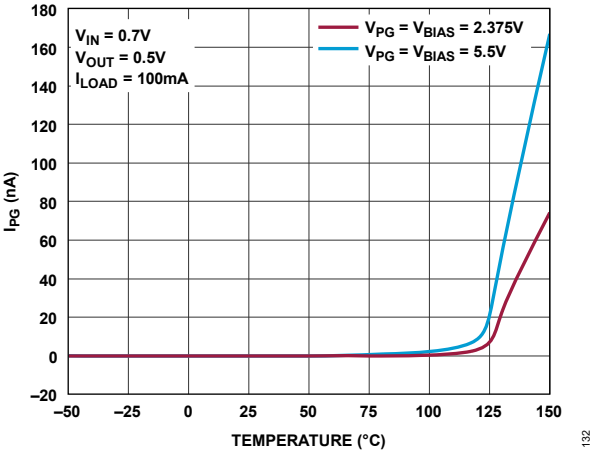


Figure 32. PG Pin Leakage Current

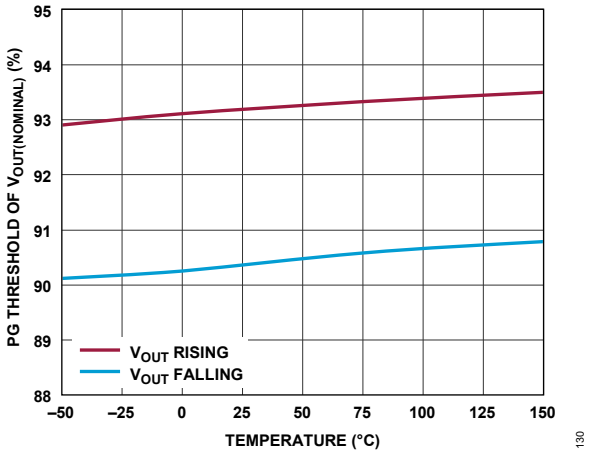


Figure 30. Power Good Threshold

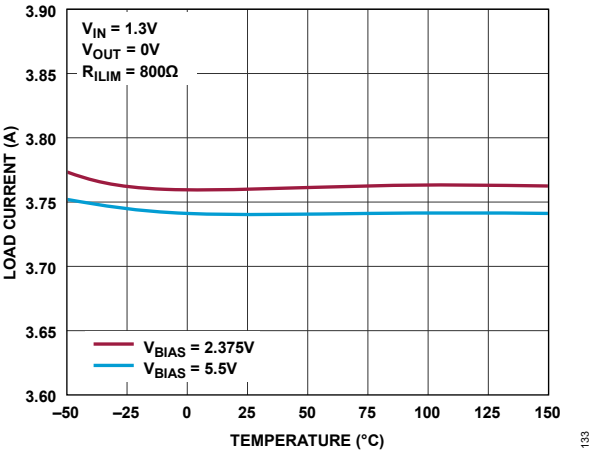


Figure 33. External Current Limit (3.75A)

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

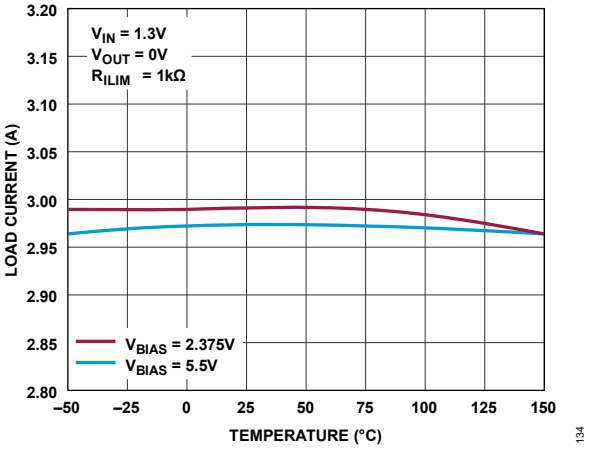


Figure 34. External Current Limit (3A)

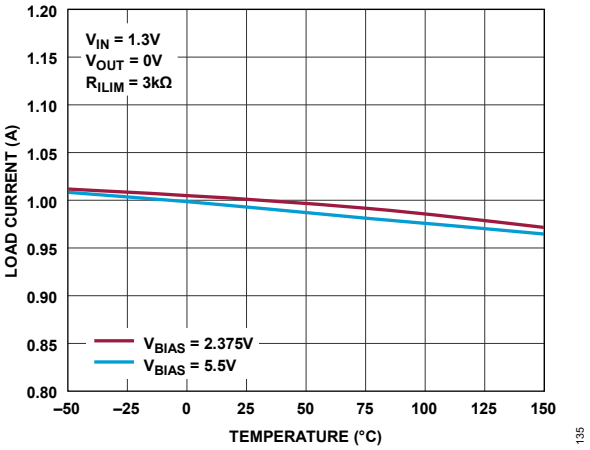


Figure 35. External Current Limit (1A)

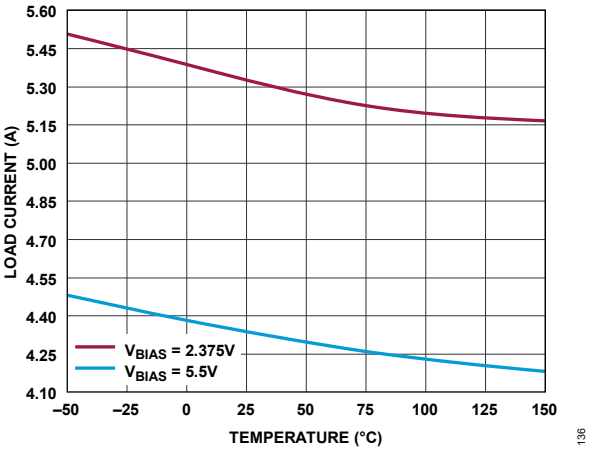


Figure 36. Internal Current Limit

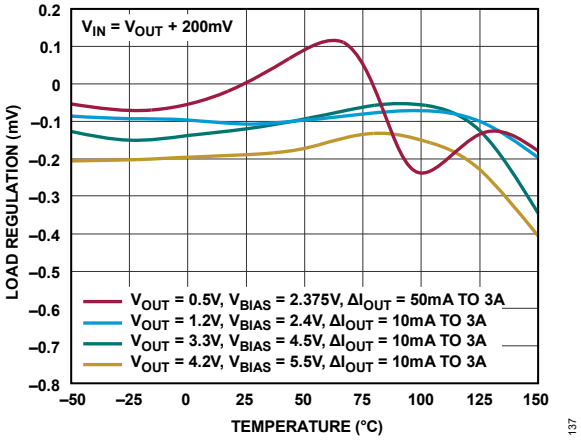


Figure 37. Load Regulation

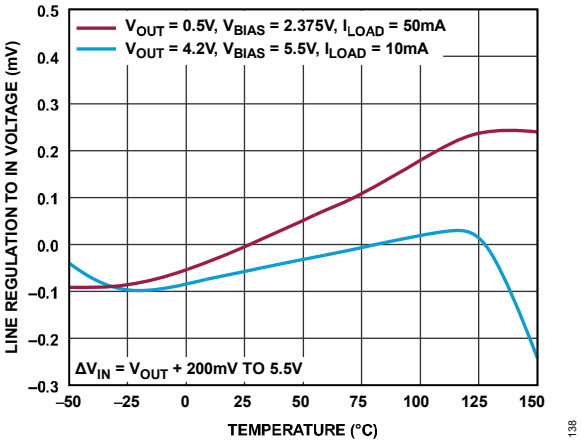


Figure 38. V_{IN} Line Regulation

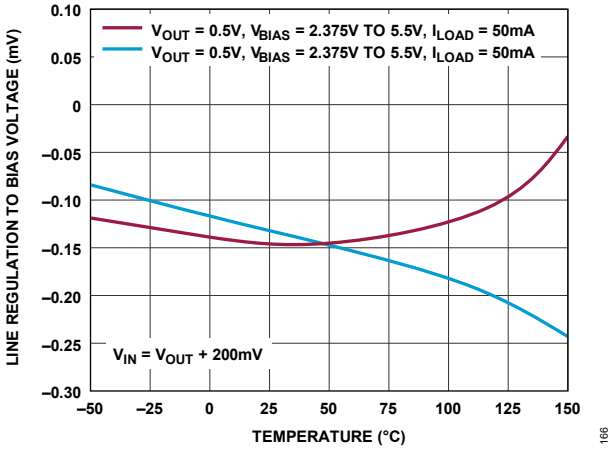


Figure 39. V_{BIAS} Line Regulation

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

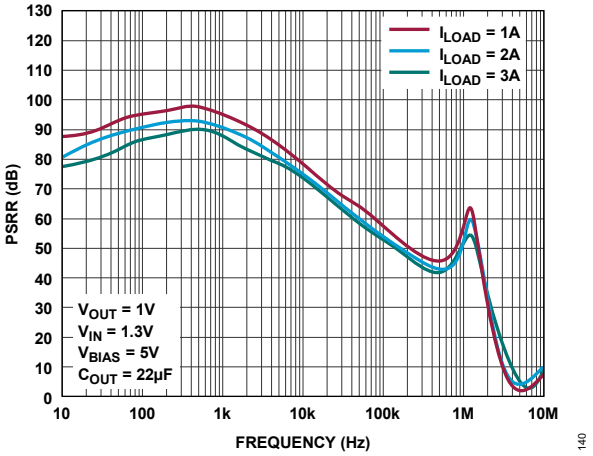


Figure 40. IN PSRR

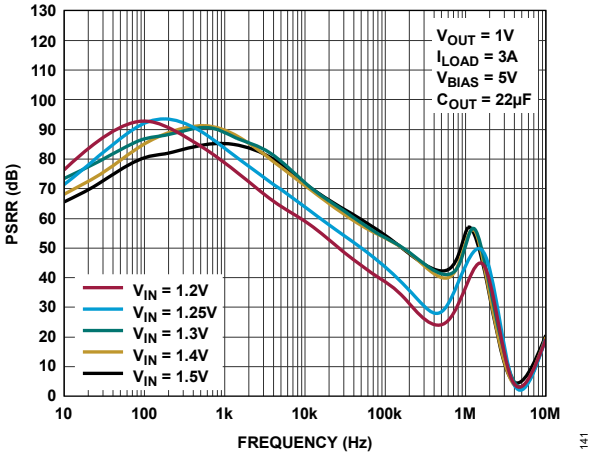


Figure 41. IN PSRR

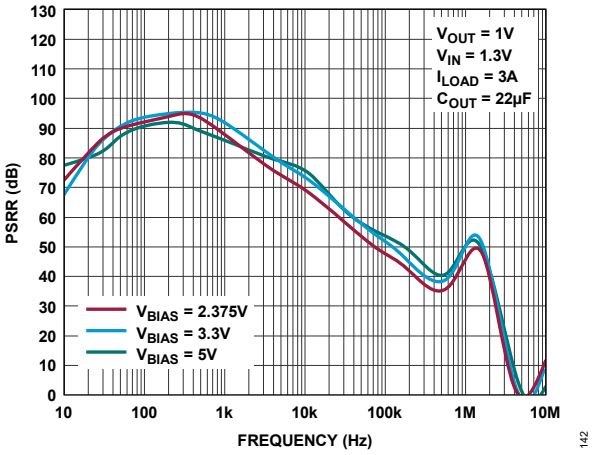


Figure 42. IN PSRR

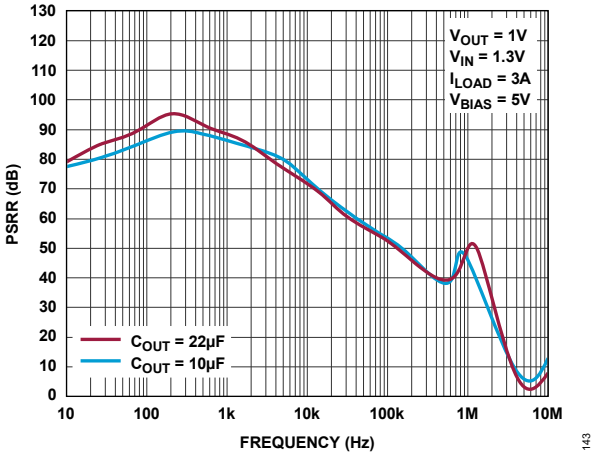


Figure 43. IN PSRR

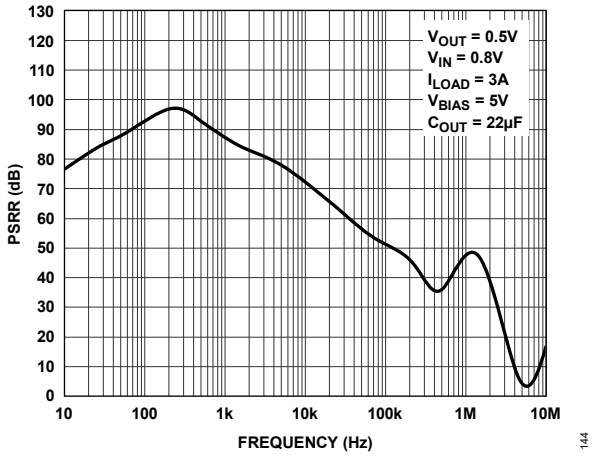


Figure 44. IN PSRR

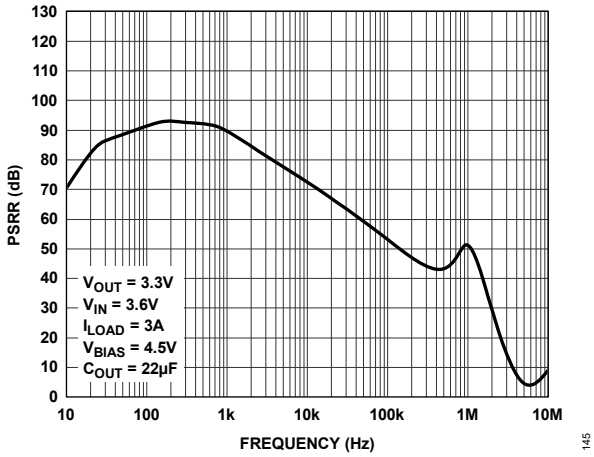


Figure 45. IN PSRR

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

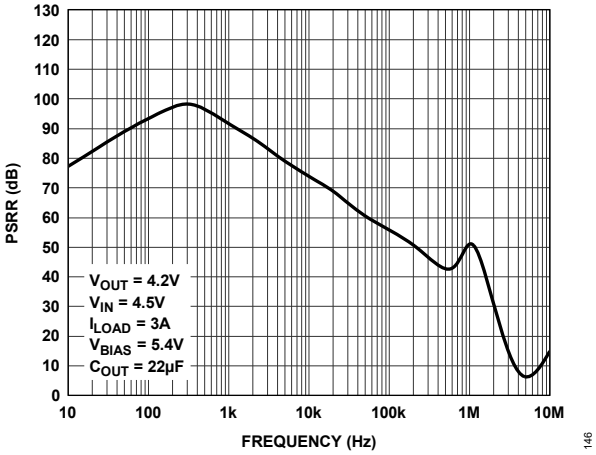


Figure 46. IN PSRR

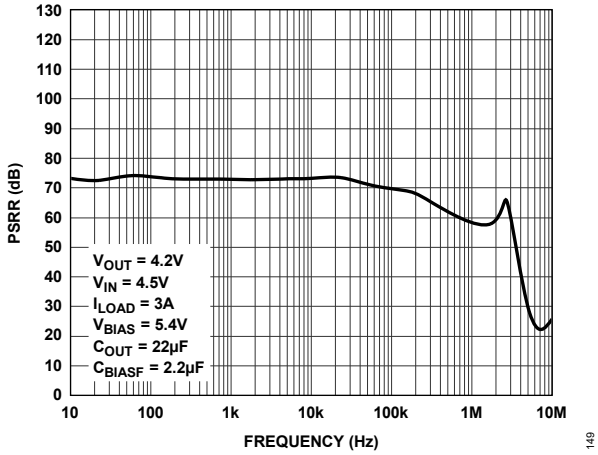


Figure 49. BIAS PSRR

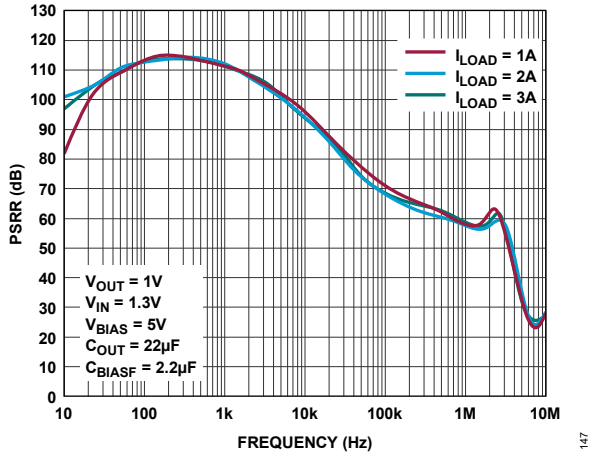


Figure 47. BIAS PSRR

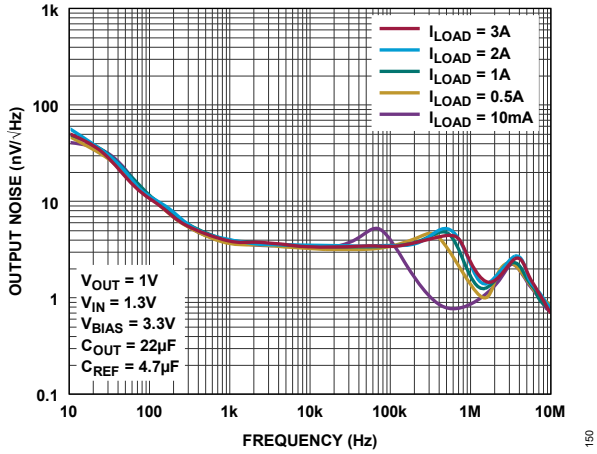


Figure 50. Noise Spectral Density

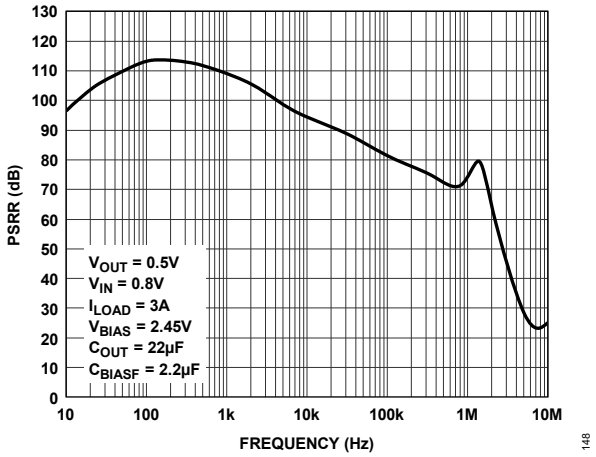


Figure 48. BIAS PSRR

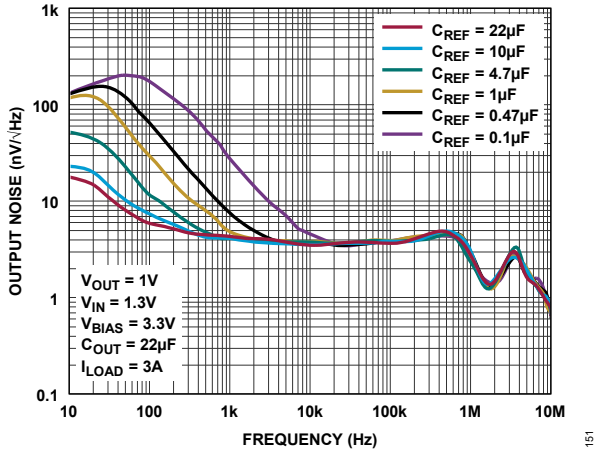


Figure 51. Noise Spectral Density

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

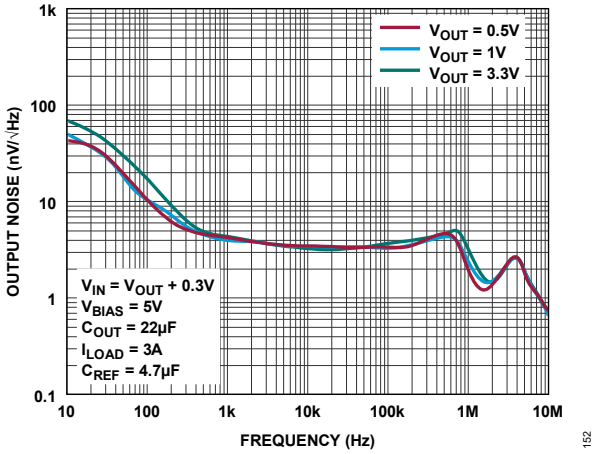


Figure 52. Noise Spectral Density

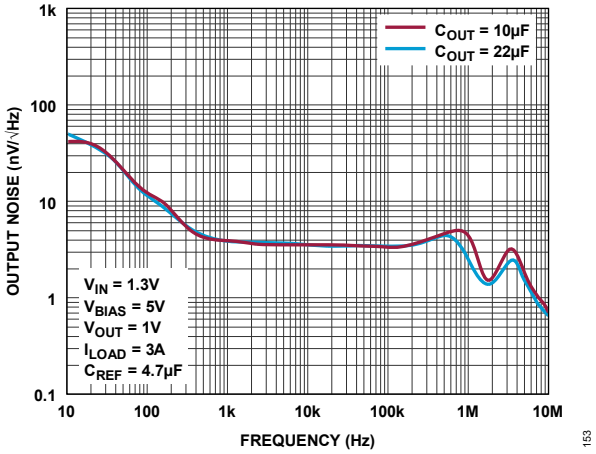


Figure 53. Noise Spectral Density

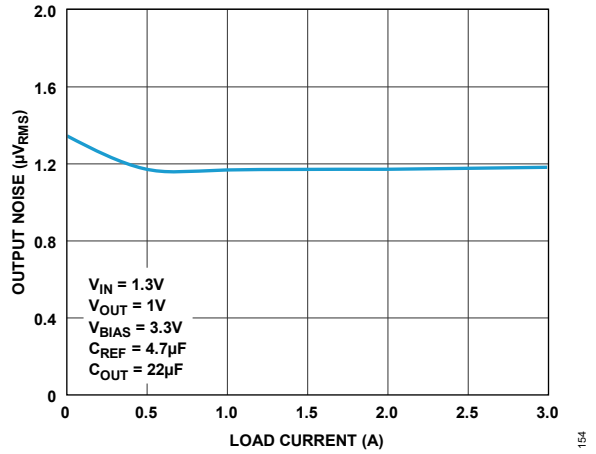


Figure 54. Integrated RMS Output Noise (10Hz to 100kHz)

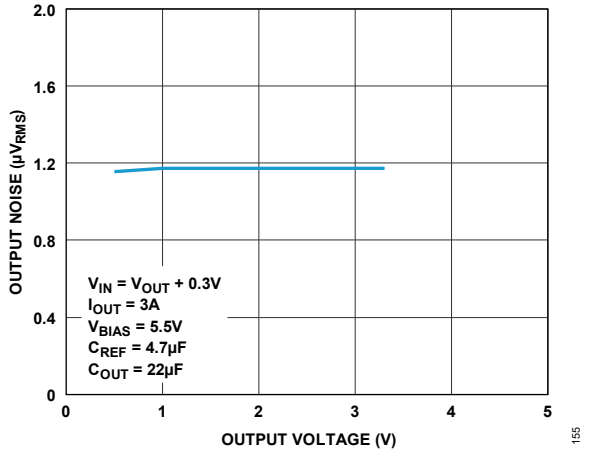


Figure 55. Integrated RMS Output Noise (10Hz to 100kHz)

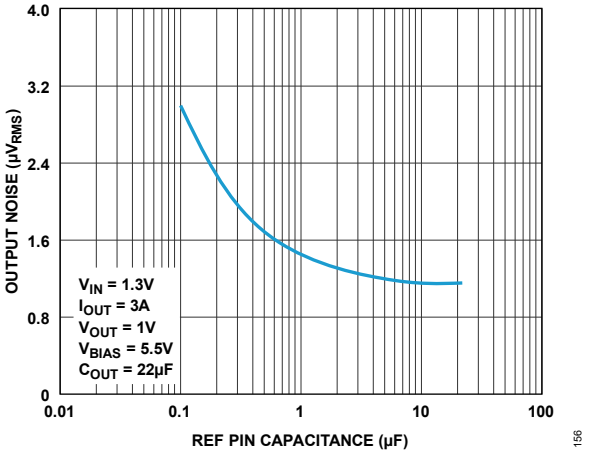


Figure 56. Integrated RMS Output Noise (10Hz to 100kHz)

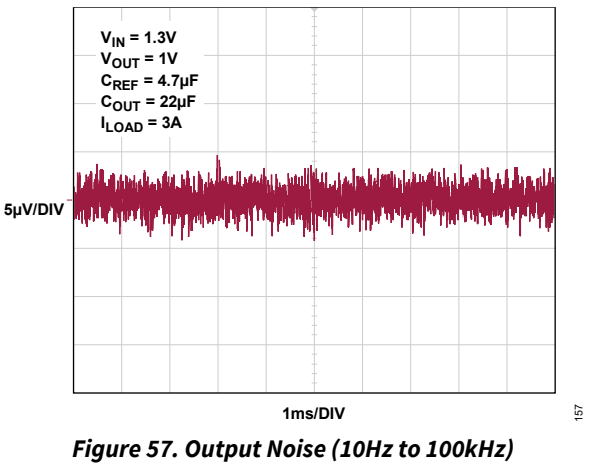


Figure 57. Output Noise (10Hz to 100kHz)

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

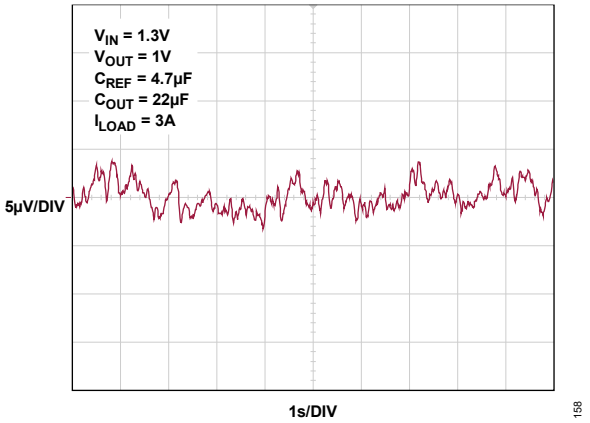


Figure 58. Output Noise (0.1Hz to 10Hz)

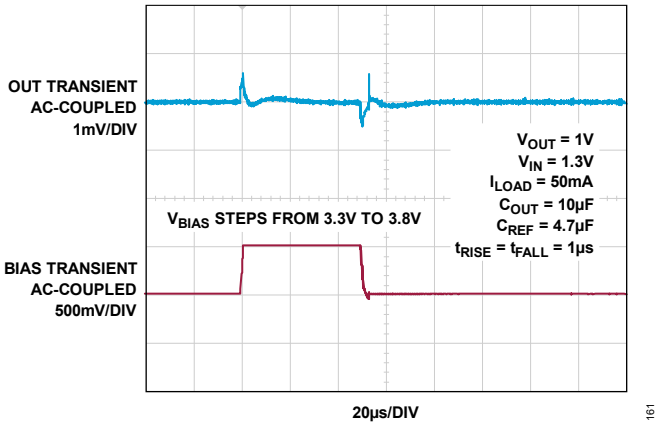


Figure 61. BIAS Pin Line Transient

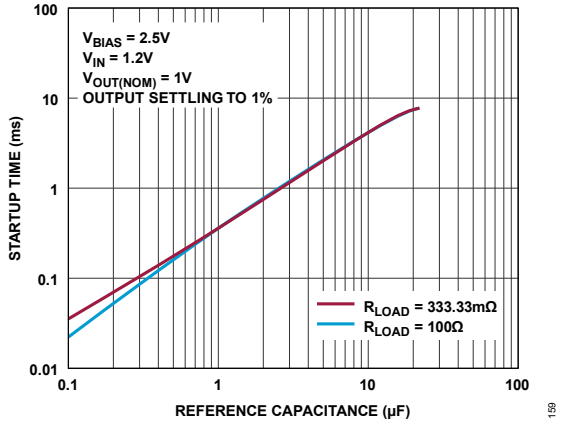


Figure 59. Startup Time

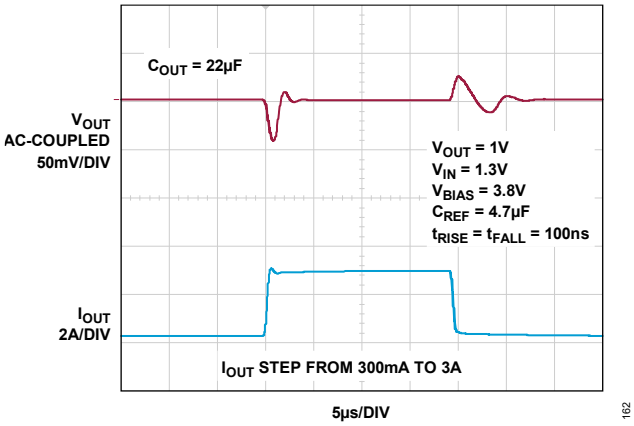


Figure 62. Load Transient

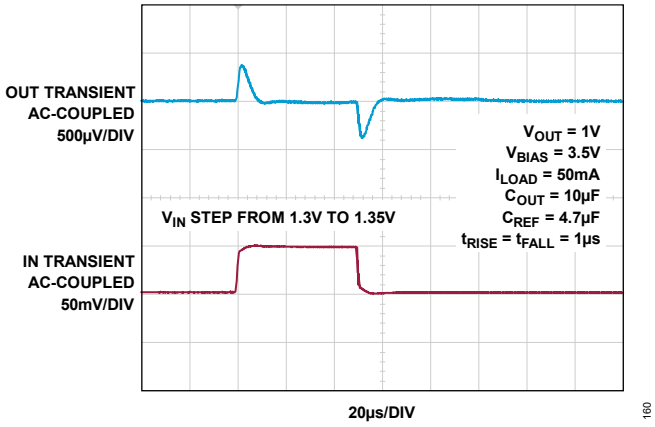


Figure 60. IN Pin Line Transient

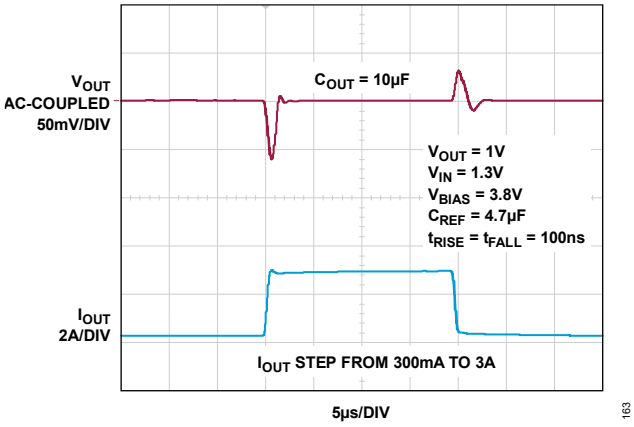


Figure 63. Load Transient

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless noted otherwise.

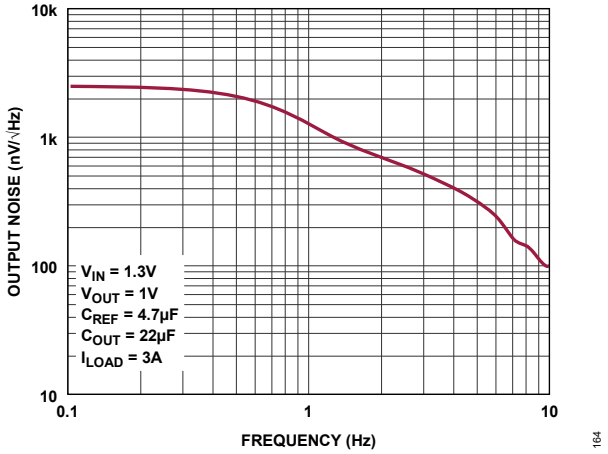
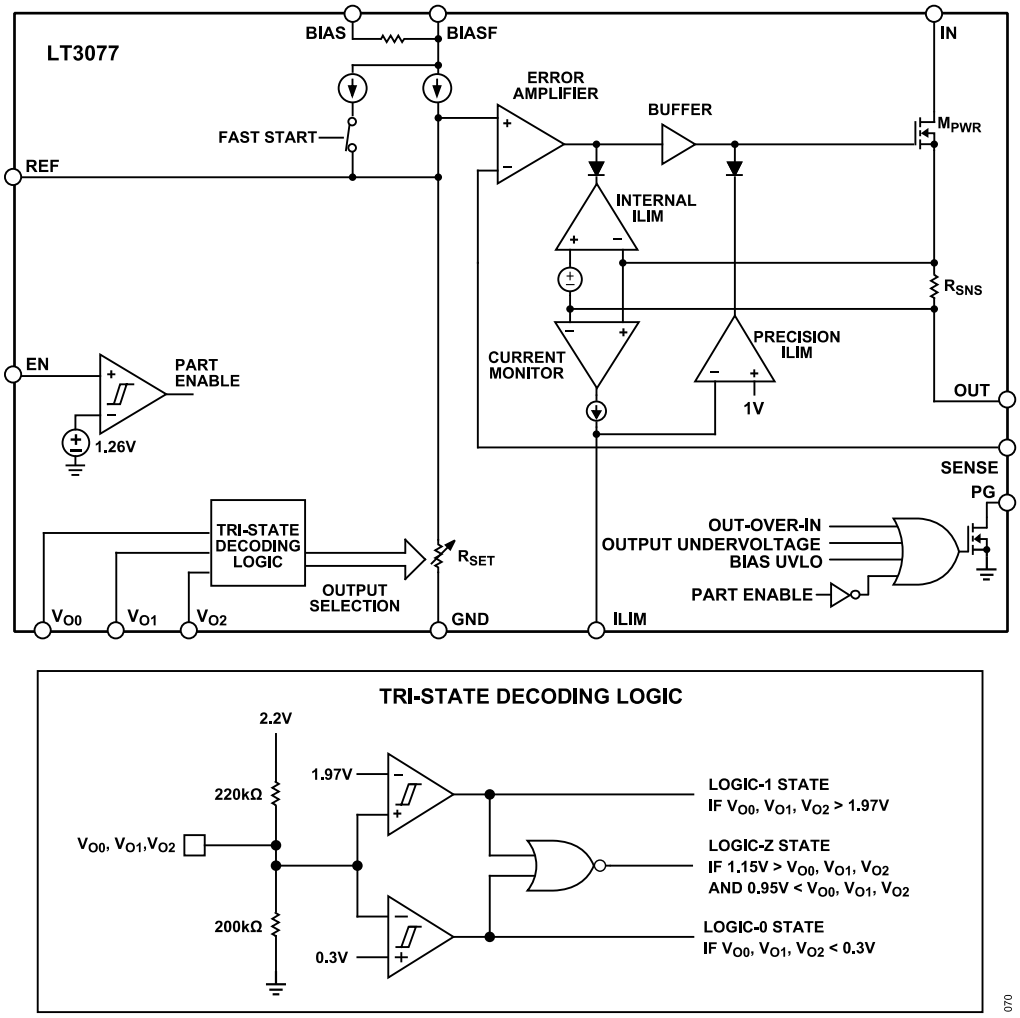


Figure 64. Noise Spectral Density

FUNCTIONAL DIAGRAM



APPLICATIONS INFORMATION

The LT3077 is a low voltage, ultra-low noise, and ultra-fast transient response linear regulator. The device supplies up to 3A with a typical dropout voltage of 85mV. A 4.7µF reference bypass capacitor decreases output voltage noise to 1.2µV_{RMS}. The LDO's wide bandwidth and high PSRR permit the use of small ceramic capacitors, saving bulk capacitance and cost. The LT3077 is ideal for high-performance FPGAs, microprocessors, RF communication, and noise-sensitive supply applications.

Output Voltage

The LT3077's unity-gain operation provides virtually constant output noise, PSRR, and bandwidth independent of the programmed output voltage. Output voltages are digitally selectable in 50mV increments from 0.5V to 1.2V, 100mV increments from 1.2V to 1.8V, and discrete levels at 2V, 2.5V, 3V, 3.3V, and 4.2V.

Three trilevel input pins, V_{O0}, V_{O1}, and V_{O2}, select the output voltage. *Table 6* illustrates the three-bit digital word-to-output voltage relationship resulting from setting these pins high, low, or allowing them to float. An input logic low state is guaranteed with less than 300mV referenced to GND, and a logic high state is guaranteed with greater than 1.97V. The range between 950mV to 1.15V defines the logic Hi-Z (input floating) state. These pins may be connected high by strapping them to V_{BIAS} or driving them with digital ports. Pins that float may either float or require logic that has Hi-Z output capability. This allows the output voltage to be dynamically changed if necessary.

Table 6. V_{OUT} Selection Matrix

V_{OUT} (V)	V_{O2}	V_{O1}	V_{O0}
0.50	0	0	0
0.55	0	0	Z
0.60	0	0	1
0.65	0	Z	0
0.70	0	Z	Z
0.75	0	Z	1
0.80	0	1	0
0.85	0	1	Z
0.90	0	1	1
0.95	Z	0	0
1.00	Z	0	Z
1.05	Z	0	1
1.10	Z	Z	0
1.15	Z	Z	Z
1.20	Z	Z	1
1.30	Z	1	0
1.40	Z	1	Z
1.50	Z	1	1
1.60	1	0	0
1.70	1	0	Z
1.80	1	0	1
2.00	1	Z	0
2.50	1	Z	Z
3.00	1	Z	1
3.30	1	1	0
4.20	1	1	Z
DO NOT USE	1	1	1

0 = Low, Z = Hi-Z (Float), 1 = High

REF – Voltage Reference

The REF pin is the voltage output of the internal current reference feeding into a resistor DAC. A 4.7µF REF capacitor to GND decreases reference voltage noise, and soft starts OUT at enable. Soft-start time is determined by the value of the REF capacitor used.

The REF pin must not be DC loaded by anything except for applications that parallel other LT3077 regulators for higher output currents. See the *Paralleling Devices for Higher Output Current* section for further details.

Overdriving the REF Pin

The REF pin can be overdriven by an external source for applications that need to set the Output voltage to a value other than those programmable using the V_{O0}, V_{O1}, and V_{O2} pins. The LT3077 uses a current source with a typical value of 100µA into a resistor DAC. The resistor DAC and the current source are inversely related and may vary up to ±15% such that the IR product is constant. This variation in the internal current and resistor needs to be accounted for when externally driving the REF pin.

It is recommended that the VOX pin configuration be set to select a REF pin voltage lower than the required overdriven REF voltage to ensure the fast start current is shut off when LT3077 regulates the output. As shown in *Figure 65*, the REF can be overdriven directly by an external voltage source, or as shown in *Figure 66*, a voltage source followed by a resistor-divider. In case where the REF pin is driven by an external voltage source followed by a resistor-divider, the external voltage source can be a fixed voltage source or can be varied using a servo loop to achieve higher accuracy.

When using an external voltage source with a resistor-divider, the resulting REF pin voltage can be calculated using superposition principle as shown in the following equation:

$$V_{REF} = V_{EXT} \times \left(\frac{(R_{INT} || R_{EXT2})}{(R_{INT} || R_{EXT2}) + R_{EXT1}} \right) + I_{INT} \times (R_{INT} || R_{EXT1} || R_{EXT2})$$

Where I_{INT} is the internal 100µA current reference, R_{INT} is the nominal resistor value for the corresponding VOX setting, R_{EXT1} and R_{EXT2} are the external resistors forming the resistor-divider and V_{EXT} is the external voltage source overdriving the REF pin.

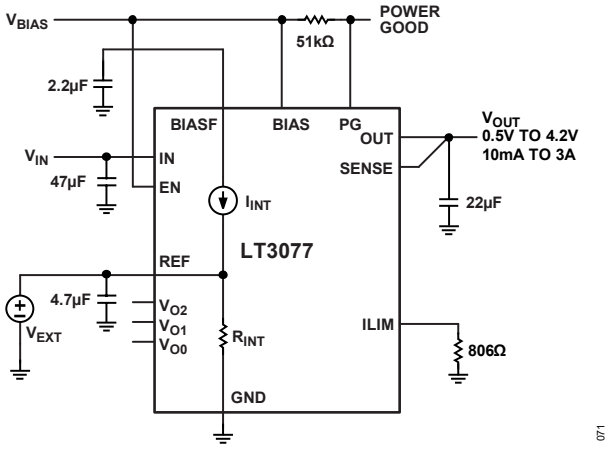


Figure 65. REF Overdriven Directly by an External Voltage Source

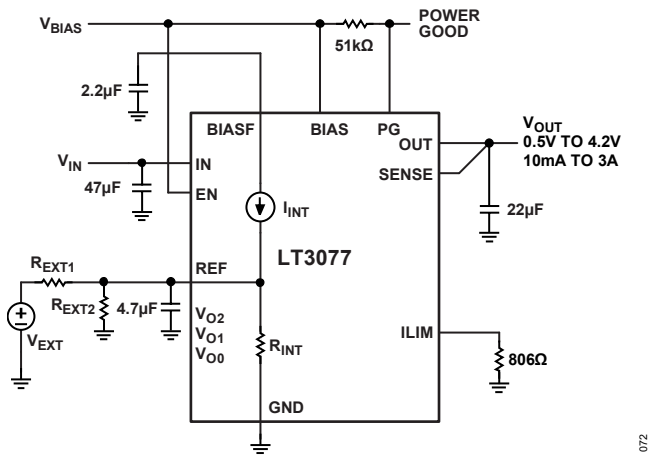


Figure 66. REF Overdriven by a Voltage Source Followed by a Resistor-Divider

When using an external voltage source with resistor-dividers, choose R_{EXT1} and R_{EXT2} such that R_{EXT2} value is at most 10% of nominal R_{INT} value to assure accuracy across process variations in R_{INT}.

Example: Setting REF to be 1.025V with a 1.25V external reference and using resistor-dividers.

Set the VOX pins such that LT3077 selects the 1V output setting (V_{O0} and V_{O2} are Hi-Z and V_{O1} is GND).

For 1V setting:

$$R_{INT(NOMINAL)} = 1V/100\mu A = 10k\Omega$$

Select:

$$R_{EXT2} = R_{INT}/10 = 1k\Omega$$

Using these values, the equation is:

$$R_{EXT2}||R_{INT} = 1k\Omega||10k\Omega = 909.0909\Omega$$

Substituting in the above equation for V_{REF}, the equation is:

$$1.025V = 1.25V \times \left(\frac{909.0909\Omega}{909.0909\Omega + R_{EXT1}}\right) + 100\mu A \times (909.0909\Omega||R_{EXT1})$$

Solving for R_{EXT1} gives R_{EXT1} = 218.978Ω. The closest 1% resistor is 221Ω.

If overdriving the REF pin, V_{OUT} thresholds for power good mentioned in *Table 1* can no longer be guaranteed.

Enable Function – Turning ON and OFF

The EN pin enables/disables the reference, the output transistor, and disables auxiliary functions. Pulling EN low places the regulator into Nap mode. In Nap mode, the quiescent current decreases to less than 10µA. The LT3077 has an accurate 1.26V turn-on threshold on the EN pin with 80mV of hysteresis. This threshold can be used with a resistor-divider from the bias supply to define an accurate UVLO threshold for the regulator. The EN pin current (I_{EN}) at the threshold shown in *Table 1* must be considered when calculating the resistor-divider network as follows:

$$V_{BIAS(UVLO)} = 1.26V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN/UV} \times R_{EN2}$$

Where:

R_{EN1} and R_{EN2} are the resistors from the EN pin to GND and the EN pin to BIAS pin respectively. I_{EN} can be ignored if R_{EN1} is less than 100kΩ. If unused, tie the EN pin to BIAS.

BIAS Undervoltage Lockout

An internal undervoltage lockout (UVLO) comparator monitors the BIAS rail. If V_{BIAS} drops below the UVLO threshold, all functions shut down, the pass transistors are gated off, and output currents fall to zero. The typical BIAS pin UVLO threshold is 2.2V on the rising edge of V_{BIAS}. The UVLO circuit incorporates about 130mV of hysteresis on the falling edge of V_{BIAS}.

Power Good

The PG pin is an open-drain NMOS output that actively pulls low if EN is low or if any one of these fault modes is detected:

- V_{OUT} is less than 93% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}.
- V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the falling edge of V_{OUT}.
- V_{BIAS} is less than its undervoltage lockout threshold.
- The OUT-over-IN voltage detector activates.

Stability and Output Capacitance

The LT3077 feedback loop requires a minimum output capacitance of 10µF for stability. ADI recommends mounting low ESR, X5R, or X7R ceramic capacitors near the LT3077 OUT and GND pins. Include wide routing planes for OUT and GND to minimize inductance. If possible, mount the regulator immediately adjacent to the application load to minimize distributed inductance for optimal load transient performance. Point-of-load applications present the best-case layout scenario for extracting full LT3077 performance.

Additional ceramic capacitors distributed beyond the immediate decoupling capacitors are acceptable and recommended at the point of the load because the distributed PCB inductance isolates them from the primary compensation capacitors.

Many of the applications in which the LT3077 excels, such as FPGA, ASIC processor, or DSP supplies, typically require a high-frequency decoupling capacitor network for the device being powered. This network generally consists of many low-value ceramic capacitors in parallel. In parallel, multiple low-value capacitors present a favorable frequency characteristic that reduces the parasitic inductance of the capacitors.

Consider the use of ceramic capacitors. Ceramic capacitors are manufactured with various dielectrics, each with different temperatures and applied voltage behavior. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are suitable for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients, as shown in *Figure 67* and *Figure 68*. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor.

The X7R type has better stability across temperatures, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify the operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases but expected capacitance at operating voltage should be verified. Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates a voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

In addition to the DC bias and temperature variation noted above, variation in effective capacitance with applied AC voltage needs to be considered as well. Ceramic capacitors are typically specified for an AC ripple of 1V. Effective capacitance decreases with lower AC ripple voltages. Effective capacitance will decrease by 30% or more with the very low AC ripple at the output of the LT3077. Contact the ceramic capacitor vendor for more information on temperature, DC bias voltage, and AC ripple voltage effects when selecting a capacitor to meet the minimum capacitance requirements of the LT3077.

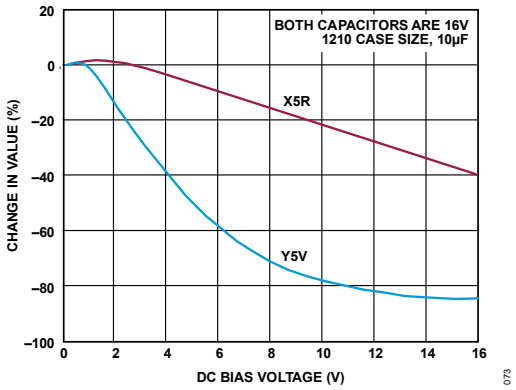


Figure 67. Ceramic Capacitor DC Bias Characteristics

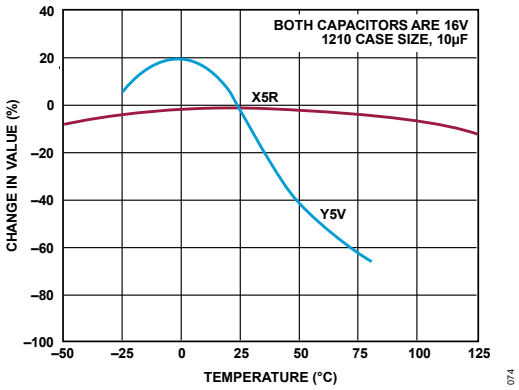


Figure 68. Ceramic Capacitor Temperature Characteristics

Stability and Input Capacitance

The LT3077 is stable with a minimum capacitance of 4.7µF connected to the IN pins. Use low ESR capacitors to minimize instantaneous voltage drops under large-load transient conditions. Large V_{IN} droops during large-load transients may cause the regulator to enter dropout with the corresponding degradation in load transient response. Therefore, increased input and output capacitance values may be necessary depending on an application's requirements. Sufficient input capacitance is critical as the circuit is intentionally operated close to dropout to minimize power. Ideally, the output impedance of the supply that powers IN should be less than 20mΩ to support a 3A load with large transients.

In cases where a wire is used to connect a power supply to the input of the LT3077 (and also from the ground of the LT3077 back to the power supply ground), large input capacitors are required to avoid an unstable application. This is due to the inductance of the wire forming an LC tank circuit with the input capacitor and not a result of the LT3077 being unstable. A wire's self-inductance, or isolated inductance, is directly proportional to its length. However, the diameter of a wire does not have a significant influence on its self-inductance. For example, one inch of 18-AWG, 0.04 inch diameter wire has 28nH of self-inductance. The self-inductance of a 2-AWG isolated wire with a diameter of 0.26 inch is about half the inductance of the 18-AWG wire. The overall self-inductance of a wire can be reduced in two ways. One is to divide the current flowing toward the LT3077 between two parallel conductors. In this case, the farther the wires are placed apart, the more the inductance is reduced, up to a 50% reduction when set a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed near each other, mutual inductance is added to the overall self-inductance of the wires. The most effective way to reduce overall inductance is to place the forward and return-current conductors (the wire for the input and the wire for the return ground) in very close proximity. In this case, two 18-AWG wires separated by 0.05 inches reduce the overall self-inductance to about one-fourth of a single isolated wire. If the LT3077 is powered by a battery mounted near the ground and power planes on the same circuit board, a 10µF input capacitor is sufficient for stability. If a distant supply powers the LT3077, use a low ESR, large value input capacitor on the order of 220µF. As power supply output impedance varies, the minimum input capacitance needed for application stability also varies.

BIAS/BIASF Pin Requirements

The BIAS pin supplies current to most of the internal control circuitry and the output stage, which drives the pass transistor. The LT3077 requires a minimum 2.2µF bypass capacitor on the BIASF pin for stability and proper operation. No bypass capacitor is needed on the BIAS pin. To ensure proper operation, the BIAS voltage must satisfy the following conditions: 2.375V ≤ V_{BIAS} ≤ 5.5V and V_{BIAS} ≥ (V_{OUT} + 1.2V). For V_{OUT} ≤ 1.15V, the minimum BIAS voltage is limited to 2.375V.

Load Regulation

The LT3077 corrects for a parasitic package, and PCB I-R drops when the SENSE pin is Kelvin connected to output capacitors. The LT3077 handles moderate levels of output line impedance, but excessive impedance between V_{OUT} and C_{OUT} causes an excessive phase shift in the feedback loop and adversely affects stability.

PCB Layout Considerations

Given the LT3077's high bandwidth and high PSRR, careful PCB layout must be employed to achieve full device performance. *Figure 69* shows the EVAL-LT3077-AZ evaluation board with a layout that delivers the full performance of the regulator. Refer to the *EVAL-LT3077-AZ evaluation board user guide* for further details.

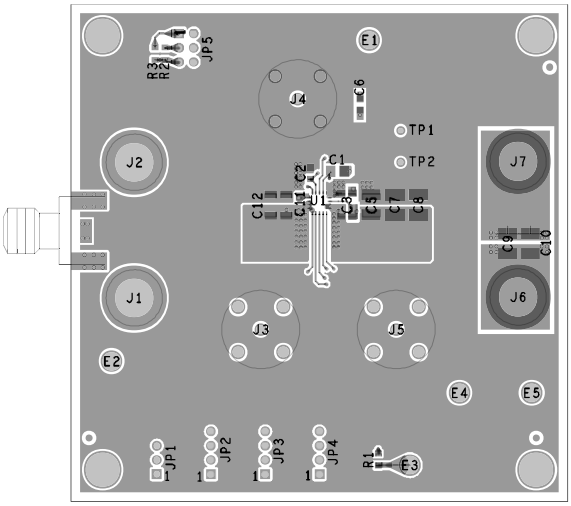


Figure 69. EVAL-LT3077-AZ Evaluation Board

Protection Features

The LT3077 has an internal current limit that clamps output current to 4.5A. In addition, the LT3077 has a ±10% accurate programmable precision current limit. The die junction temperature can exceed the 125°C maximum operating temperature if the ambient temperature is high enough. If this occurs, the LT3077 relies on an internal thermal safety feature. Typically at 168°C, the LT3077 thermal shutdown engages and the output is shut down until the IC temperature falls below its thermal hysteresis limit.

Externally Programmable Current Limit

The ILIM pin's current limit threshold is 1V. Connecting a resistor from ILIM to GND sets the maximum current flowing out of the ILIM pin, which in turn, programs LT3077's current limit. With a 3A x kΩ programming scale factor, the current limit can be calculated as follows:

$$Current\ Limit = \frac{3A \times k\Omega}{R_{ILIM}}$$

For example, a 1kΩ resistor programs the current limit to 3A, and a 2kΩ resistor programs the current limit to 1.5A. Kelvin connect this resistor to the LT3077's GND pin for good accuracy.

As shown in the electrical characteristic table (*Table 1*), the ILIM pin sources current proportional (1:3000) to output current; if the external current limit is not used, connect ILIM to GND, which sets the internal current limit to 4.5A.

Thermal Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT3077. The IN and OUT pins on the bottom of the package should be soldered to IN and OUT planes accordingly. In addition, the IN and OUT must be connected to large copper layers below with thermal vias; these layers spread heat dissipated by the LT3077. Placing additional vias can reduce thermal resistance further. The die temperature is calculated by multiplying the LT3077 power dissipation by the thermal resistance from the junction to the ambient.

The internal overtemperature protection monitors the junction temperature of the LT3077. If the junction temperature reaches approximately 168°C, the LT3077 output shuts down until the temperature drops about 7°C.

Calculating Junction Temperature

Example: Given an output voltage of 1.2V, input voltage of 1.5V, and BIAS voltage of 5V, output current ranges from 10mA to 3A, and a maximum ambient temperature of 50°C, what is the maximum junction temperature?

The LT3077's power dissipation is:

$$I_{OUT(MAX)} \times (V_{IN} - V_{OUT}) + I_{GND} \times V_{BIAS}$$

where:

$I_{OUT(MAX)} = 3A$

$V_{BIAS} = 5V$

$$I_{GND}(at\ I_{OUT} = 3A\ and\ V_{BIAS} = 5V) = 5mA$$

thus:

$$P_{DISS} = 3A \times (1.5V - 1.2V) + 5mA \times 5V = 0.925W$$

When a 3mm x 3mm LFCSP-RT package is used, the thermal resistance is in the range of 41°C/W to 47°C/W. Note that the θ_{JA} numbers vary beyond the 41°C/W to 47°C/W depending on board composition and layout. Considering a θ_{JA} value of 44°C/W, the junction temperature rise above the ambient approximately equals:

$$0.925W \times 44°C/W = 40.7°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

$$T_{JMAX} = 50°C + 40.7°C = 90.7°C$$

Paralleling Devices for Higher Output Current

As shown in *Figure 70*, multiple LT3077s may be paralleled to obtain a higher output current. This paralleling concept borrows from the scheme employed by the *LT3080* product family.

To accomplish this paralleling, connect the IN and OUT pins of the multiple devices together. Also, connect the REF pins of the multiple devices. This effectively gives an averaged value of multiple reference voltage sources. The OUT of each LT3077 is connected to the common load using a small piece of PC trace as a ballast resistor (≅2mΩ) or an actual sense resistor beyond the feedback SENSE tap of each regulator. The ballast resistor ensures output current sharing. Keep this ballast trace area free of solder to maintain a controlled resistance.

Table 7 shows a simple guideline for PCB trace resistance as a function of weight and trace width.

Table 7. PC Board Trace Resistance [1]

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

[1] Trace resistance is measured in mΩ/in.

Output Noise

The LT3077 offers many advantages for noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a conventional regulator are its voltage reference, error amplifier, noise from the resistor divider network used for setting output voltage, and the noise gain created by this resistor-divider.

LT3077's unity-gain follower architecture presents no gain from the REF pin to the output. Therefore, if a capacitor bypasses the REF pin internal resistor DAC, the output noise is independent of the programmed output voltage. The resultant output noise is set just by the error amplifier's noise — typically 3.5nV/$\sqrt{Hz}$ from 10kHz to 1MHz and 1.2μV_{RMS} in a 10Hz to 100kHz bandwidth using a 4.7µF REF pin capacitor. Paralleling multiple LT3077s further reduces noise by $\sqrt{N}$ for N parallel regulators.

Filtering High Frequency Spikes

For applications where the LT3077 is used to post-regulate a switching converter, its high PSRR effectively suppresses any noise present at the switcher's switching frequency — typically 100kHz to 4MHz. However, the high frequency (hundreds of MHz) spikes — beyond the LT3077's bandwidth — associated with the switcher's power switch transition times almost directly pass through the LT3077. While the output capacitor is partly intended to absorb these spikes, its ESL limits its ability at these frequencies. A ferrite bead or the inductance associated with a short (example: 0.5 inch) PCB trace between the switcher's output and the LT3077's input can serve as an LC filter to suppress these very high-frequency spikes.

Fast Start-Up

For ultra-low noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value REF pin capacitor is required, up to 22µF. While this normally significantly increases the regulator's start-up time, the LT3077 incorporates fast start-up circuitry that increases the REF pin current to about 2mA during start-up. For a 22µF capacitor, this reduces the start-up time from 100ms to 5ms.

The 2mA current source remains engaged until REF is 98.8% of its final value on the rising edge. It restarts when REF is below 91% of the output setting on the falling edge unless the regulator is in the current limit, thermal shutdown or any UVLO situation.

TYPICAL APPLICATION CIRCUITS

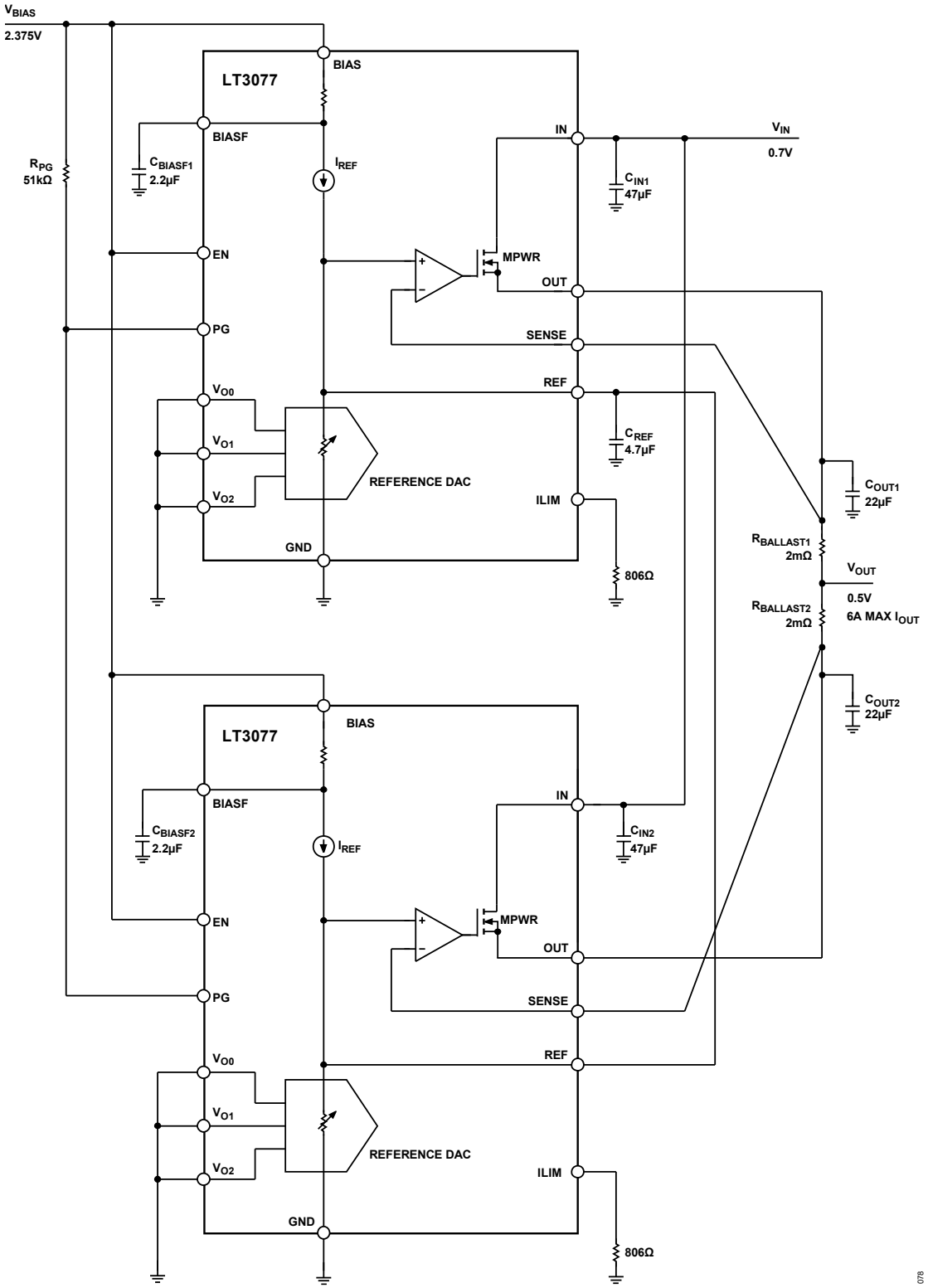
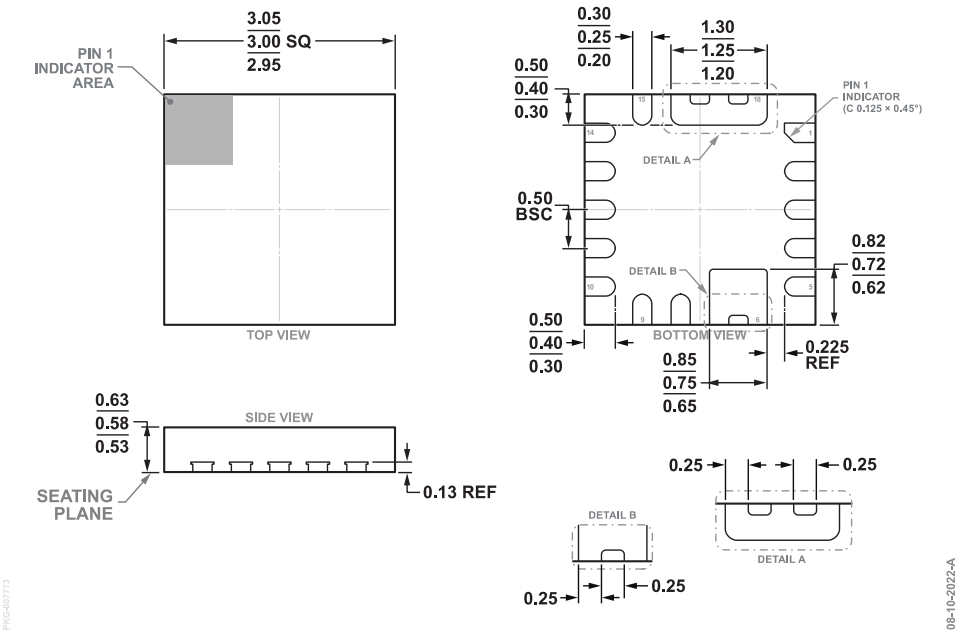


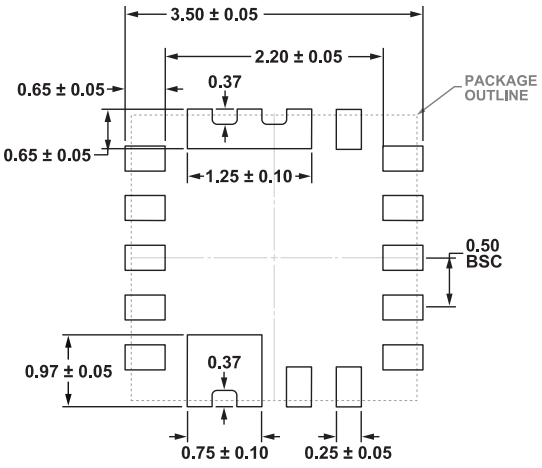
Figure 70. Paralleling Multiple LT3077s for Higher Output Current

OUTLINE DIMENSIONS

18-Lead Lead Frame Chip Scale Package, Routable, No Solder Spheres [LFCSP_RT]
3 x 3 mm Body and 0.58 mm Package Height
(CR-18-1)
Dimensions shown in millimeters



RECOMMENDED SOLDER PAD LAYOUT
(TOP VIEW)



ORDERING GUIDE

Table 8. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	MSL RATING	PACKING QUANTITY	PACKAGE OPTION
LT3077ACRZ	-40°C to 125°C	18-LEAD (3mm x 3mm LFCSP-RT)	3	Tray, 490	CR-18-1
LT3077ACRZ-R7	-40°C to 125°C	18-LEAD (3mm x 3mm LFCSP-RT)	3	Reel, 2500	CR-18-1

[1] All models are RoHS compliant parts.

EVALUATION BOARDS

Table 9. Evaluation Boards

MODEL [1]	DESCRIPTION
EVAL-LT3077-AZ	Evaluation Board

[1] The EVAL-LT3077-AZ is a RoHS compliant part.

RELATED PARTS

Table 10. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LT3073	3A, Ultra-Low Noise, High PSRR, 45mV Dropout Ultra-Fast Linear Regulator	45mV Dropout, Digitally Programmable V_{OUT}: 0.5V to 4.2V, Digital Output Margining: ±2.5%, Ultra-low Output Noise: 1.2µV_{RMS}, High PSRR: 52dB at 1MHz, Direct Parallelable, Soft Start, Stable with Low ESR Ceramic Output Capacitors (10µF minimum), 22-Lead 3mm × 4mm LQFN Package.
LT3078	5.5V, 5A, Ultra-Low noise, High PSRR, 55mV Dropout Ultra-Fast Linear Regulator	55mV Dropout, Digitally Programmable V_{OUT}: 0.5V to 4.2V, Digital Output Margining: ±2.5%, Ultra-low Output Noise: 1.3µV_{RMS}, High PSRR: 49dB at 1MHz, Direct Parallelable, Soft Start, Stable with Low ESR Ceramic Output Capacitors (22µF minimum), 22-Lead 3mm × 4mm LQFN Package.
LT3070-1	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Digital Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Digital Output Margining: ±1%, ±3% or ±5%, Low Output Noise:25µV_{RMS}; Directly Parallelable, Soft Start, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28 Lead 4mm × 5mm QFN Package.
LT3071	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Analog Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Analog Margining: ±10%, Low Output Noise: 25µV_{RMS}; Directly Parallelable, Output Current Monitor, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28 Lead 4mm × 5mm QFN Package.

PART NUMBER	DESCRIPTION	COMMENTS
LT3072	Dual, Low Noise, 2.5A Programmable Output, 80mV Low Dropout Linear Regulator	Dual, Independent 2.5A Outputs, Dropout Voltage: 80mV, Low Output Noise: 12μV_{RMS} (10Hz to 100kHz), Digitally Programmable V_{OUT}: 0.6V to 2.5V, Output Tolerance: ±1.25%/±1.5% Over-load, Line and Temperature, Analog Output Margining: ±10% Range, 36-Lead 4mm × 7mm QFN Package.
ADP1763	3A, Low V_{IN}, Low Noise, CMOS Linear Regulator	95mV Dropout, Fixed (0.9V to 1.5V) and Adjustable (0.5V to 1.5V) V_{OUT}, V_{IN} = 1.1V to 1.98V, 2μV_{RMS} Noise (100Hz to 100kHz), Programmable Soft Start, Direct Parallelable, Stable with Ceramic Capacitors (10µF minimum), AEC-Q100 qualified, 16-Lead 3mm x 3mm LFCSP Package.
ADP1765	5A, Low V_{IN}, Low Noise, CMOS Linear Regulator	59mV Dropout, Fixed (0.55V to 1.5V) and Adjustable (0.5V to 1.5V) V_{OUT}, V_{IN} = 1.1V to 1.98V, 2μV_{RMS} Noise (100Hz to 100kHz), Programmable Soft Start, Direct Parallelable, Stable with Ceramic Capacitors (22µF minimum), 16-Lead 3mm x 3mm LFCSP Package.
MAX38907	4A, High-Performance LDO Linear Regulator	79mV Dropout, Digitally Programmable V_{OUT}: 0.6V to 5V, V_{IN} = 0.9V to 5.5V, Digital Margining: ±5%, Programmable Soft Start, Reverse Current Protection, Active Discharge, 20-Lead 5mm x 5mm TQFN Package.
LT3041	20V, 1A, Ultra-low Noise, Ultra-high PSRR Linear Regulator with VIOC Control	1μV_{RMS} Noise (10Hz to 100kHz), 8μV_{P-P} Noise (0.1Hz to 10Hz), 80dB PSRR at 1MHz, V_{IN} = 2.2V to 20V, V_{OUT} = 0.2V to 15V, 310mV Dropout, Direct Parallelable, Programmable Current Limit and Power Good, Stable with Low ESR Ceramic Capacitors (2x 10µF Minimum), 14-Lead 4mm x 3mm DFN Package.
LT3045	500mA, Ultra-low Noise and Ultra-high PSRR LDO	0.8μV_{RMS} Noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV Dropout Voltage, 3mm × 3mm DFN and MSOP Packages.
LT3042	200mA, Ultra-low Noise and Ultra-high PSRR LDO	0.8μV_{RMS} Noise and 79dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV Dropout Voltage, Programmable Current Limit and Power Good, 3mm× 3mm DFN and MSOP Packages.
LT3083	3A, Parallelable, Low Noise, Low Dropout Linear Regulator	310mV Dropout Voltage (2-Supply Operation), Low Noise: 40μV_{RMS}, V_{IN}: 1.2V to 23V, V_{OUT}: 0V to 22.6V, Current-Based Reference with one Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; TO-220, DD-PAK, TSSOP, 4mm × 4mm DFN-12 Packages.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	7/24	Initial Release	—