9 kHz to 13 GHz, Differential SPDT Switch

FEATURES

- Frequency range: 9 kHz to 13 GHz
- Nonreflective, differential, 100 Ω impedance design
- Low insertion loss
  - 0.8 dB to 10 GHz
  - 0.9 dB to 13 GHz
- High isolation
  - >45 dB to 10 GHz
  - >40 dB to 13 GHz
- High input linearity
  - P0.1dB: >31 dBm typical
  - IP3: 65 dBm typical
- High power handling
  - Through path: 31 dBm typical
  - Terminated path: 30 dBm typical
  - Hot switching: 27 dBm typical
- On and off time: 5 µs typical
- Positive control interface: CMOS-/LVTTL-compatible
- All off state control
- Pin-compatible with ADRF5062, fast switching version
- 20-terminal, 3.0 mm × 3.0 mm LGA package

APPLICATIONS

- Test instrumentation
- Data converter interfaces
- High data rate interfaces

FUNCTIONAL BLOCK DIAGRAM

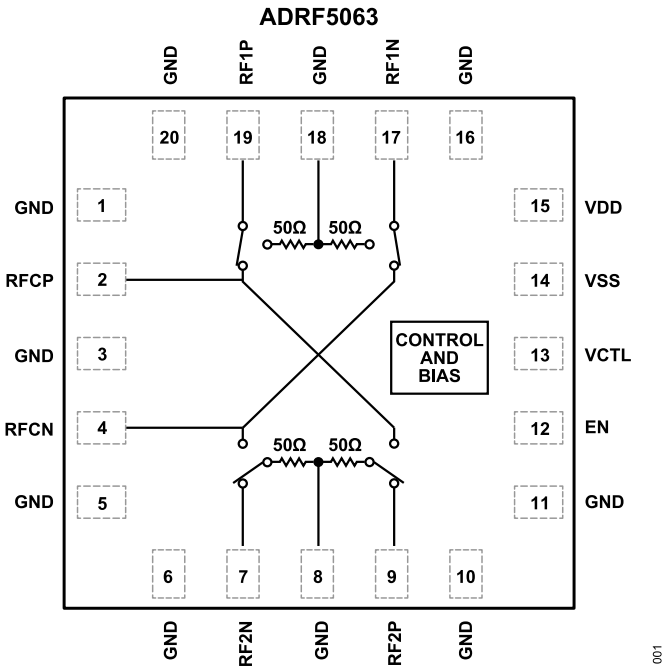

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5063 is a silicon, nonreflective, differential, SPDT switch. The ADRF5063 operates from 9 kHz to 13 GHz with insertion loss of lower than 0.9 dB and isolation of higher than 40 dB. The ADRF5063 has a RF input power handling capability of differential 31 dBm for through paths, differential 30 dBm for terminated paths and differential 27 dBm hot switching at the RF common port.

The ADRF5063 can operate with dual-supply voltages of ±3.3 V or a single-supply voltage of +3.3V when VSS is connected to GND. The ADRF5063 employs complementary metal-oxide semiconductor (CMOS)-compatible and low voltage transistor logic (LVTTL)-compatible controls. The ADRF5063 has an enable control to feature all off states.

The ADRF5063 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is connected to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. For more details, see Table 2.

The ADRF5063 is pin-compatible with the ADRF5062, fast switching version, which operates from 100 MHz to 13 GHz.

The ADRF5063 comes in a 20-terminal, 3.0 mm × 3.0 mm LGA package and can operate from −40°C to +105°C.

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REVISION HISTORY

11/2024—Rev. 0 to Rev. A

Changes to Data Sheet Title ... 1
Changes to Theory of Operation Section ... 10
Changes to RF Input and Output Section ... 10
Changes to Table 7 ... 10

10/2024—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, digital control voltage (V_{CTL}) = 0 V or 3.3 V, T_{CASE} = 25°C, and a 100 Ω differential system, unless otherwise noted. RFC refers to the RFCP and RFCN differential pair, RF1 refers to the RF1P and RF1N differential pair, RF2 refers to the RF2P and RF2N differential pair, and RFx refers the RF1 and RF2 differential pairs.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		13000	MHz
INSERTION LOSS						
RFC to RF1		0.1 GHz to 6 GHz		0.6		dB
		6 GHz to 10 GHz		0.8		dB
		10 GHz to 13 GHz		0.9		dB
RFC to RF2		0.1 GHz to 6 GHz		0.6		dB
		6 GHz to 10 GHz		0.8		dB
		10 GHz to 13 GHz		0.9		dB
RETURN LOSS						
RFC (On)		0.1 GHz to 10 GHz		20		dB
		10 GHz to 13 GHz		19		dB
RFx (On)		0.1 GHz to 6 GHz		20		dB
		6 GHz to 13 GHz		18		dB
RFx (Off)		0.1 GHz to 13 GHz		20		dB
ISOLATION						dB
RFC to RFx		0.1 GHz to 6 GHz		52		dB
		6 GHz to 10 GHz		47		dB
		10 GHz to 13 GHz		42		dB
RFx to RFx		0.1 GHz to 6 GHz		52		dB
		6 GHz to 10 GHz		45		dB
		10 GHz to 13 GHz		40		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	$t_{RISE, FALL}$	10% to 90% of RF output		2.5		µs
On and Off Time	$t_{ON, OFF}$	50% V_{CTL} to 90% of RF output		5		µs
0.1 dB Settling Time		50% V_{CTL} to 0.1 dB of final RF output		7		µs
INPUT LINEARITY[1]						
0.1 dB Power Compression	P0.1dB	f = 0.1 GHz to 13 GHz		>31		dBm
Third-Order Intercept	IP3	f = 2.3 GHz, two-tone input power = 20 dBm each tone, Δf = 1 MHz		65		dBm
DIFFERENTIAL PAIR CHARACTERISTICS						
Amplitude Imbalance RF1		6 GHz		0.1		dB
		10 GHz		0.2		dB
		13 GHz		0.25		dB
Amplitude Imbalance RF2		6 GHz		−0.1		dB
		10 GHz		−0.3		dB
		13 GHz		−0.4		dB
Phase Imbalance RF1		6 GHz		6		Degrees
		10 GHz		8		Degrees
		13 GHz		9		Degrees
Phase Imbalance RF2		6 GHz		−4		Degrees
		10 GHz		−5		Degrees
		13 GHz		−3		Degrees
Group Delay	t_{GD}			45		ps

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY CURRENTS		VDD and VSS pins				
Positive	V_{DD}			135		µA
Negative	V_{SS}			510		µA
DIGITAL CONTROL INPUTS		VCTL and EN pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTL}		0		V_{DD}	V
RF Input Power[2, 3]	P_{IN}	f = 1 MHz to 13 GHz, T_{CASE} = 85°C[4]				
Through Path		RF signal is applied to RFC or through connected RFx			31	dBm
Terminated Path		RF signal is applied to terminated RFx			30	dBm
Hot Switching		RF signal is present at RFC while switching between RFx			27	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 12 and Figure 15.

[2] For power derating over frequency, see Figure 2.

[3] Apply 3 dB derating for RFCx and RFxx rating in single-ended operation.

[4] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

SPECIFICATIONS

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3 V, V_{SS} = 0 V, V_{CTL} = 0 V or 3.3 V, T_{CASE} = 25°C, and a 100 Ω differential system, unless otherwise noted. RFC refers to the RFCP and RFCN differential pair, RF1 refers to the RF1P and RF1N differential pair, RF2 refers to the RF2P and RF2N differential pair, and RFx refers the RF1 and RF2 differential pairs.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		13000	MHz
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		2.5		µs
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		5		µs
0.1 dB RF Settling Time		50% V_{CTL} to 0.1 dB of final RF output		7		µs
INPUT LINEARITY		f = 1 MHz to 13 GHz				
0.1 dB Power Compression	P0.1dB			22		dBm
Third-Order Intercept	IP3	f = 2.3 GHz, two-tone input power = 0 dBm each tone, Δf = 1 MHz		53		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1, 2]	P_{IN}	f = 0.1 GHz to 13 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RFx			21	dBm
Terminated Path		RF signal is applied to terminated RFx			21	dBm
Hot Switching		RF signal is applied to the RFC while switching between RFx			21	dBm

[1] For power derating over frequency, see Figure 2.

[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 3. Absolute Maximum Ratings

Parameter[1, 2]	Rating
Supply Voltage	
Positive	−0.3V to +3.6 V
Negative	−3.6 V to +0.3 V
Digital Control Inputs[3]	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power (V_{DD}= 3.3 V, V_{SS} = −3.3 V, f[4] = 1 MHz to 13 GHz, T_{CASE} = 85°C[5])	
Through Path	31.5 dBm
Terminated Path	30.5 dBm
Hot Switching (RFC)	27.5 dBm
RF Input Power[4] (V_{DD}= 3.3 V, V_{SS}= 0 V, f = 1 MHz to 13 GHz, T_{CASE} = 85°C)	
Through Path	21.5 dBm
Terminated Path	22.5 dBm
Hot Switching (RFC)	21.5 dBm
RF Input Power, Unbiased (V_{DD} and V_{SS} = 0 V)	30 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 RF input power specifications are defined over 100 Ω differential pairs.

2 RFC refers to the RFCP and RFCN differential pair.

3 Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

4 For power derating over frequency, see Figure 2.

5 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-20-15		
Through Path	110	°C/W
Terminated Path	50	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

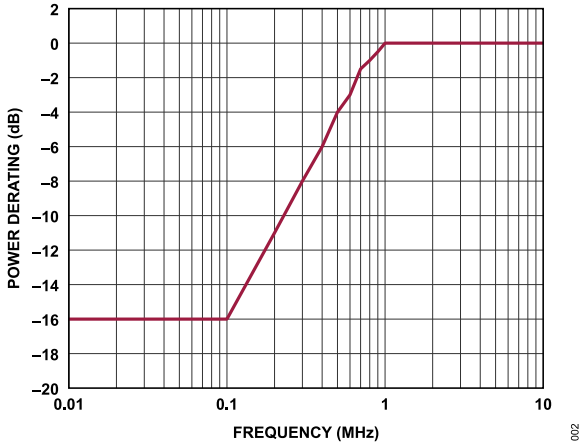

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5063

Table 5. ADRF5063, 20-Terminal LGA

ESD Model[1]	Withstand Threshold (V)	Class
HBM		
RF1x, RF2x, and RFCx Pins	1250	1C
Supply and Control Pins	1500	1C
CDM	500	C2A

1 RF1x refers to the RF1P and RF1N, RF2x refers to the RF2P and RF2N pins, and RFCx refers to the RFCP and RFCN pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

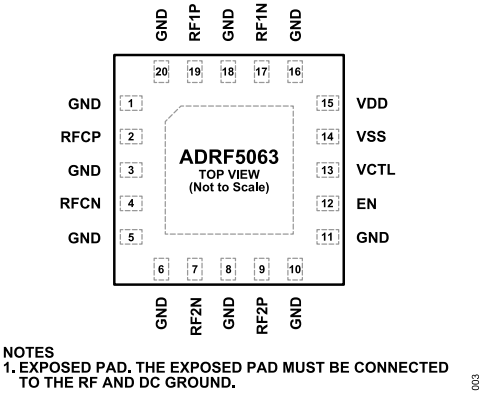

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 6, 8, 10, 11, 16, 18, 20	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
2, 4, 7, 9, 17, 19	RFCP, RFCN, RF2N, RF2P, RF1N, RF1P	The RFCx, RF1x, and RF2x pins are DC-coupled to 0 V and RF matched to differential, 100 Ω impedance as differential pairs. See Figure 4 for the interface schematic.
12	EN	Enable Input. See Table 7 for the truth table. See Figure 5 for the interface schematic.
13	VCTL	Control Input. See Table 7 for the truth table and Figure 5 for the interface schematic.
14	VSS	Negative Supply Voltage. See Figure 6 for the interface schematic.
15	VDD	Positive Supply Voltage. See Figure 7 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground.

INTERFACE SCHEMATICS

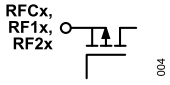

Figure 4. RFCx, RF1x, and RF2x Interface Schematic

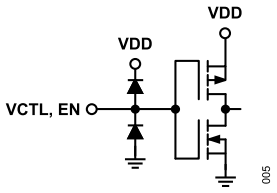

Figure 5. VCTL and EN Interface Schematic

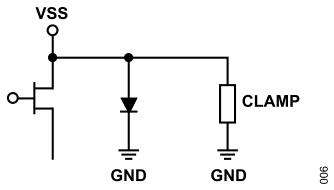

Figure 6. VSS Interface Schematic

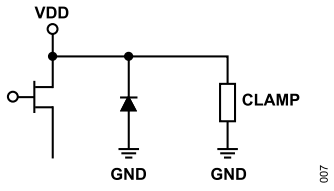

Figure 7. VDD Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTL} = 0 V or 3.3 V, and T_{CASE} = 25°C, and a 100 Ω differential system, unless otherwise noted. RFC refers to the RFCP and RFCN differential pair, RF1 refers to the RF1P and RF1N differential pair, RF2 refers to the RF2P and RF2N differential pair, and RFx refers the RF1 and RF2 differential pairs.

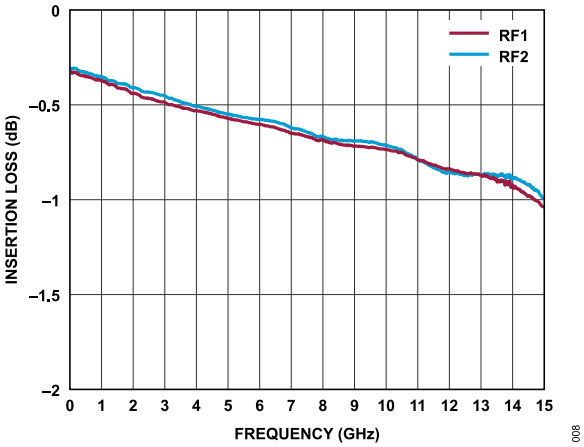

Figure 8. Insertion Loss vs. Frequency, RF1 and RF2

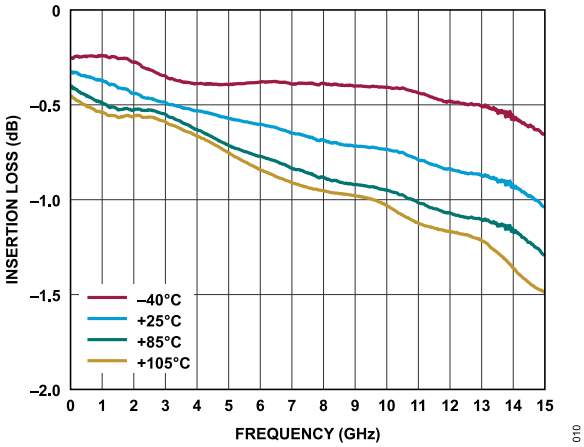

Figure 10. Insertion Loss vs. Frequency over Temperature

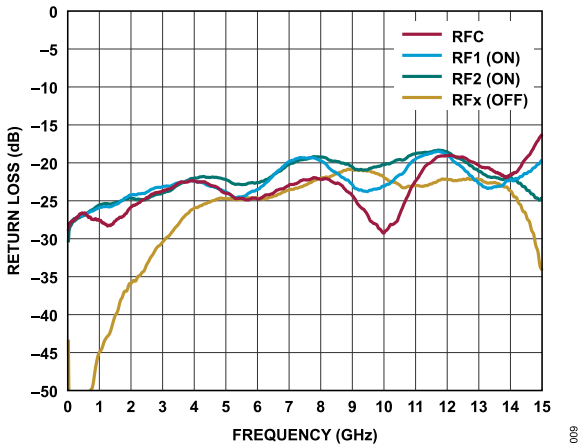

Figure 9. Return Loss vs. Frequency

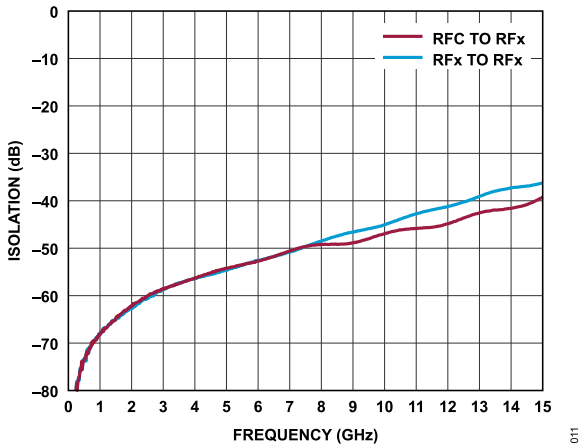

Figure 11. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION, RF IMBALANCE, AND GROUP DELAY

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTL} = 0 V or 3.3 V, T_{CASE} = 25°C, and a 100 Ω differential system, unless otherwise noted. RF1 refers to the RF1P and RF1N differential pair, and RF2 refers to the RF2P and RF2N differential pair.

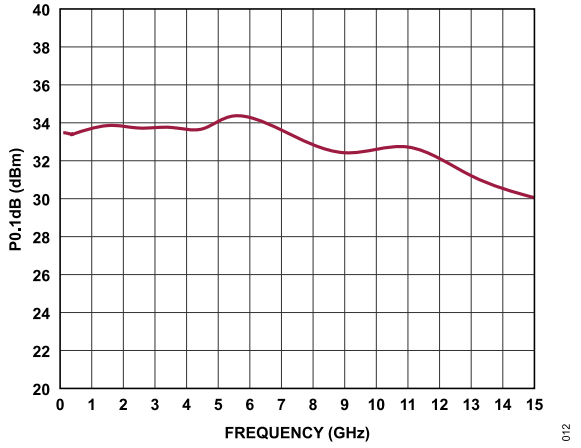

Figure 12. P0.1 dB vs. Frequency

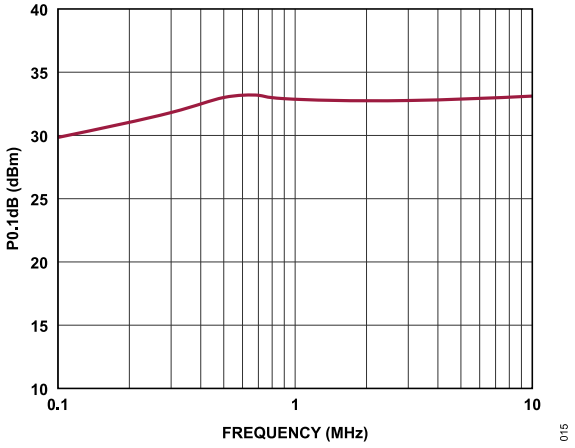

Figure 15. P0.1 dB vs. Frequency, Low-Frequency Detail

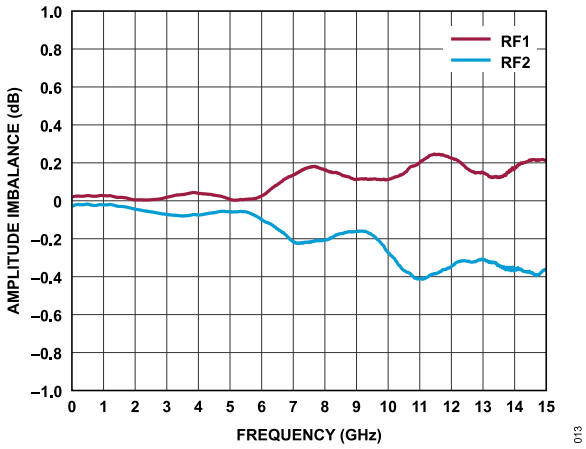

Figure 13. Amplitude Imbalance vs. Frequency, RF1 and RF2

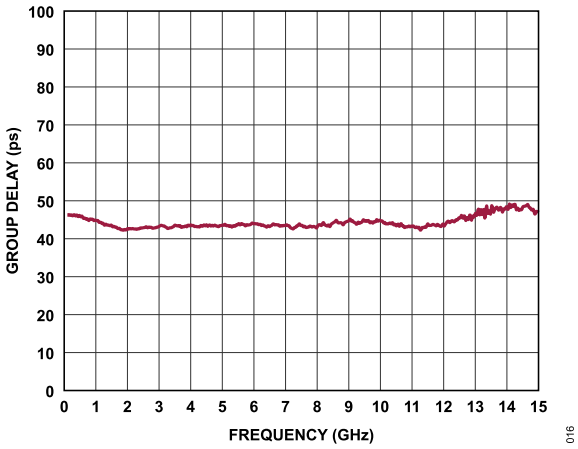

Figure 16. Group Delay vs. Frequency

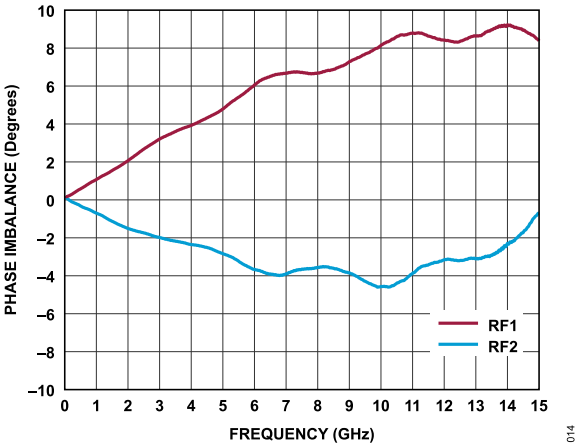

Figure 14. Phase Imbalance vs. Frequency, RF1 and RF2

THEORY OF OPERATION

The ADRF5063 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS-/LVTTL-compatible control interface. The driver features two digital control input pins, EN and VCTL. When EN is low, the ADRF5063 is in the all off state, meaning that both RFC to RF1 and RFC to RF2 paths are in an isolation state. When EN is high, the logic level applied to the VCTL pin determines which RF port is in the insertion loss state and which RF port is in the isolation state (see Table 7).

RF INPUT AND OUTPUT

The RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to differential 100 Ω impedance. For single-ended 50 Ω applications, contact Analog Devices, Inc., Technical Support.

When the EN pin is logic high, the logic level applied to the VCTL pin determines which RF port is in the insertion loss state and which RF port is in the isolation state. The insertion loss path conducts the input RF signal pair between the RFC pair and the selected RF1 and RF2 pairs.

When the EN pin is logic low, the switch is in an all off state regardless of the logic state of the VCTL pin. Both the RF1 to RFC path and the RF2 to RFC path are in an isolation state. The isolation path provides high loss between the insertion loss path and the unselected RF throw pair. The unselected RF throw ports are terminated to internal differential 100 Ω resistors.

The ADRF5063 is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or to the selected RF throw port.

POWER SUPPLY

The ADRF5063 requires a positive supply voltage applied to the VDD pin, and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and ensure that the supply is in the specified range.
3. Power up VSS.
4. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
5. Apply signals to the RF input port. The design is bidirectional; the input signal can be applied to the RFC port while the RF throw ports are outputs or vice versa.

The ideal power-down sequence is the reverse of the previous ideal power-up sequence.

Single-Supply Operation

The ADRF5063 can operate with a single positive supply voltage applied to the VDD pin, and the VSS pin connected to ground. However, some performance differences can occur in the input compression, input third-order intercept, and timing specifications. See Table 2 for further details.

Table 7. Control Voltage Truth Table

Digital Control Inputs		RF Paths[1]	
EN	VCTL	RFC to RF1	RFC to RF2
High	Low	Isolation (off)	Insertion loss (on)
High	High	Insertion loss (on)	Isolation (off)
Low	Low or high	Isolation (off)	Isolation (off)

[1] RFC refers to the RFCP and RFCN differential pair, RF1 refers to the RF1P and RF1N differential pair, and RF2 refers to the RF2P and RF2N differential pair.

APPLICATIONS INFORMATION

The ADRF5063 has two power supply pins (VDD and VSS) and two control pins (VCTL and EN). Figure 17 shows the external components and connections for the supply and control pins. The VDD and VSS pins are decoupled with 100 pF multilayer ceramic capacitors. The ADRF5063 pinout allows the placement of decoupling capacitors close to the device. No other external components are needed for bias and operation, except for DC blocking capacitors on the RFCx, RF1x, and RF2x pins when the RF lines are biased at a voltage different than 0 V. For more details, see the Pin Configuration and Function Descriptions section.

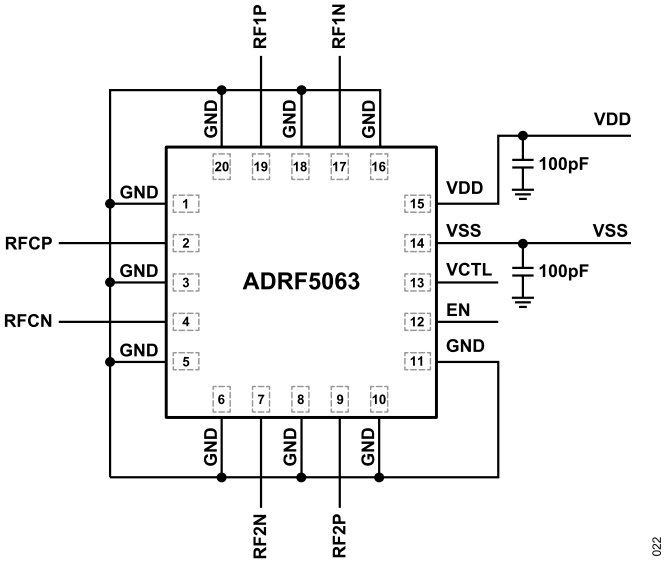

Figure 17. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50 Ω characteristic impedance on the PCB. Figure 18 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. The RF trace with a 14 mil width and a 7 mil clearance is recommended for 1.5 mil finished copper thickness.

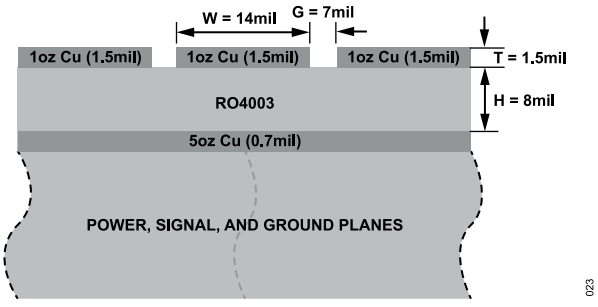

Figure 18. Example PCB Stack-Up

Figure 19 shows the routing of the RF traces, supply, and control signals from the ADRF5063. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the ADRF5063 is the bottom side.

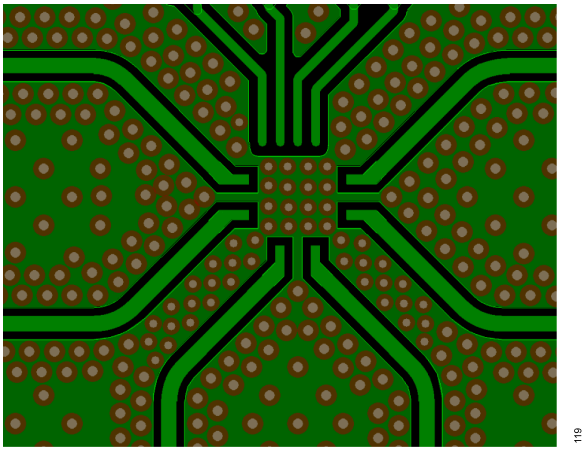

Figure 19. PCB Routings

Figure 20 shows the recommended layout from the RF pins of the ADRF5063 to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to the device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width till the package edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

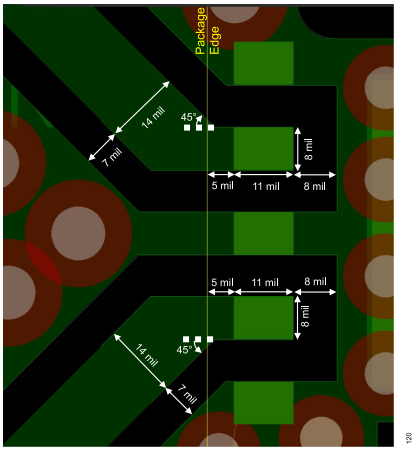

Figure 20. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design and for further recommendations, contact Analog Devices, Inc., Technical Support.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CC-20-15	LGA	20-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5063BCCZN	−40°C to +105°C	20-Terminal LGA	CC-20-15
ADRF5063BCCZN-R7	−40°C to +105°C	20-Terminal LGA	CC-20-15

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Table 8. Evaluation Boards

Model[1]	Description
ADRF5063-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.