Data Sheet

AD7606B

8-Channel DAS with 16-Bit, 800 kSPS Bipolar Input, Simultaneous Sampling ADC

FEATURES

- 16-bit ADC with 800 kSPS on all channels
- Input buffer with 5 MΩ analog input impedance (R_{IN})
- Single 5 V analog supply and 1.71 V to 3.6 V V_{DRIVE} supply
- Per channel selectable analog input ranges
  - Single-ended, bipolar: ±10 V, ±5 V, and ±2.5 V
- Flexible digital filter, oversampling ratio up to 256
- −40°C to +125°C operating temperature range
- ±21 V input clamp protection with 8 kV ESD
- Pin to pin compatible with the AD7606
- 1 ppm/°C typical positive and negative full-scale error drift
- Calibration and diagnostics features available in software mode
- ≤22 LSB (typical) open circuit code error (R_{PD} = 10 kΩ)

CALIBRATION AND DIAGNOSTICS

- Per channel system phase, offset, and gain calibration
- Analog input open circuit detection feature
- Self diagnostics and monitoring features
- CRC error checking on read/write data and registers

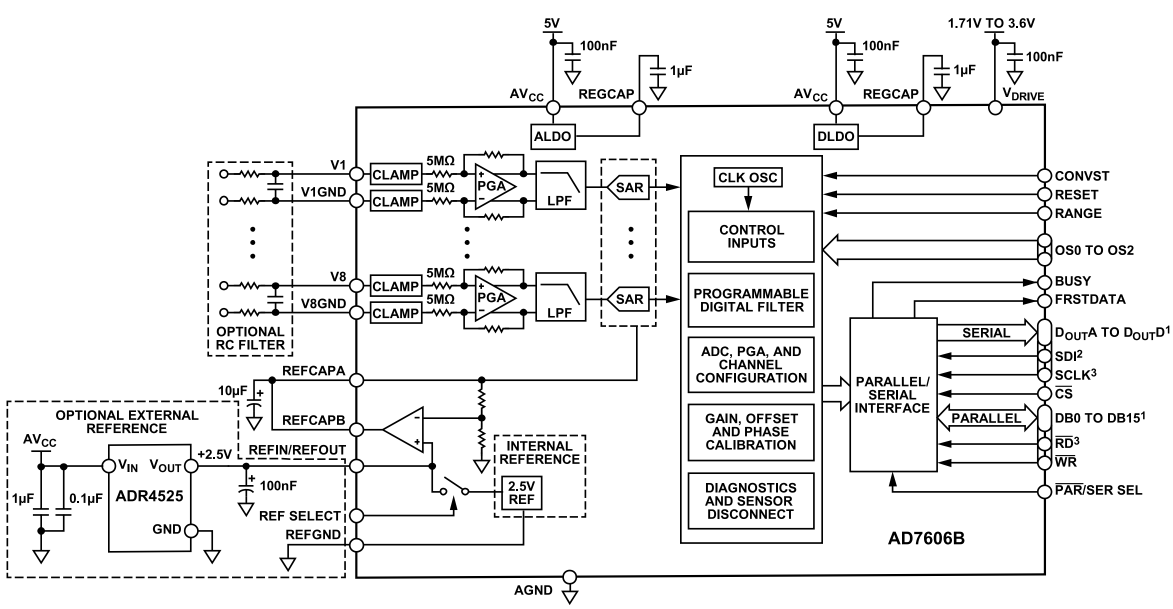
APPLICATIONS

- Power line monitoring
- Protective relays
- Multiphase motor control
- Instrumentation and control systems
- Data acquisition systems

COMPANION PRODUCTS

- Voltage references: ADR4525, LT6657, LTC6655
- Digital isolators: ADuM142E, ADuM6422A, ADuM5020, AD-uM5028
- AD7606x family software model
- Additional companion products on the AD7606B product page.

FUNCTIONAL BLOCK DIAGRAM



[1]D_{OUT}A TO D_{OUT}D ARE SINGLE FUNCTIONS OF MULTIFUNCTION PINS, DB7/D_{OUT}A TO DB10/D_{OUT}D.
[2]SDI IS A SINGLE FUNCTION OF THE DB11/SDI MULTIFUNCTION PIN.
[3]RD AND SCLK ARE SINGLE FUNCTIONS OF THE RD/SCLK MULTIFUNCTION PIN.

Figure 1. Functional Block Diagram

Rev. B

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

6/2025—Rev. A to Rev. B

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GENERAL DESCRIPTION

The AD7606B is a 16-bit, simultaneous sampling, analog-to-digital data acquisition system (DAS) with eight channels. Each channel contains analog input clamp protection, a programmable gain amplifier (PGA), a low-pass filter (LPF), and a 16-bit successive approximation register (SAR), analog-to-digital converter (ADC). The AD7606B also contains a flexible digital filter, a low drift, 2.5 V precision reference and a reference buffer to drive the ADC and flexible parallel and serial interfaces.

The AD7606B operates from a single 5 V supply and accommodates ±10 V, ±5 V, and ±2.5 V true bipolar input ranges when sampling at throughput rates of 800 kSPS for all channels.

The input clamp protection tolerates voltages up to ±21 V. The AD7606B has a 5 MΩ analog input impedance, resulting in less than 20 LSB bipolar zero code when the input signal is disconnected and pulled ground through a 10 kΩ external resistor. The single supply operation, on-chip filtering, and high input impedance eliminate the need for external driver op amps, which require bipolar supplies. For applications with lower throughput rates, the AD7606B flexible digital filter can be used to improve noise performance.

In hardware mode, the AD7606B is fully compatible with the AD7606. In software mode, the following advanced features are available:

- Additional ±2.5 V analog input range
- Analog input range (±10 V, ±5 V, and ±2.5 V), selectable per channel
- Additional oversampling (OS) options, up to OS × 256
- System gain, system offset, and system phase calibration per channel
- Analog input open circuit detector
- Diagnostic multiplexer
- Monitoring functions (serial peripheral interface (SPI), invalid read/write, cyclic redundancy check (CRC), overvoltage and undervoltage events, busy stuck monitor, and reset detection)

Note that throughout this data sheet, multifunction pins, such as the $\overline{RD}$/SCLK pin, are referred to either by the entire pin name or by a single function of the pin, for example, the SCLK pin, when only that function is relevant.

Table 1. Bipolar Input, Simultaneous Sampling, Pin-to-Pin Compatible Family of Devices

Input Type	Resolution (Bits)	R_{IN}[1] = 1 MΩ, 200 kSPS	R_{IN} = 5 MΩ, 800 kSPS	R_{IN} = 1 MΩ, 1 MSPS	Number of Channels
Single-Ended	18	AD7608		AD7606C-18[2]	8
	16	AD7606	AD7606B[2]	AD7606C-16[2]	8
		AD7606-6			6
		AD7606-4			4
	14	AD7607			8
True Differential	18	AD7609		AD7606C-18[2]	8
	16			AD7606C-16[2]	8

[1] R_{IN} is input impedance.

[2] This state-of-the-art device is recommended for newer designs as an alternative to the AD7606, AD7608, and AD7609.

SPECIFICATIONS

Voltage reference (V_{REF}) = 2.5 V external and internal, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V, logic supply voltage (V_{DRIVE}) = 1.71 V to 3.6 V, sample frequency (f_{SAMPLE}) = 800 kSPS, with no OS, T_A = −40°C to +125°C, single-ended input, and all input voltage ranges, unless otherwise noted.

Table 2. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	Input frequency (f_{IN}) = 1 kHz sine wave, unless otherwise noted				
Signal-to-Noise Ratio (SNR)[1]	No OS, ±10 V range	87.5	89.5		dB
	No OS, ±5 V range	86.5	88.5		dB
	No OS, ±2.5 V range	83.5	86		dB
	Oversampling ratio (OSR) = 16×, ±10 V range	92	93.5		dB
	OSR = 16×, ±5 V range	90.5	92		dB
	OSR = 16×, ±2.5 V range	87.5	89		dB
Total Harmonic Distortion (THD)	All input ranges				
	f_{SAMPLE} = 200 kSPS		−105	−94	dB
	f_{SAMPLE} = 800 kSPS		−100	−90	dB
Signal-to-Noise-and-Distortion	No OS, ±10 V range	86.5	88.5		dB
	No OS, ±5 V range	85.5	87.7		dB
	No OS, ±2.5 V range	83	85.5		dB
	OSR = 16×, ±10 V range	89	92		dB
	OSR = 16×, ±5 V range	89	91.3		dB
	OSR = 16×, ±2.5 V range	86.5	88.7		dB
Spurious-Free Dynamic Range (SFDR)			−104		dB
Channel-to-Channel Isolation	f_{IN} on unselected channels up to 160 kHz		−110		dB
Full-Scale Step Settling Time	0.01% of full scale				
	±10 V range		70		µs
	±5 V range		110		µs
	±2.5V range		130		µs
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±10 V range		22.5		kHz
	−3 dB, ±5 V range		13.5		kHz
	−3 dB, ±2.5 V range		11.5		kHz
	−0.1 dB, ±10 V range		3		kHz
	−0.1 dB, ±5 V range		2		kHz
	−0.1 dB, ±2.5 V range		2		kHz
Phase Delay	±10 V range		7.5		µs
	±5 V range		12		µs
	±2.5 V range		14		µs
Phase Delay Matching	±10 V range			240	ns
	±5 V range			365	ns
	±2.5 V range			445	ns
DC ACCURACY					
Resolution	No missing codes	16			Bits
Differential Nonlinearity (DNL)			±0.5	±0.99	LSB[2]
Integral Nonlinearity (INL)	f_{SAMPLE} = 800 kSPS		±1	±2.5	LSB[2]
	f_{SAMPLE} = 200 kSPS		±1	±2	LSB[2]
Total Unadjusted Error (TUE)	External reference		±3	±47	LSB
Positive and Negative Full-Scale (FS) Error[3]			±2	±30	LSB
	R_{FILTER}[4] = 20 kΩ, system gain calibration disabled		126		LSB
	R_{FILTER}Footnote. = 0 kΩ to 65 kΩ, system gain calibration enabled		4		LSB

SPECIFICATIONS

Table 2. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Positive and Negative FS Error Drift			±1	±3	ppm/°C
Positive and Negative FS Error Matching			3	20	LSB
Bipolar Zero Code Error			±1	±20	LSB[2]
	T_A = −40°C to +85°C		±1	±14	LSB
Bipolar Zero Code Error Drift			±0.5	±2.5	ppm/°C
Bipolar Zero Code Error Matching			1.5	23	LSB[2]
	T_A = −40°C to +85°C		1.4	14	LSB
Open Circuit Code Error	Pull-down resistor (R_{PD})[5] = 10 kΩ, ±10 V range		±12	±30	LSB
	R_{PD} = 10 kΩ, ±10 V range, T_A = −40°C to +85°C		±12	±20	LSB
	R_{PD} = 10 kΩ, ±5 V range		±17	±35	LSB
	R_{PD} = 10 kΩ, ±5 V range, T_A = −40°C to +85°C		±17	±25	LSB
	R_{PD} = 10 kΩ, ±2.5 V range		±22	±40	LSB
	R_{PD} = 10 kΩ, ±2.5 V range, T_A = −40°C to +85°C		±22	±30	LSB
SYSTEM CALIBRATION					
Positive Full-Scale (PFS) and Negative Full-Scale (NFS) Calibration Range	Series resistor in front of the Vx+ and VxGND inputs	0		64	kΩ
Offset Calibration Range		−128		+127	LSB
Phase Calibration Range		0		318.75	µs
PFS and NFS Error	After gain calibration		±5		LSB
Offset Error	After offset calibration		±0.5		LSB
Phase Error	After phase calibration		±1		µs
ANALOG INPUT					
Input Voltage Ranges	Vx − VxGND				
	±10 V range	−10		+10	V
	±5 V range	−5		+5	V
	±2.5 V range	−2.5		+2.5	V
Input Voltage Ranges	VxGND − AGND				
	±10 V range	−0.7		+1.9	V
	±5 V range	−0.1		+2.7	V
	±2.5 V range	−0.1		+3.1	V
Analog Input Current	See the Typical Performance Characteristics section		$(V_{IN} − 2)/R_{IN}$		µA
Input Impedance (R_{IN})[6]			5		MΩ
Input Capacitance (C_{IN})[7]			5		pF
Input Impedance Drift			±1	±25	ppm/°C
REFERENCE INPUT AND OUTPUT					
Reference Input Voltage	External reference	2.495	2.5	2.505	V
DC Leakage Current				±0.12	µA
Input Capacitance (C_{IN})[7]			7.5		pF
Reference Output Voltage	Internal reference, T_A = 25°C	2.4975	2.5	2.5025	V
Reference Temperature Coefficient			±3	±10	ppm/°C
Reference Voltage to the ADC	REFCAPA (Pin 44) and REFCAPB (Pin 45)	4.39		4.41	V
LOGIC INPUTS					
Input High Voltage (V_{INH})		0.7 × V_{DRIVE}			V
Input Low Voltage (V_{INL})				0.3 × V_{DRIVE}	V
Input Current (I_{IN})				±1	µA
Input Capacitance[7]			5		pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	Current source (I_{SOURCE}) = 100 µA	V_{DRIVE} − 0.2			V

SPECIFICATIONS

Table 2. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Low Voltage (V_{OL})	Current sink (I_{SINK}) = 100 µA			0.2	V
Floating State Leakage Current				±1	µA
Output Capacitance (C_{OUT})[7]			5		pF
Output Coding	Twos complement				N/A[8]
CONVERSION RATE					
Conversion Time	See Table 3		0.75		µs
Acquisition Time (t_{ACQ})[9]			0.5		µs
Throughput Rate	Per channel			800	kSPS
POWER REQUIREMENTS					
AV_{CC}		4.75	5	5.25	V
V_{DRIVE}		1.71		3.6	V
REGCAP		1.875		1.93	V
AV_{CC} Current (I_{AVCC})					
Normal Mode (Static)			7.5	9.5	mA
Normal Mode (Operational)	f_{SAMPLE} = 800 kSPS		43	47.5	mA
	f_{SAMPLE} = 10 kSPS		8	10	mA
Standby			3.5	4.5	mA
Shutdown Mode			0.5	5	µA
V_{DRIVE} Current (I_{DRIVE})					
Normal Mode (Static)			1.8	3.5	µA
Normal Mode (Operational)	f_{SAMPLE} = 800 kSPS		1.1	1.5	mA
	f_{SAMPLE} = 10 kSPS		30	75	µA
Standby			1.6	3	µA
Shutdown Mode			0.8	2	µA
Power Dissipation					
Normal Mode (Static)			40	50	mW
Normal Mode (Operational)	f_{SAMPLE} = 800 kSPS		230	255	mW
	f_{SAMPLE} = 10 kSPS		42	50	mW
Standby			18	24	mW
Shutdown Mode			2.5	25	µW

1 No OS means no oversampling is applied.

2 LSB means least significant bit. With a ±2.5 V input range, 1 LSB = 76.293 µV. With a ±5 V input range, 1 LSB = 152.58 µV. With a ±10 V input range, 1 LSB = 305.175 µV.

3 These specifications include the full temperature range variation and contribution from the reference buffer.

4 R_{FILTER} is a resistor placed in a series to the analog input front end. See Figure 58.

5 See Figure 61.

6 Input impedance variation is factory trimmed and accounted for in the System Gain Calibration section.

7 Not production tested. Sample tested during initial release to ensure compliance.

8 N/A means not applicable.

9 The ADC input is settled by the internal PGA. Therefore, the t_{ACQ} time is the time between the end of the conversion and the start of the next conversion with no impact on external components.

SPECIFICATIONS

TIMING SPECIFICATIONS

Universal Timing Specifications

AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 1.71 V to 3.6 V, V_{REF} = 2.5 V external reference and internal reference, and T_A = −40°C to +125°C, unless otherwise noted. Interface timing is tested using a load capacitance of 20 pF, dependent on V_{DRIVE} and load capacitance for serial interface.

Table 3. Universal Timing Specifications

Parameter	Min	Typ	Max	Unit	Description
t_{CYCLE}	1.25			µs	Minimum time between consecutive CONVST rising edges (excluding oversampling modes)[1]
t_{LP_CNV}	10			ns	CONVST low pulse width
t_{HP_CNV}	10			ns	CONVST high pulse width
$t_{D\_CNV\_BSY}$					CONVST high to BUSY high delay time
			20	ns	V_{DRIVE} ≥ 2.7 V
			25	ns	V_{DRIVE} < 2.7 V
t_{S_BSY}	0			ns	Minimum time from BUSY falling edge to $\overline{RD}$ falling edge setup time (in parallel interface) or to MSB being available on D_{OUT}x line (in serial interface)
t_{D_BSY}	25			ns	Minimum time between last $\overline{RD}$ falling edge (in parallel interface) or last LSB being clocked out (serial interface) and the following BUSY falling edge, read during conversion
t_{ACQ}	0.40			µs	Acquisition time, which is effectively the time from end of conversion to start of new conversion
t_{CONV}	0.65		0.85	µs	Conversion time, no oversampling
	2.2		2.3	µs	Oversampling by 2
	4.65		4.8	µs	Oversampling by 4
	9.6		9.9	µs	Oversampling by 8
	19.4		20	µs	Oversampling by 16
	39.2		40.2	µs	Oversampling by 32
	78.7		80.8	µs	Oversampling by 64
	157.6		161.9	µs	Oversampling by 128
	315.6		324	µs	Oversampling by 256
t_{RESET}					
Partial Reset	55		2000	ns	Partial RESET high pulse width
Full Reset	3000			ns	Full RESET high pulse width
t_{DEVICE_SETUP}[2]				µs	Time between RESET falling edge and first CONVST rising edge
Partial Reset	50			ns	
Full Reset	253			µs	
t_{WAKE_UP}					Wake-up time after standby/shutdown mode
Standby	1			µs	
Shutdown	10			ms	
$t_{POWER-UP}$	10			ms	Time between stable AV_{CC}/V_{DRIVE} and assertion of RESET

1 Applies to serial mode when all four D_{OUT}x lines are selected.

2 For the first RESET edge after power up, this time will be longer, depending on $t_{POWER-UP}$ time. The shorter the $t_{POWER-UP}$ time, the longer the t_{DEVICE_SETUP} ($t_{POWER-UP}$ + t_{DEVICE_SETUP} > 2 sec.)

SPECIFICATIONS

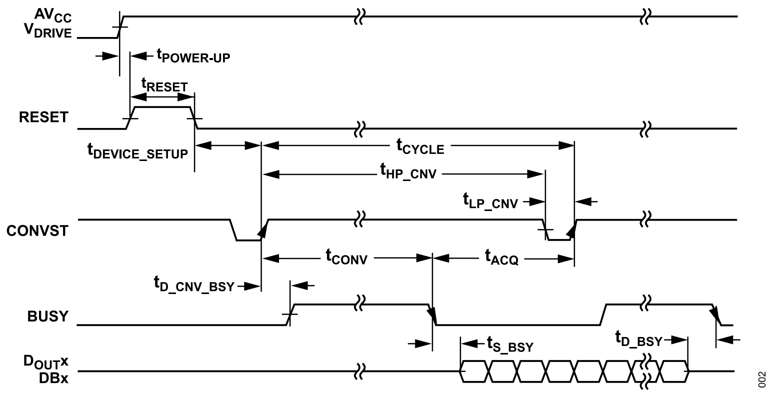


Figure 2. Universal Timing Diagram

Parallel Mode Timing Specifications

Table 4. Parallel Mode Timing Specifications

Parameter	Min	Typ	Max	Unit	Description
$t_{S\_\overline{CS}\_\overline{RD}}$	0			ns	$\overline{\text{CS}}$ falling edge to $\overline{\text{RD}}$ falling edge setup time
$t_{H\_\overline{RD}\_\overline{CS}}$	0			ns	$\overline{\text{RD}}$ rising edge to $\overline{\text{CS}}$ rising edge hold time
$t_{HP\_\overline{RD}}$	10			ns	$\overline{\text{RD}}$ high pulse width
$t_{LP\_\overline{RD}}$	10			ns	$\overline{\text{RD}}$ low pulse width
$t_{HP\_\overline{CS}}$	10			ns	$\overline{\text{CS}}$ high pulse width
$t_{D\_\overline{CS}\_DB}$			35	ns	Delay from $\overline{\text{CS}}$ until DBx three-state disabled
$t_{H\_\overline{CS}\_DB}$	0			ns	$\overline{\text{CS}}$ to DBx hold time
$t_{D\_\overline{RD}\_DB}$					Data access time after falling edge of $\overline{\text{RD}}$
			27	ns	$V_{DRIVE} \geq 2.7$ V
			37	ns	$V_{DRIVE} < 2.7$ V
$t_{H\_\overline{RD}\_DB}$	12			ns	Data hold time after falling edge of $\overline{\text{RD}}$
$t_{DHZ\_\overline{CS}\_DB}$			40	ns	$\overline{\text{CS}}$ rising edge to DBx high impedance
$t_{CYC\_\overline{RD}}$					$\overline{\text{RD}}$ falling edge to next $\overline{\text{RD}}$ falling edge
	30			ns	$V_{DRIVE} \geq 2.7$ V
	40			ns	$V_{DRIVE} < 2.7$ V
$t_{D\_\overline{CS}\_FD}$			26	ns	Delay from $\overline{\text{CS}}$ falling edge until FRSTDATA three-state disabled
$t_{D\_\overline{RD}\_FDH}$			30	ns	Delay from $\overline{\text{RD}}$ falling edge until FRSTDATA high
$t_{D\_\overline{RD}\_FDL}$			30	ns	Delay from $\overline{\text{RD}}$ falling edge until FRSTDATA low
$t_{DHZ\_\overline{CS}\_FD}$			28	ns	Delay from $\overline{\text{CS}}$ rising edge until FRSTDATA three-state enabled
$t_{S\_\overline{CS}\_\overline{WR}}$	0			ns	$\overline{\text{CS}}$ to $\overline{\text{WR}}$ setup time
$t_{HP\_\overline{WR}}$	213			ns	$\overline{\text{WR}}$ high pulse width
$t_{LP\_\overline{WR}}$					$\overline{\text{WR}}$ low pulse width
	88			ns	$V_{DRIVE} \geq 2.7$ V
	213			ns	$V_{DRIVE} < 2.7$ V
$t_{H\_\overline{WR}\_\overline{CS}}$	0			ns	$\overline{\text{WR}}$ hold time
$t_{S\_DB\_\overline{WR}}$	5			ns	Configuration data to $\overline{\text{WR}}$ setup time
$t_{H\_\overline{WR}\_DB}$	5			ns	Configuration data to $\overline{\text{WR}}$ hold time
$t_{CYC\_\overline{WR}}$	230			ns	Configuration data settle time, $\overline{\text{WR}}$ rising edge to next $\overline{\text{WR}}$ rising edge

SPECIFICATIONS

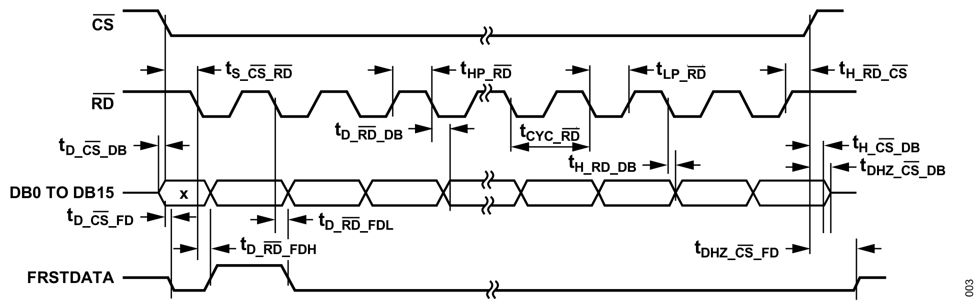


Figure 3. Parallel Mode Read Timing Diagram, Separate CS and RD Pulses

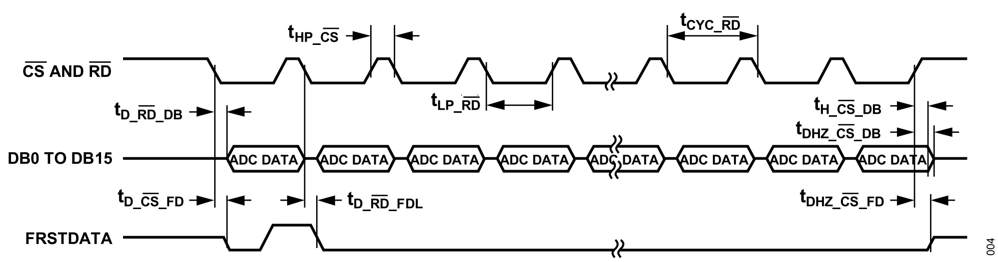


Figure 4. Parallel Mode Read Timing Diagram, Linked CS and RD

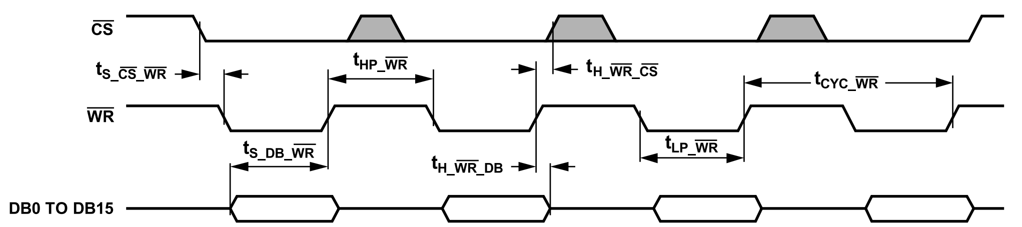


Figure 5. Parallel Mode Write Operation Timing Diagram

Serial Mode Timing Specifications

Table 5. Serial Mode Timing Specifications

Parameter	Min	Typ	Max	Unit	Description
f_{SCLK}					SCLK frequency, $f_{SCLK} = 1/t_{SCLK}$
			60	MHz	$V_{DRIVE} \geq 2.7$ V
			40	MHz	$V_{DRIVE} < 2.7$ V
t_{SCLK}	$1/f_{SCLK}$			μs	Minimum SCLK period
$t_{S\_\overline{CS}\_SCK}$	2			ns	$\overline{CS}$ to SCLK falling edge setup time
$t_{H\_SCK\_\overline{CS}}$	2			ns	SCLK to $\overline{CS}$ rising edge hold time
t_{LP_SCK}	$0.4 \times t_{SCLK}$			ns	SCLK low pulse width
t_{HP_SCK}	$0.4 \times t_{SCLK}$			ns	SCLK high pulse width
$t_{D\_\overline{CS}\_DO}$					Delay from $\overline{CS}$ until $D_{OUT}x$ three-state disabled
			9	ns	$V_{DRIVE} \geq 2.7$ V
			18	ns	$V_{DRIVE} < 2.7$ V
$t_{D\_SCK\_DO}$					Data out access time after SCLK rising edge
			15	ns	$V_{DRIVE} \geq 2.7$ V
			25	ns	$V_{DRIVE} < 2.7$ V
$t_{H\_SCK\_DO}$	5			ns	Data out hold time after SCLK rising edge

SPECIFICATIONS

Table 5. Serial Mode Timing Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Description
$t_{S\_SDI\_SCK}$	8			ns	Data in setup time before SCLK falling edge
$t_{H\_SCK\_SDI}$	0			ns	Data in hold time after SCLK falling edge
$t_{DHZ\_\overline{CS}\_DO}$					$\overline{CS}$ rising edge to D_{OUT}x high impedance
			7	ns	$V_{DRIVE} \geq 2.7$ V
			22	ns	$V_{DRIVE} < 2.7$ V
$t_{\overline{WR}}$	25			ns	Time between writing and reading the same register or between two writes, if $f_{SCLK} > 50$ MHz
$t_{D\_\overline{CS}\_FD}$			26	ns	Delay from $\overline{CS}$ until D_{OUT}x three-state disabled or delay from $\overline{CS}$ until MSB valid
$t_{D\_SCK\_FDL}$			18	ns	16th SCLK falling edge to FRSTDATA low
t_{DHZ_FD}			28	ns	$\overline{CS}$ rising edge until FRSTDATA three-state enabled

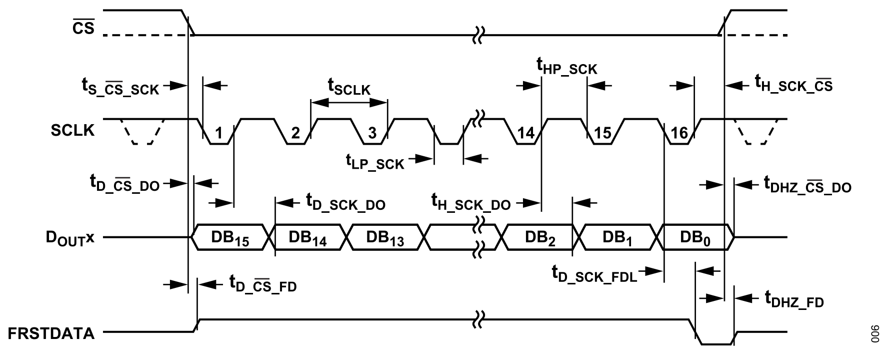


Figure 6. Serial Timing Diagram, ADC Read Mode (Channel 1)

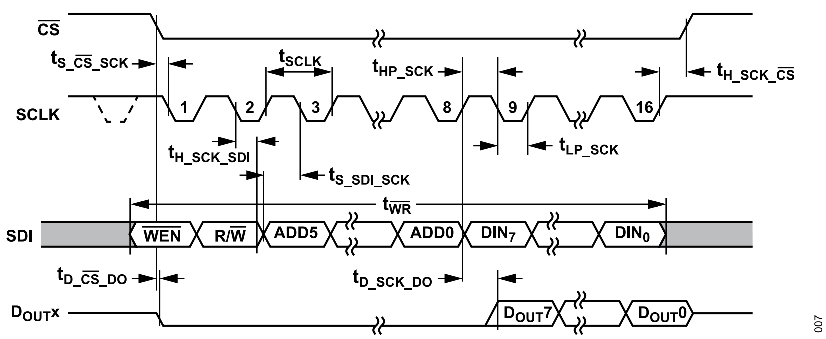


Figure 7. Serial Interface Timing Diagram, Register Map Read/Write Operations

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6. Absolute Maximum Ratings

Parameter	Rating
AV_{CC} to AGND	−0.3 V to +6.5 V
V_{DRIVE} to AGND	−0.3 V to AV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±21 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN/REFOUT to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/Sn Temperature, Soldering	
Reflow (10 sec to 30 sec)	240 (+0)°C
Pb-Free Temperature, Soldering Reflow	260 (+0)°C

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
ST-64-2	40	7	°C/W

[1] Simulated data based on JEDEC 2s2p thermal test PCB in a JEDEC natural convention environment.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

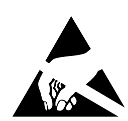
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for AD7606B

Table 8. AD7606B, 64-Lead LQFP

ESD Model	Withstand Threshold (V)	Class
HBM		
All Pins Except Analog Inputs	3500	3A
Analog Input Pins Only	8000	3A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

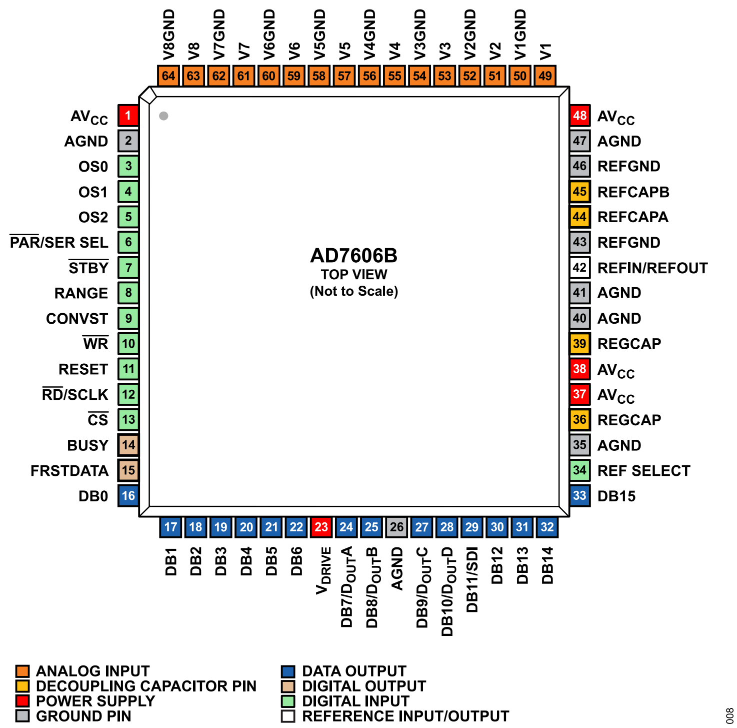


Figure 8. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
1, 37, 38, 48	P	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these supply pins to AGND.
2, 26, 35, 40, 41, 47	P	AGND	Analog Ground. The AGND pins are the ground reference points for all analog circuitry on the AD7606B. All analog input signals and external reference signals must be referred to the AGND pins. All six of the AGND pins must connect to the AGND plane of a system.
3 to 5	DI	OS0 to OS2	Oversampling Mode Pins. OS0 to OS2 select the oversampling ratio or enable software mode (see Table 13 for oversampling pin decoding). See the Digital Filter section for more details about the oversampling mode of operation.
6	DI	$\overline{\text{PAR}}$/SER SEL	Parallel/Serial Interface Selection Input. If the $\overline{\text{PAR}}$/SER SEL pin is tied to a logic low, the parallel interface is selected. If the $\overline{\text{PAR}}$/SER SEL pin is tied to a logic high, the serial interface is selected. See the Digital Interface section for more information on each interface available.
7	DI	$\overline{\text{STBY}}$	Standby Mode Input. In hardware mode, the $\overline{\text{STBY}}$ pin, in combination with the RANGE pin, places the AD7606B in one of two power-down modes: standby mode or shutdown mode. In software mode, the $\overline{\text{STBY}}$ pin is ignored. Therefore, it is recommended to connect the $\overline{\text{STBY}}$ pin to logic high. See the Power-Down Modes section for more information on both hardware mode and software mode.
8	DI	RANGE	Analog Input Range Selection Input. In hardware mode, the RANGE pin determines the input range of the analog input channels (see Table 10). If the $\overline{\text{STBY}}$ pin is at logic low, the RANGE pin determines the power-down mode (see Table 15). In software mode, the RANGE pin is ignored. However, the RANGE pin must be tied high or low.
9	DI	CONVST	Conversion Start Input. When the CONVST pin transitions from low to high, the analog input is sampled on all eight SAR ADCs. In software mode, the CONVST pin can be configured as an external oversampling clock. Providing a low jitter external clock improves the SNR performance for large oversampling ratios. See the External Oversampling Clock section for further details.
10	DI	$\overline{\text{WR}}$	Digital Input. In hardware mode, the $\overline{\text{WR}}$ pin has no function. Therefore, the $\overline{\text{WR}}$ pin can be tied high, tied low, or shorted to CONVST. In software mode, the $\overline{\text{WR}}$ pin is an active low write pin for writing registers using the parallel interface. See the Parallel Interface section for more information.
11	DI	RESET	Reset Input, Active High. Full and partial reset options are available. The type of reset is determined by the length of the reset pulse. Ensure that the device receives a full reset pulse after power-up. See the Reset Functionality section for further details.
12	DI	$\overline{\text{RD}}$/SCLK	Parallel Data Read Control Input ($\overline{\text{RD}}$) when the Parallel Interface is Selected.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Pin Function Descriptions (Continued)

Pin No.	Type[1]	Mnemonic	Description
			Serial Clock Input (SCLK) when the Serial Interface is Selected. See the Digital Interface section for more details.
13	DI	$\overline{CS}$	Chip Select. The $\overline{CS}$ pin is the active low chip select input for ADC data reads or register data reads and writes, in both serial and parallel interfaces. See the Digital Interface section for more details.
14	DO	BUSY	Busy Output. The BUSY pin transitions to a logic high along with the CONVST rising edge. The BUSY output remains high until the conversion process for all channels is complete.
15	DO	FRSTDATA	First Data Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel interface (see Figure 3) or the serial interface (see Figure 6). See the Digital Interface section for more details.
16 to 22	DO/DI	DB0 to DB6	Parallel Output/Input Data Bits. When using the parallel interface, these pins act as three-state parallel digital input and output pins (see the Parallel Interface section). When using the serial interface, tie the pins to AGND. See Table 22 for more details on each data interface and operation mode.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage (1.71 V to 3.6V) supplied at the V_{DRIVE} pin determines the operating voltage of the interface. The V_{DRIVE} pin is nominally at the same supply as the supply of the host interface, that is, the data signal processor (DSP) and field programmable gate array (FPGA).
24	DO/DI	DB7/D_{OUT}A	Parallel Output/Input Data Bit 7 (DB7). When using the parallel interface, DB7/D_{OUT}A pin acts as a three-state parallel digital input/output pin. Serial Interface Data Output Pin (D_{OUT}A). When using the serial interface, DB7/D_{OUT}A pin functions as D_{OUT}A. See Table 22 for more details on each data interface and operation mode.
25	DO/DI	DB8/D_{OUT}B	Parallel Output/Input Data Bit 8 (DB8). When using the parallel interface, DB8/D_{OUT}B pin acts as a three-state parallel digital input and output pin. Serial Interface Data Output Pin (DOUTB).When using the serial interface, DB8/D_{OUT}B pin functions as D_{OUT}B. See Table 22 for more details on each data interface and operation mode.
27	DO/DI	DB9/D_{OUT}C	Parallel Output/Input Data Bit 9 (DB9). When using the parallel interface, DB9/D_{OUT}C pin acts as a three-state parallel digital input and output pin. Serial Interface Data Output Pin (D_{OUT}C).When using the serial interface, this pin functions as D_{OUT}C if in software mode and using the four data output lines option. See Table 22 for more details on each data interface and operation mode.
28	DO/DI	DB10/D_{OUT}D	Parallel Output/Input Data Bit 10 (DB10). When using the parallel interface, DB10/D_{OUT}D pin acts as a three-state parallel digital input/output pin. Serial Interface Data Output Pin (DOUTD). When using serial interface, this pin functions as D_{OUT}D if in software mode and using the four data output lines option. See Table 22 for more details on each data interface and operation mode.
29	DO/DI	DB11/SDI	Parallel Output/Input Data Bit 11 (DB11). When using parallel interface, DB11/SDI pin acts as a three-state parallel digital input and output pin. Serial Data Input (SDI). When using the serial interface in software mode, DB11/SDI pin functions as a serial data input. See Table 22 for more details on each data interface and operation mode.
30 to 33	DO/DI	DB12 to DB15	Parallel Output/Input Data Bits, DB12 to DB15. When using the parallel interface, DB12 to DB15 pins act as three-state parallel digital input and output pins (see the Parallel Interface section). When using the serial interface, tie these pins to AGND.
34	DI	REF SELECT	Internal/External Reference Selection Logic Input. If the REF SELECT pin is set to logic high, the internal reference is selected and enabled. If the REF SELECT pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
36, 39	P	REGCAP	Decoupling Capacitor Pin for Voltage Output from 1.9 V Internal Regulator, Analog Low Dropout (ALDO) and Digital Low Dropout (DLDO). The REGCAP output pins must be decoupled separately to AGND using a 1 µF capacitor.
42	REF	REFIN/REFOUT	Reference Input (REFIN)/Reference Output (REFOUT). The internal 2.5 V reference is available on the REFOUT pin for external use while the REF SELECT pin is set to logic high. Alternatively, by setting the REF SELECT pin to logic low, the internal reference is disabled and an external reference of 2.5 V must be applied to this input (REFIN). A 100 nF capacitor must be applied from the REFIN pin to ground, close to the REFGND pins, for both internal and external reference options. See the Reference section for more details.
43, 46	REF	REFGND	Reference Ground Pins. The REFGND pins must be connected to AGND.
44, 45	REF	REFCAPA, REFCAPB	Reference Buffer Output Force and Sense Pins. The REFCAPA and REFCAPB pins must be connected together and decoupled to AGND using a low effective series resistance (ESR), 10 µF ceramic capacitor. The voltage on the REFCAPA and REFCAPB pins is typically 4.4 V.
49	AI	V1	Channel 1 Positive Analog Input Pin.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Pin Function Descriptions (Continued)

Pin No.	Type[1]	Mnemonic	Description
50	AI GND	V1GND	Channel 1 Negative Analog Input Pin.
51	AI	V2	Channel 2 Positive Analog Input Pin.
52	AI GND	V2GND	Channel 2 Negative Analog Input Pin.
53	AI	V3	Channel 3 Positive Analog Input Pin.
54	AI GND	V3GND	Channel 3 Negative Analog Input Pin.
55	AI	V4	Channel 4 Positive Analog Input Pin.
56	AI GND	V4GND	Channel 4 Negative Analog Input Pin.
57	AI	V5	Channel 5 Positive Analog Input Pin.
58	AI GND	V5GND	Channel 5 Negative Analog Input Pin.
59	AI	V6	Channel 6 Positive Analog Input Pin.
60	AI GND	V6GND	Channel 6 Negative Analog Input Pin.
61	AI	V7	Channel 7 Positive Analog Input Pin.
62	AI GND	V7GND	Channel 7 Negative Analog Input Pin.
63	AI	V8	Channel 8 Positive Analog Input Pin.
64	AI GND	V8GND	Channel 8 Negative Analog Input Pin.

[1] P is power supply, DI is digital input, DO is digital output, REF is reference input and output, AI is analog input, and GND is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

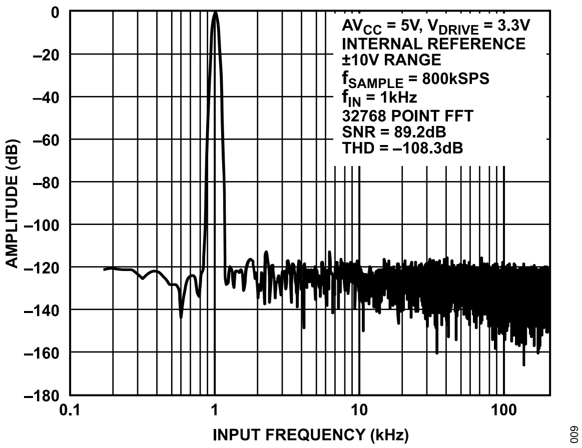


Figure 9. Fast Fourier Transform (FFT), ±10 V Range

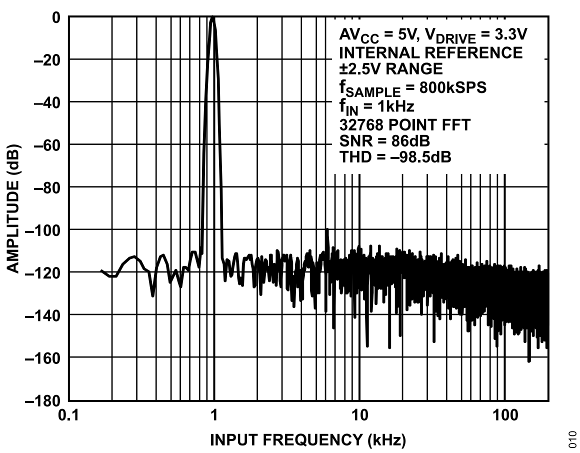


Figure 10. FFT, ±2.5 V Range

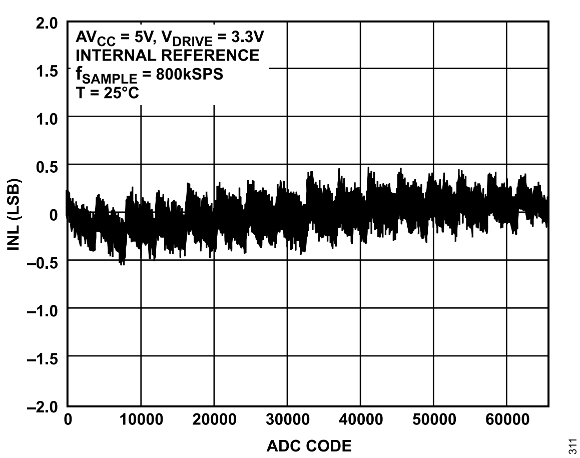


Figure 11. Typical INL, ±10 V Range

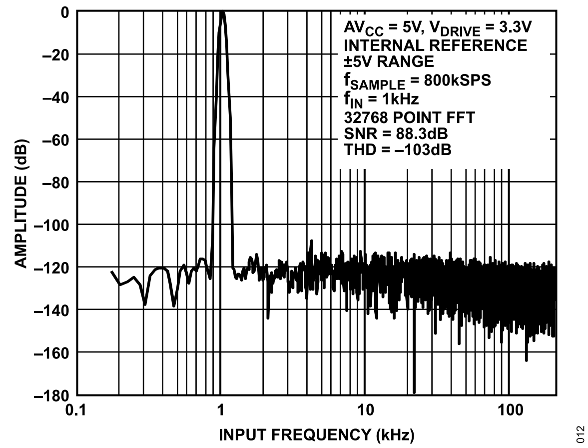


Figure 12. FFT, ±5 V Range

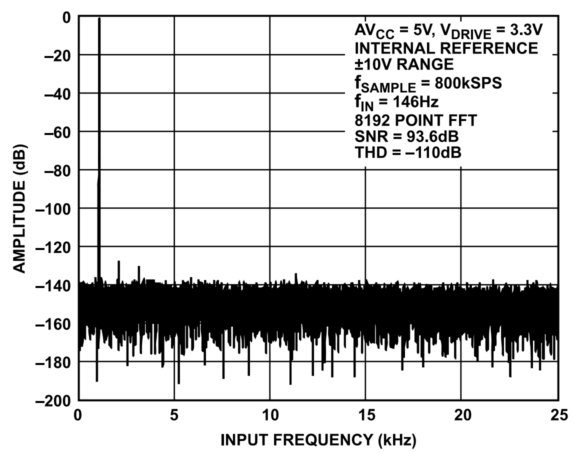


Figure 13. FFT Oversampling by 16, ±10 V Range

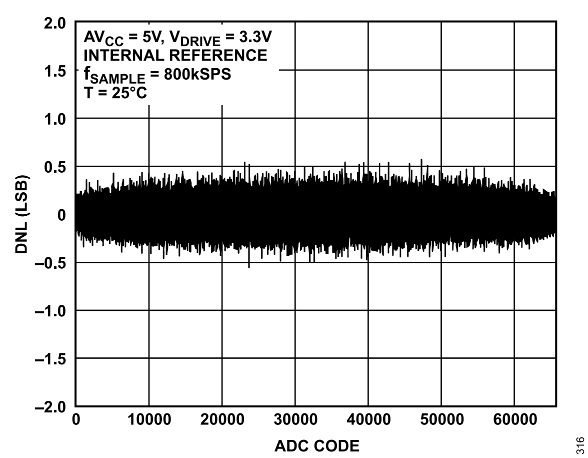


Figure 14. Typical DNL

TYPICAL PERFORMANCE CHARACTERISTICS

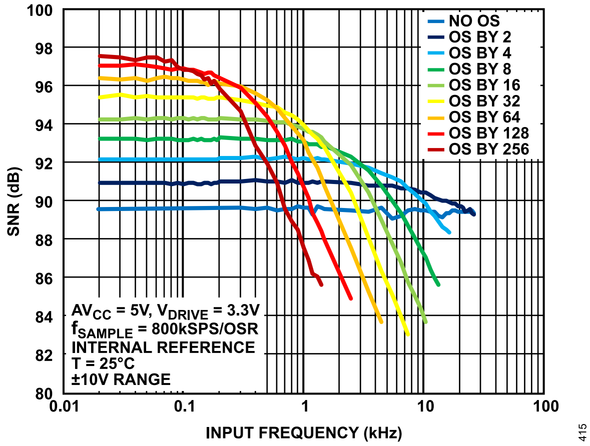


Figure 15. SNR vs. Input Frequency for Different OSR Values, ±10 V Range, Internal OS Clock

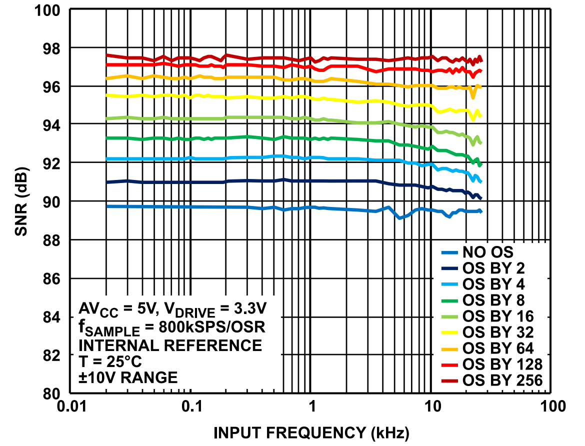


Figure 18. SNR vs. Input Frequency for Different OSR Values, ±10 V Range, External OS Clock

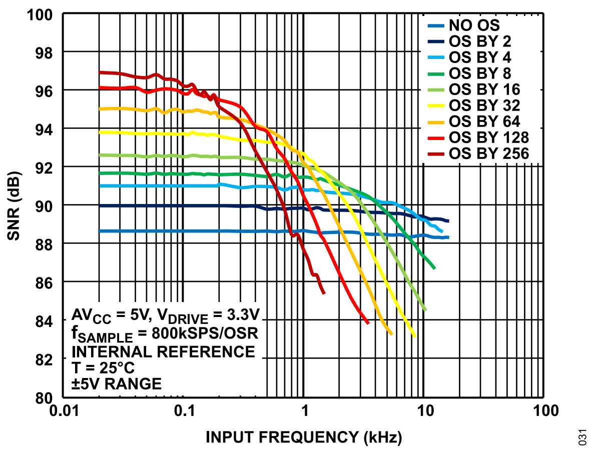


Figure 16. SNR vs. Input Frequency for Different OSR Values, ±5 V Range, Internal OS Clock

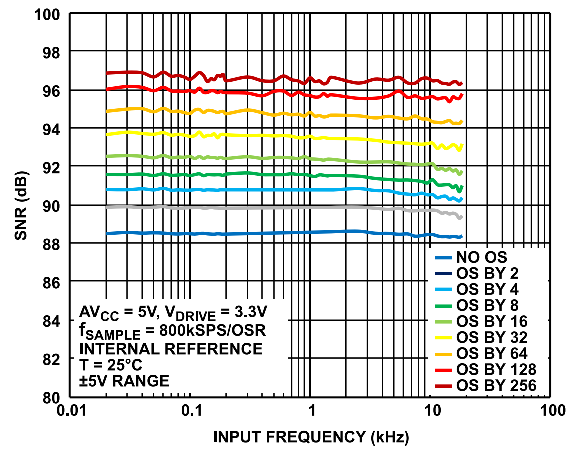


Figure 19. SNR vs. Input Frequency for Different OSR Values, ±5 V Range, External OS Clock

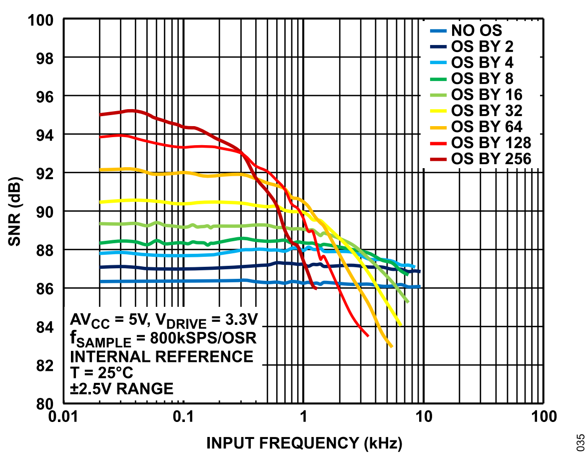


Figure 17. SNR vs. Input Frequency for Different OSR Values, ±2.5 V Range, Internal OS Clock

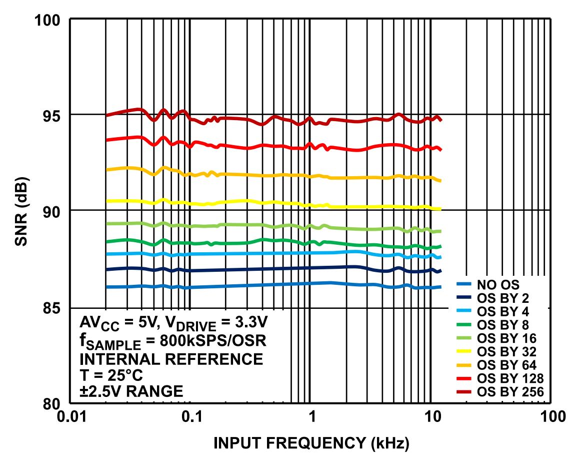


Figure 20. SNR vs. Input Frequency for Different OSR Values, ±2.5 V Range, External OS Clock

TYPICAL PERFORMANCE CHARACTERISTICS

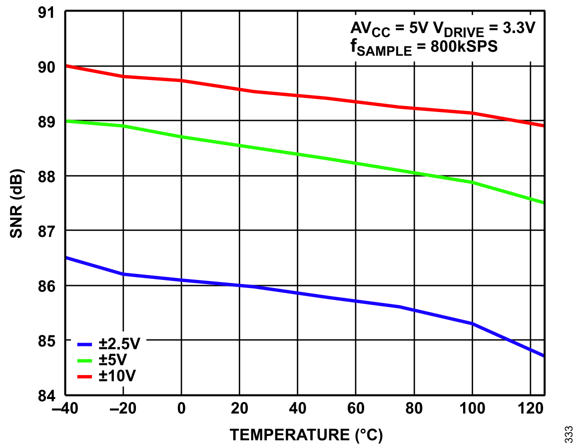


Figure 21. SNR vs. Temperature

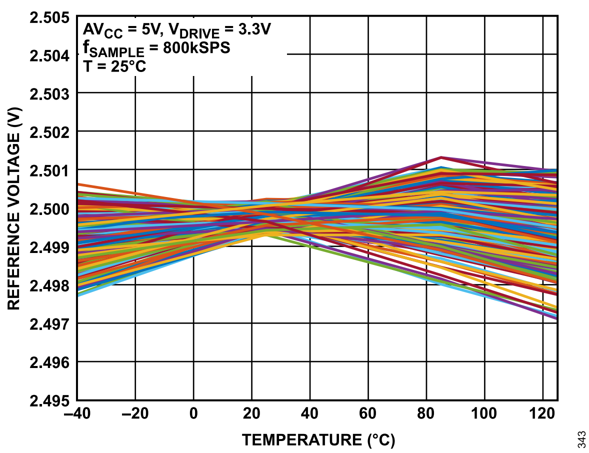


Figure 22. Reference Drift

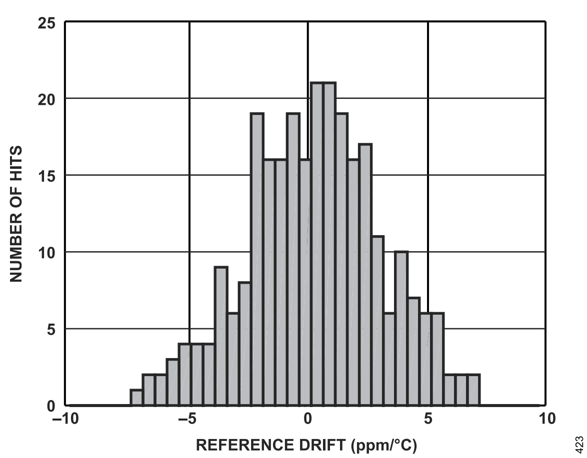


Figure 23. Reference Drift Histogram

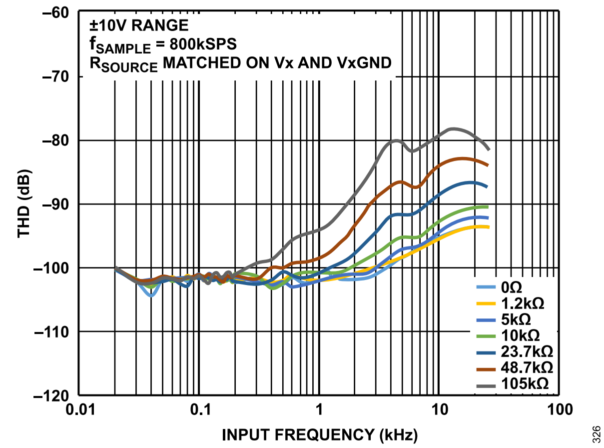


Figure 24. THD vs. Input Frequency for Various Source Impedances (R_{SOURCE}), ±10 V Range

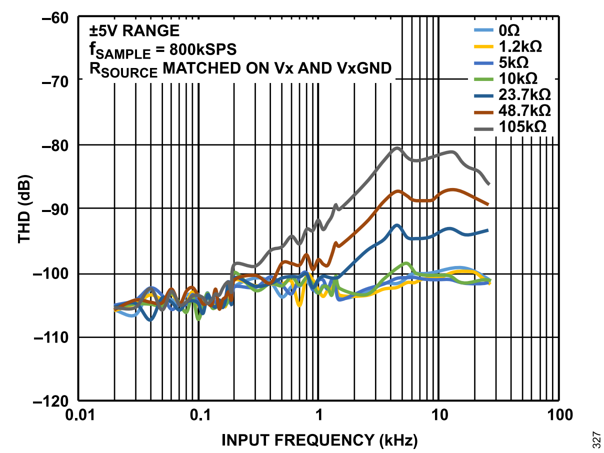


Figure 25. THD vs. Input Frequency for Various Source Impedances, ±5 V Range

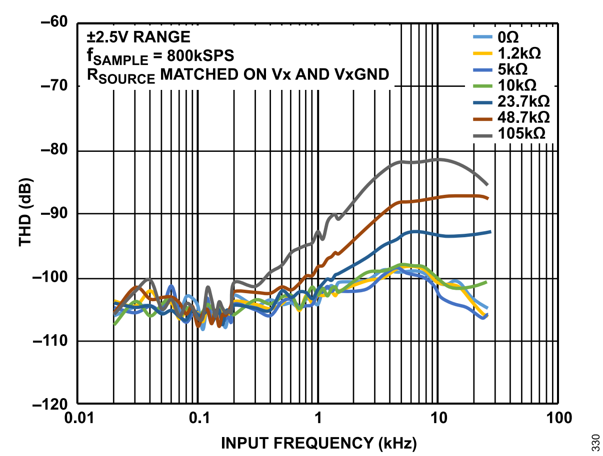


Figure 26. THD vs. Input Frequency for Various Source Impedances, ±2.5 V Range

TYPICAL PERFORMANCE CHARACTERISTICS

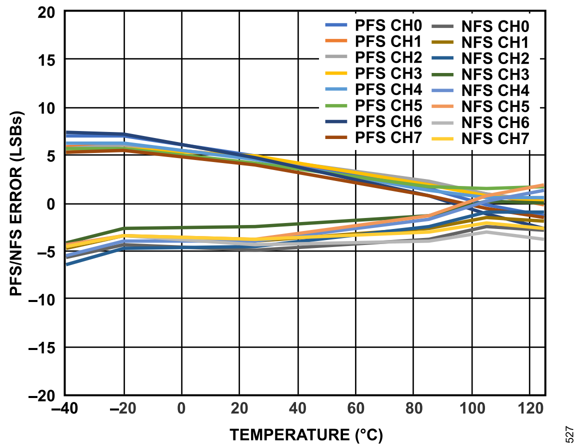


Figure 27. Positive Full-Scale and Negative Full-Scale (PFS/NFS) Error vs. Temperature, ±10 V Range

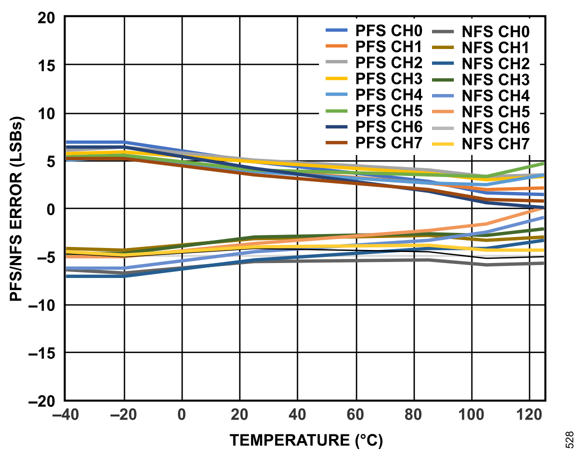


Figure 28. PFS/NFS Error vs. Temperature, ±5 V Range

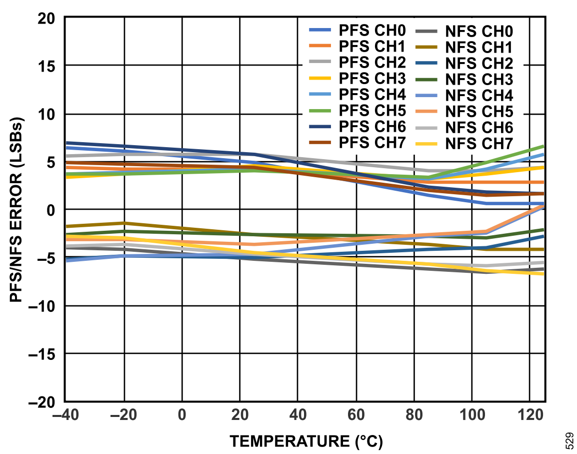


Figure 29. PFS/NFS Error vs. Temperature, ±2.5 V Range

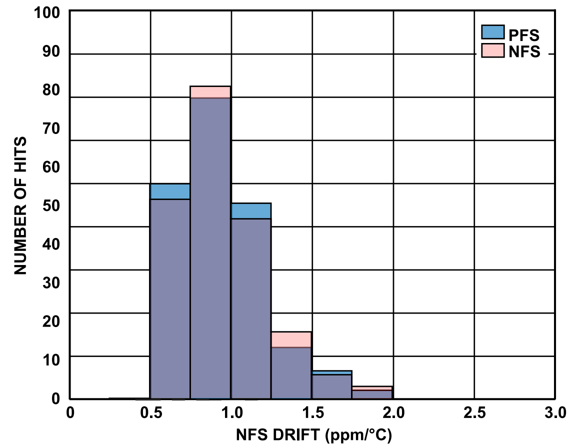


Figure 30. PFS/NFS Drift Histogram, External Reference

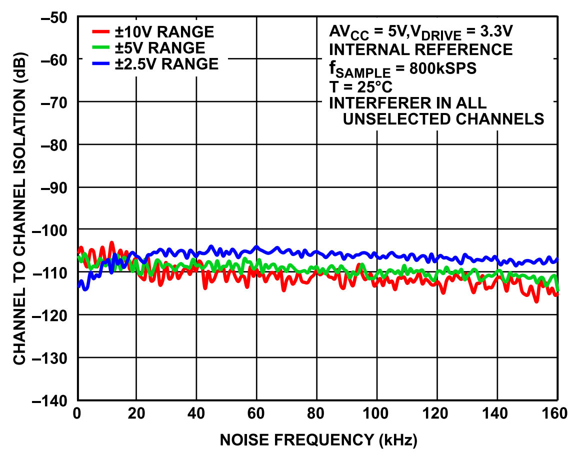


Figure 31. Channel-to-Channel Isolation vs. Noise Frequency

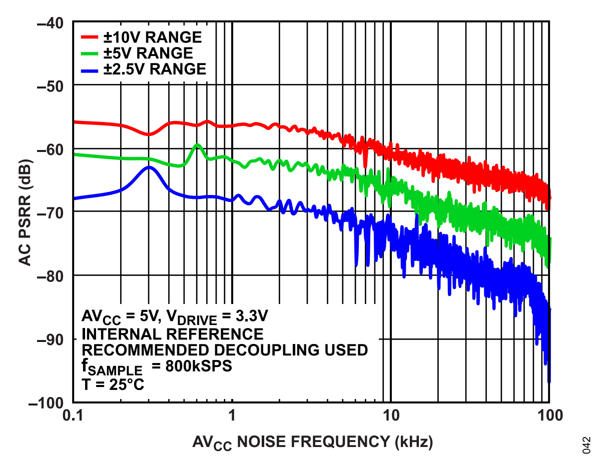


Figure 32. AC Power Supply Rejection Ratio (PSRR)

TYPICAL PERFORMANCE CHARACTERISTICS

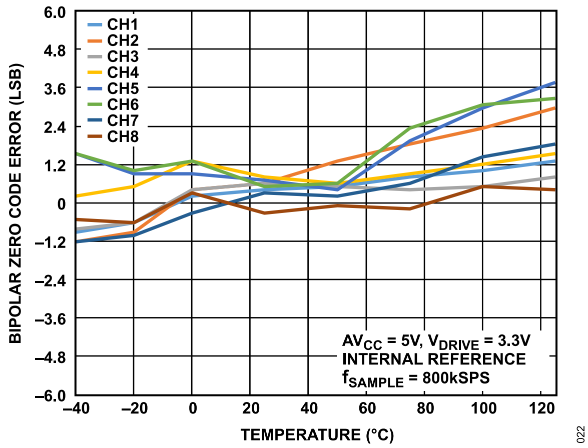


Figure 33. Bipolar Zero Code Error vs. Temperature, ±10 V Range

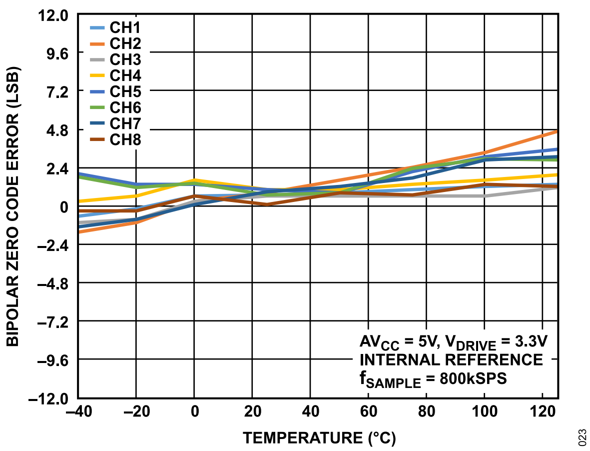


Figure 34. Bipolar Zero Code Error vs. Temperature, ±5 V Range

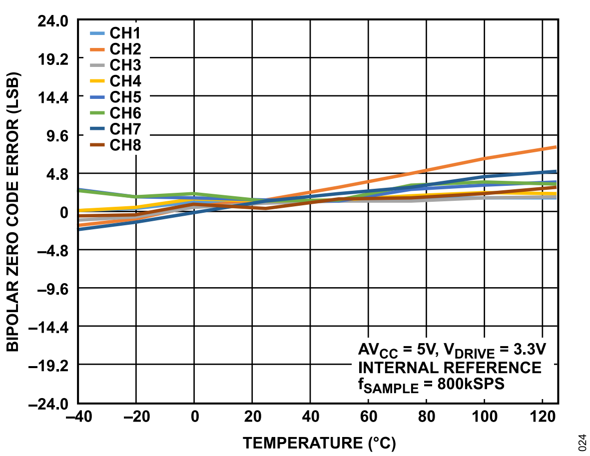


Figure 35. Bipolar Zero Code Error vs. Temperature, ±2.5 V Range

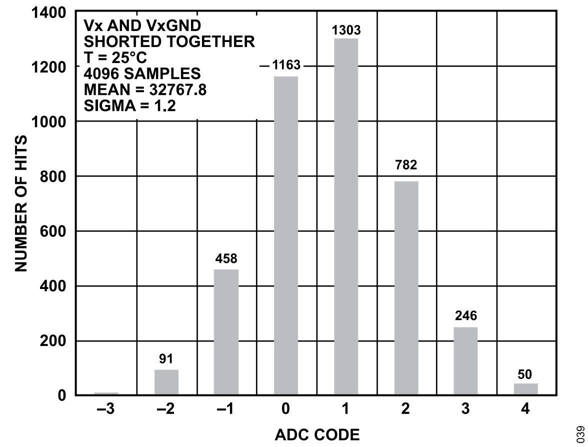


Figure 36. Histogram of Codes, ±10 V Range

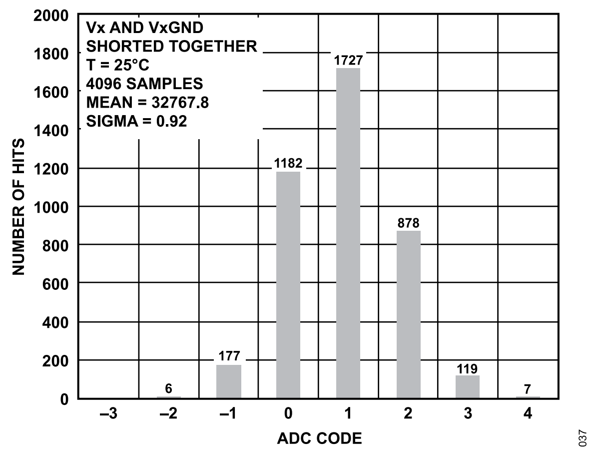


Figure 37. Histogram of Codes, ±5 V Range

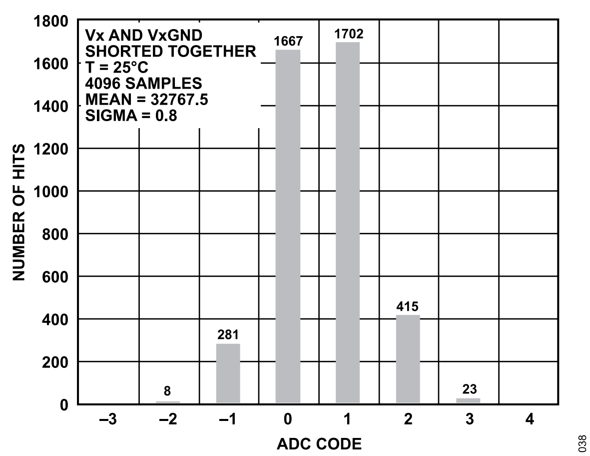


Figure 38. Histogram of Codes, ±2.5 V Range

TYPICAL PERFORMANCE CHARACTERISTICS

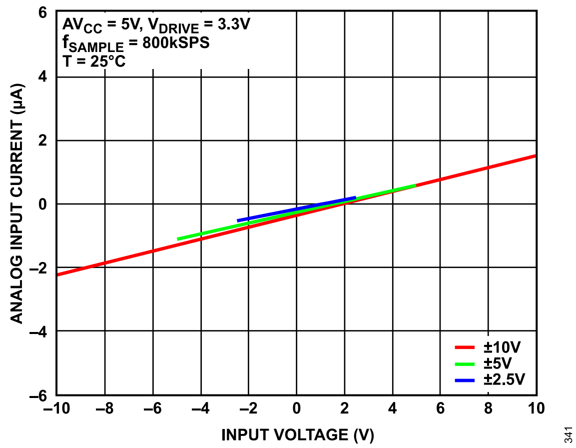


Figure 39. Analog Input Current vs. Input Voltage

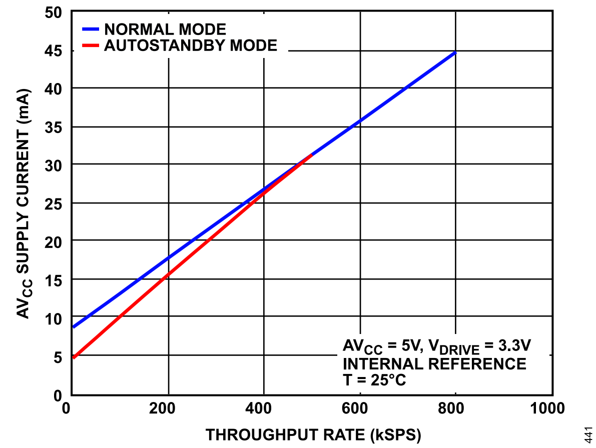


Figure 41. AV_{CC} Supply Current vs. Throughput Rate

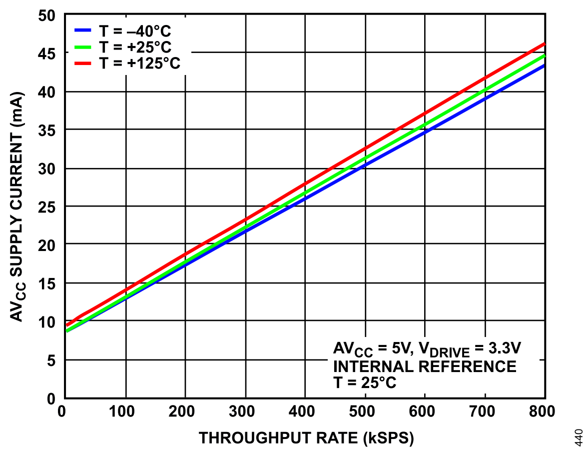


Figure 40. AV_{CC} Supply Current vs. Throughput Rate

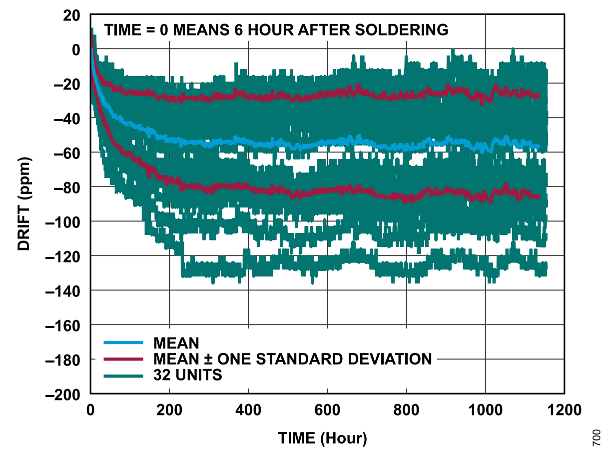


Figure 42. Long Term Drift

TERMINOLOGY

Integral Nonlinearity (INL)

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale at ½ LSB below the first code transition and full scale at ½ LSB above the last code transition.

Differential Nonlinearity (DNL)

DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error

Bipolar zero code error is the deviation of the midscale transition (all 1s to all 0s) from the ideal, which is 0 V − ½ LSB.

Bipolar Zero Code Error Matching

Bipolar zero code error match is the absolute difference in bipolar zero code error between any two input channels.

Open Circuit Code Error

Open circuit code error is the ADC output code when there is an open circuit on the analog input, and a pull-down resistor (R_{PD}) connected between the analog input pair of pins. See Figure 61 for more details.

Positive Full-Scale (PFS) Error

PFS error is the deviation of the actual last code transition from the ideal last code transition (for example, 10 V − 1½ LSB (9.99954), 5 V − 1½ LSB (4.99977), or 2.5 V − 1½ LSB (2.49988)) after the bipolar zero code error is adjusted out. The PFS error includes the contribution from the internal reference and reference buffer.

Positive Full-Scale (PFS) Error Matching

PFS error matching is the absolute difference in PFS error between any two input channels.

Negative Full-Scale (NFS) Error

NFS error is the deviation of the first code transition from the ideal first code transition (for example, −10 V + ½ LSB (−9.99984), −5 V + ½ LSB (−4.99992), or −2.5 V + ½ LSB (−2.49996)) after the bipolar zero code error is adjusted out. The NFS error includes the contribution from the internal reference and reference buffer.

Negative Full-Scale (NFS) Error Matching

NFS error matching is the absolute difference in NFS error between any two input channels.

Total Unadjusted Error (TUE)

TUE is the maximum deviation of the output code from the ideal. TUE includes INL errors, bipolar zero code and positive and negative full-scale errors, and reference errors.

Signal-to-Noise and Distortion Ratio (SINAD)

SINAD ratio is the measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the RMS amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$, excluding DC).

The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise.

The theoretical SINAD for an ideal N-bit converter with a sine wave input is given by

$$SINAD = (6.02\,N + 1.76)\ \text{(dB)} \quad (1)$$

Thus, for a 16-bit converter, the SINAD is 98 dB.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the harmonics to the fundamental. For the AD7606B, THD is defined as

$$THD(dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2}}{V_1} \quad (2)$$

where:
V_1 is the rms amplitude of the fundamental.
V_2 to V_9 are the rms amplitudes of the second through ninth harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS signal amplitude of the input signal to the RMS value of the peak spurious spectral component.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. The power supply rejection (PSR) is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSRR is defined as the ratio of the 100 mV p-p sine wave applied to the AV_{CC} supplies of the ADC frequency, f_S, to the power of the ADC output at that frequency, f_S.

$$PSRR\ \text{(dB)} = 20\log(0.1/Pf_S) \quad (3)$$

where:
Pf_S is equal to the power at frequency, f_S, coupled on the AV_{CC} supply.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between all input channels. It is measured by applying a full-scale sine wave signal, up to 160 kHz, to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied (see Figure 31).

TERMINOLOGY

Phase Delay

Phase delay is a measure of the absolute time delay between when an input is sampled by the converter and when the result associated with that sample is available to be read back from the ADC, including delay induced by the analog front end of the device.

Phase Delay Drift

Phase delay drift is the change in phase delay per unit temperature across the entire operating temperature of the device.

Phase Delay Matching

Phase delay matching is the maximum phase delay seen between any simultaneously sampled pair.

Box Method

The box method is represented by the following equation:

$$TCV_{OUT} = \left| \frac{max\{V_{OUT}(T_1, T_2, T_3)\} - min\{V_{OUT}(T_1, T_2, T_3)\}}{V_{OUT}(T_2) \times (T_3 - T_1)} \right| \times 10^6 \quad (4)$$

where:
TCV_{OUT} is expressed in ppm/°C.
$V_{OUT}(T_X)$ is the output voltage at temperature T_X.
T_1 = −40°C.
T_2 = +25°C.
T_3 = +125°C.

This box method ensures that TCV_{OUT} accurately portrays the maximum difference between any of the three temperatures at which the output voltage of the device is measured.

THEORY OF OPERATION

ANALOG FRONT END

The AD7606B is a 16-bit, simultaneous sampling, analog-to-digital DAS with eight channels. Each channel contains analog input clamp protection, a PGA, a low-pass filter, and a 16-bit SAR ADC.

Analog Input Ranges

The AD7606B can handle true bipolar, single-ended input voltages.

In software mode, it is possible to configure an individual analog input range per channel using Address 0x03 through Address 0x06. The logic level on the RANGE pin is ignored in software mode.

In hardware mode, the logic level on the RANGE pin determines either ±10 V or ±5 V single-ended as the analog input range of all analog input channels, as shown in Table 10.

A logic change on the RANGE pin has an immediate effect on the analog input range. However, there is typically a settling time of approximately 80 µs in addition to the normal acquisition time requirement. Changing the RANGE pin during a conversion is not recommended for fast throughput rate applications.

Table 10. Analog Input Range Selection

Range (V)	Hardware Mode[1]	Software Mode[2]
±10 Single-Ended	RANGE pin high	Address 0x03 through Address 0x06
±5 Single-Ended	RANGE pin low	Address 0x03 through Address 0x06
±2.5	Not applicable	Address 0x03 through Address 0x06

1 The same analog input range, ±10 V or ±5 V, applies to all eight channels.

2 The analog input range is selected on a per channel basis using the memory map.

Analog Input Impedance

The analog input impedance (R_{IN}) of the AD7606B is typically 5 MΩ. R_{IN} is a fixed input impedance that does not vary with the AD7606B sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7606B, allowing direct connection to the source or sensor. Therefore, bipolar supplies can be removed from the signal chain.

Analog Input Clamp Protection

Figure 43 shows the analog input circuitry of the AD7606B. Each analog input of the AD7606B contains clamp protection circuitry. Despite single, 5 V supply operation, this analog input clamp protection allows an input overvoltage of up to ±21 V.

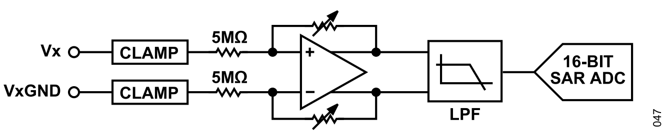


Figure 43. Analog Input Circuitry for Each Channel

Figure 44 shows the input clamp current vs. the source voltage characteristic of the clamp circuit. For input voltages of up to ±21 V, no current flows in the clamp circuit. For input voltages that are above ±21 V, the AD7606B clamp circuitry turns on.

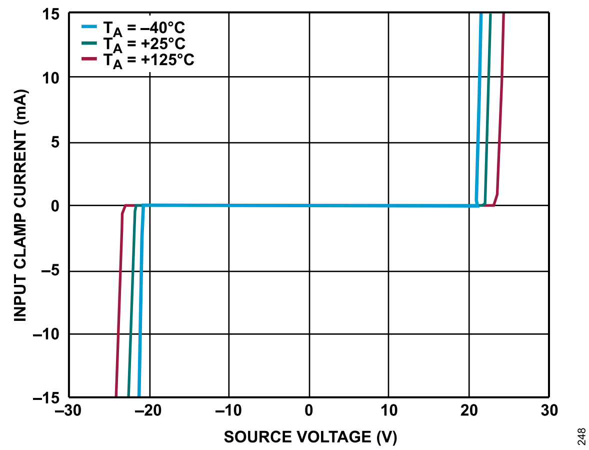


Figure 44. Input Protection Clamp Profile

It is recommended to place a series resistor on the analog input channels to limit the current to ±10 mA for input voltages greater than ±21 V. In an application where there is a series resistance (R) on an analog input channel, Vx+, it is recommended to match the resistance (R) with the resistance on VxGND to eliminate any offset introduced to the system, as shown in Figure 45. However, in software mode, a per channel system offset calibration removes the offset of the full system (see the System Offset Calibration section).

During normal operation, it is not recommended to leave the AD7606B in a condition where the analog input is greater than the input range for extended periods of time because this condition can degrade the bipolar zero code error performance. In shutdown or standby mode, there is no such concern.

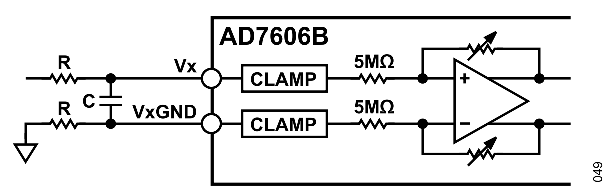


Figure 45. Input Resistance Matching on the Analog Input of the AD7606B

PGA

A PGA is provided at each input channel. The gain is configured depending on the analog input range selected (see Table 10) to scale the single-ended analog input signal to the ADC fully differential input range.

Input impedance on each input of the PGA is accurately trimmed to maintain the overall gain error. This trimmed value is then used when the gain calibration is enabled to compensate for the gain error introduced by an external series resistor. See the System Gain Calibration section for more information on the PGA feature.

THEORY OF OPERATION

Analog Input Antialiasing Filter

An analog antialiasing filter is provided on the AD7606B. Figure 46 and Figure 47 show the frequency response and phase response, respectively, of the analog antialiasing filter. In the ±10 V range, the −3 dB frequency is typically 22.5 kHz.

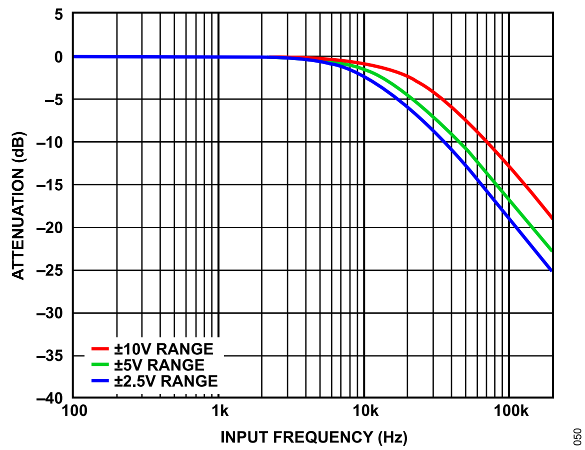


Figure 46. Analog Antialiasing Filter Frequency Response

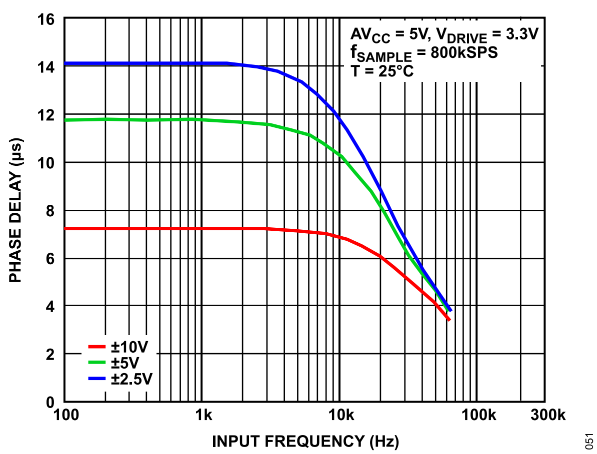


Figure 47. Analog Antialiasing Filter Phase Response

SAR ADC

The AD7606B allows the ADC to accurately acquire an input signal of full-scale amplitude to 16-bit resolution. All eight SAR ADCs sample the respective inputs simultaneously on the rising edge of the CONVST signal.

The BUSY signal indicates when conversions are in progress. Therefore, when the rising edge of the CONVST signal is applied, the BUSY pin goes logic high and transitions low at the end of the entire conversion process. The end of the conversion process across all eight channels is indicated by the falling edge of the BUSY signal. When the BUSY signal edge falls, the acquisition time for the next set of conversions begins. The rising edge of the CONVST signal has no effect while the BUSY signal is high.

New data can be read from the output register through the parallel or serial interface after the BUSY output goes low. Alternatively, data from the previous conversion can be read while the BUSY pin is high, as explained in the Reading During Conversion section.

The AD7606B contains an on-chip oscillator that performs the conversions. The conversion time for all ADC channels is t_{CONV} (see Table 3). In software mode, there is an option to apply an external clock through the CONVST pin. Providing a low jitter external clock improves SNR performance for large OSRs. See the Digital Filter section and Figure 15 to Figure 20 for further information.

Connect all unused analog input channels to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

ADC Transfer Function

The output coding of the AD7606B is twos complement.

The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is FSR/65,536 for the AD7606B. The ideal transfer characteristics for the AD7606B are shown in Figure 48. The LSB size is dependent on the analog input range selected, as shown in Table 11.

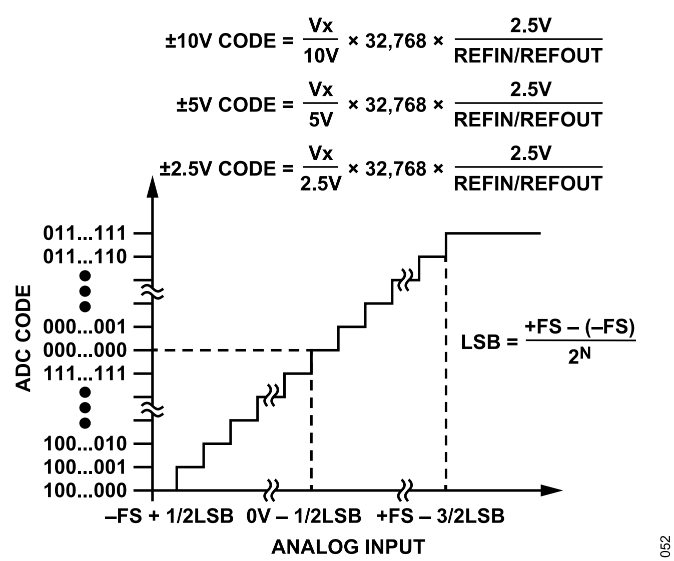


Figure 48. AD7606B Ideal Transfer Characteristics

Table 11. Input Voltage Ranges

Range (V)	PFS (V)	Midscale (V)	NFS (V)	LSB (μV)
±10	10	0	−10	305.2
±5	5	0	−5	152.6
±2.5	2.5	0	−2.5	76.3

THEORY OF OPERATION

REFERENCE

The AD7606B contains an on-chip, 2.5 V, band gap reference. The REFIN/REFOUT pin allows the following:

- Access to the internal 2.5 V reference if the REF SELECT pin is tied to logic high
- Application of an external reference of 2.5 V, like the ADR4525 or LT6657, if the REF SELECT pin is tied to logic low.

Table 12. Reference Configuration

REF SELECT Pin	Reference Selected
Logic High	Internal reference enabled
Logic Low	Internal reference disabled; an external 2.5 V reference voltage must be applied to the REFIN/REFOUT pin

The AD7606B contains a reference buffer configured to amplify the reference voltage up to approximately 4.4 V, as shown in Figure 49. The 4.4 V buffered reference is the reference used by the SAR ADC, as shown in Figure 49. After a reset, the AD7606B operates in the reference mode selected by the REF SELECT pin. The REFCAPA and REFCAPB pins must be shorted together externally, and a ceramic capacitor of 10 µF must be applied to the REFGND pin to ensure that the reference buffer is in closed-loop operation. A 10 µF ceramic capacitor is required on the REFIN/REFOUT pin.

When the AD7606B is configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin.

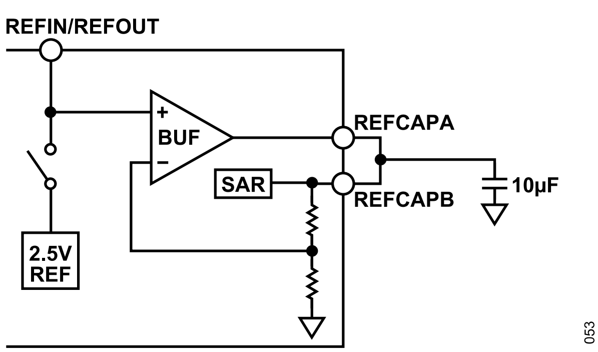


Figure 49. Reference Circuitry

Using Multiple AD7606B Devices

For applications using multiple AD7606B devices, the following configurations are recommended, depending on the application requirements.

External Reference Mode

One external reference can drive the REFIN/REFOUT pins of all AD7606B devices (see Figure 50). In this configuration, decouple each REFIN/REFOUT pin of the AD7606B with at least a 100 nF decoupling capacitor.

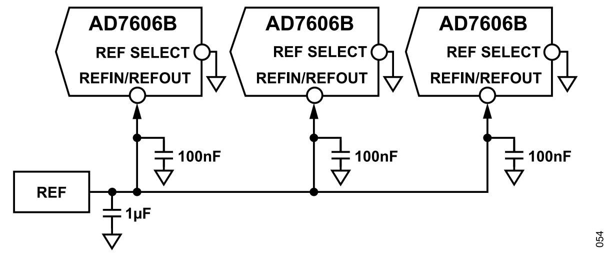


Figure 50. Single External Reference Driving Multiple AD7606B REFIN/ REFOUT Pins

Internal Reference Mode

One AD7606B device, configured to operate in internal reference mode, can drive the remaining AD7606B devices, which are configured to operate in external reference mode (see Figure 51). Decouple the REFIN/REFOUT pin of the AD7606B, configured in internal reference mode, using a 10 µF ceramic decoupling capacitor. The other AD7606B devices, configured in external reference mode, must use at least a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

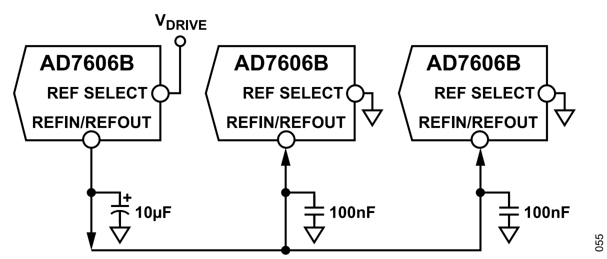


Figure 51. Internal Reference Driving Multiple AD7606B REFIN/REFOUT Pins

OPERATION MODES

The AD7606B can be operated in hardware or software mode by controlling the OSx pins (Pin 3, Pin 4, and Pin 5), described in Table 13.

In hardware mode, the AD7606B is configured depending on the logic level on the RANGE, OSx, or $\overline{\text{STBY}}$ pins.

In software mode, that is, when all three OSx pins are connected to logic high level, the AD7606B is configured by the corresponding registers accessed through the serial or parallel interface. Additional features are available, as described in Table 14.

The reference and the data interface is selected using the REF SELECT and $\overline{\text{PAR}}$/SER SEL pins, in both hardware and software modes.

THEORY OF OPERATION

Table 13. Oversampling Pin Decoding

OS2	OS1	OS0	Oversampling Ratio
0	0	0	No oversampling
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	Enters software mode

Table 14. Functionality Matrix

Parameter	Hardware Mode	Software Mode
Analog Input Range[1]	±10 V or ±5 V[2]	±10 V, ±5 V, or ±2.5 V[3]
System Gain, Phase, and Offset Calibration	Not accessible	Available[3]
OSR	From no OS to OSR = 64	From no OS to OSR = 256
Analog Input Open Circuit Detection	Not accessible	Available[3]
Serial Data Output Lines	2	Selectable: 1, 2, or 4
Diagnostics	Not accessible	Available
Power-Down Modes	Standby and shutdown	Standby, shutdown, and autostandby

1 See Table 10 for the analog input range selection.
2 Same input range configured in all input channels.
3 On a per channel basis.

Reset Functionality

The AD7606B has two reset modes: partial or full. The reset mode selected is dependent on the length of the reset high pulse. A partial reset requires the RESET pin to be held high between 55 ns and 2 µs. After 50 ns from the release of the RESET pin (t_{DEVICE_SETUP}, partial reset), the device is fully functional and a conversion can be initiated. A full reset requires the RESET pin to be held high for a minimum of 3 µs. After 253 µs (t_{DEVICE_SETUP}, full reset) from the release of the RESET pin, the device is completely reconfigured and a conversion can be initiated.

A partial reset reinitializes the following modules:

- Digital filter
- Serial peripheral interface (SPI) and parallel, resetting to ADC read mode
- SAR ADCs
- CRC logic

After the partial reset, the RESET_DETECT bit of the status register asserts (Address 0x01, Bit 7). The current conversion result is discarded after the completion of a partial reset. The partial reset does not affect the register values programmed in software mode or the latches that store the user configuration in both hardware and software modes.

A full reset returns the device to the default power-on state, the RESET_DETECT bit of the status register asserts (Address 0x01, Bit 7), and the current conversion result is discarded. The following features, in addition to the features that reinitialize with a partial reset and listed previously, are configured when the AD7606B is released from full reset:

- Hardware mode or software mode
- Interface type (serial or parallel)

Power-Down Modes

In hardware mode, two power-down modes are available on the AD7606B: standby mode and shutdown mode. The $\overline{\text{STBY}}$ pin controls whether the AD7606B is in normal mode or in one of the two power-down modes, as shown in Table 15. If the $\overline{\text{STBY}}$ pin is low, the power-down mode is selected by the state of the RANGE pin.

Table 15. Power-Down Mode Selection, Hardware Mode

Power Mode	$\overline{\text{STBY}}$ Pin	RANGE Pin
Normal Mode	1	X[1]
Standby	0	1
Shutdown	0	0

1 X means do not care.

In software mode, the power-down mode is selected through the OPERATION_MODE bits on the CONFIG register (Address 0x02, Bits[1:0]) within the memory map. There is an extra power-down mode available in software mode called autostandby mode.

THEORY OF OPERATION

Table 16. Power-Down Mode Selection, Software Mode, Through CONFIG Register (Address 0x02)

Operation Mode	Address 0x02, Bit 1	Address 0x02, Bit 0
Normal	0	0
Standby	0	1
Autostandby	1	0
Shutdown	1	1

When the AD7606B is placed in shutdown mode, all circuitry is powered down and the current consumption reduces to 5 μA, maximum. A reset pulse is needed to exit shutdown mode. The power-up time is approximately 10 ms. When the AD7606B is powered up from shutdown mode, a full reset must be applied to the AD7606B after the required power-up time elapses.

When the AD7606B is placed in standby mode, all the PGAs and all the SAR ADCs enter a low power mode, such that the overall current consumption reduces to 4.5 mA, maximum. No reset is required after exiting standby mode.

When the AD7606B is placed in autostandby mode, available only in software mode, the device automatically enters standby mode on the BUSY signal falling edge. The AD7606B exits standby mode automatically on the CONVST signal falling edge. Therefore, the CONVST signal low pulse time is longer than t_{WAKE_UP} (standby mode) = 1 μs (see Figure 52).

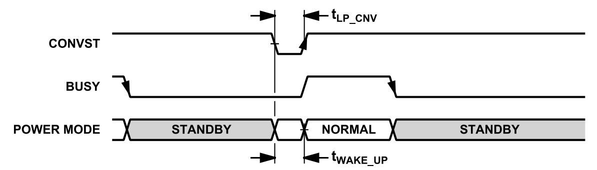


Figure 52. Autostandby Mode Operation

DIGITAL FILTER

The AD7606B contains an optional digital averaging filter that can be enabled in slower throughput rate applications that require higher SNR or dynamic range.

In hardware mode, the oversampling ratio of the digital filter is controlled using the oversampling pins, OSx, as shown in Table 13. The OSx pins are latched on the falling edge of the BUSY signal.

In software mode, that is, if all OSx pins are tied to logic high, the oversampling ratio is selected through the oversampling register (Address 0x08). Two additional oversampling ratios (OS × 128 and OS × 256) are available in software mode.

In oversampling mode, the ADC takes the first sample for each channel on the rising edge of the CONVST signal. After converting the first sample, the subsequent samples are taken by the internally generated sampling signal, as shown in Figure 53. Alternatively, this sampling signal can be applied externally as described in the External Oversampling Clock section. For example, if oversampling by eight is configured, eight samples are taken, averaged, and the result is provided on the output. A CONVST signal rising edge triggers the first sample, and the remaining seven samples are taken with an internally generated sampling signal. Consequently, turning on the averaging of multiple samples leads to an improvement in SNR performance, at the expense of reducing the maximum throughput rate. When the oversampling function is turned on, the BUSY signal high time (t_{CONV}) extends, as shown in Table 3.

Table 17 shows the trade-off in SNR vs. bandwidth and throughput for the ±10 V, ±5 V, and ±2.5 V ranges.

Figure 53 shows that the conversion time (t_{CONV}) extends when oversampling is turned on. The throughput rate ($1/t_{CYCLE}$) must be reduced to accommodate the longer conversion time and to allow the read operation to occur. To achieve the fastest throughput rate possible when oversampling is turned on, the read can be performed during the BUSY signal high time as explained in the Reading During Conversion section.

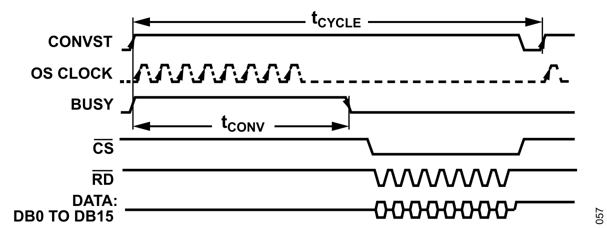


Figure 53. AD7606B Oversampling by 8 Example, Read After Conversion, Parallel Interface, OS Clock Internally Generated Sampling Signal

Table 17. Oversampling Performance

Oversampling Ratio	Input Frequency (Hz)	±10 V Range		±5 V Range		±2.5 V Range		Maximum Throughput (kSPS)
		SNR (dB)	−3 dB BW (kHz)	SNR (dB)	−3 dB BW (kHz)	SNR (dB)	−3 dB BW (kHz)	
No OS	1000	89.5	23.0	88.5	13.9	86	11.6	800
2	1000	91	22.7	89.9	13.8	87.2	11.5	400
4	1000	92.2	22.0	90.8	13.6	88	11.4	200
8	1000	93	20.0	91.5	13.0	88.4	11.1	100
16	1000	93.5	15.4	92	11.4	89	10.0	50
32	130	95.4	9.7	93.7	8.4	90.4	7.7	25
64	130	96.3	5.3	95	5.0	91.8	4.9	12.5
128[1]	50	97.1	2.7	95.9	2.7	93.3	2.7	6.25
256[1]	50	97.6	1.4	96.8	1.4	94.7	1.4	3.125

[1] Only available in software mode.

DIGITAL FILTER

PADDING OVERSAMPLING

As shown in Figure 53, an internally generated clock triggers the samples to be averaged, and then the ADC remains idle until the following CONVST signal rising edge. In software mode, through the oversampling register (Address 0x08), the internal clock (OS clock) frequency can be changed such that idle time is minimized, that is, sampling instants are equally spaced, as shown in Figure 54.

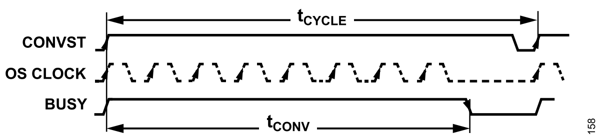


Figure 54. Oversampling by 8 Example, Oversampling Padding Enabled

Table 18. OS_PAD Bit Decoding

OS_PAD (Address 0x08, Bits[7:4])	OS Clock Frequency (kHz)
0000	800
0001	753
0010	711
0011	673.5
0100	640
0101	609.5
0110	582
0111	556.5
1000	533
1001	512
1010	492.5
1011	474
1100	457
1101	441.5
1110	426.5
1111	413

EXTERNAL OVERSAMPLING CLOCK

In software mode, there is an option to apply an external clock through the CONVST pin when oversampling mode is enabled. Providing a low jitter external clock improves SNR performance for large oversampling ratios. By applying an external clock, the input is sampled at regular time intervals, which is optimum for antialiasing performance.

To enable the external oversampling clock, Bit 5 in the CONFIG register (Address 0x02, Bit 5) must be set. Then, the throughput rate is the following:

$$Throughput = \frac{1}{t_{CNVST} \times OSR} \quad (5)$$

That is, the sampling signal is provided externally through the CONVST pin, and every OSR number of clocks, an output is averaged and provided, as shown in Figure 56. This feature is available using either the parallel interface or the serial interface.

Simultaneous Sampling of Multiple AD7606B Devices

In general, synchronizing several SAR ADCs can easily be achieved by using a common CNVST signal. However, when OS is enabled, an internal clock is used by default to trigger the subsequent samples. Any deviation between these internal clocks may impede device-to-device synchronization. This deviation can be minimized by using external OS because the CNVST signal of all the samples are managed externally.

A partial reset (t_{RESET} < 2 μs) interrupts the oversampling process and empties the data register. Therefore, if by any reason one of the AD7606B devices is not in synchrony, issuing a partial reset easily resynchronizes them all, as shown in Figure 55.

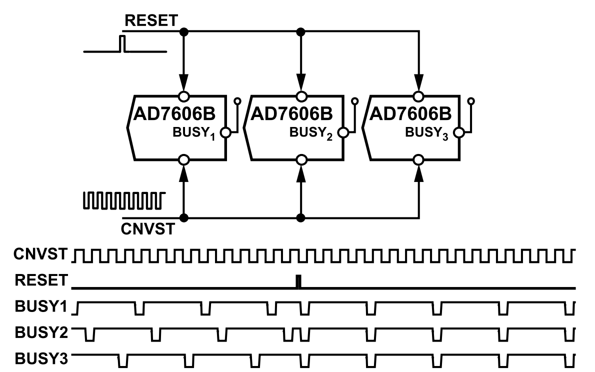


Figure 55. Synchronizing Multiple AD7606B Devices with External OS Clock Enabled

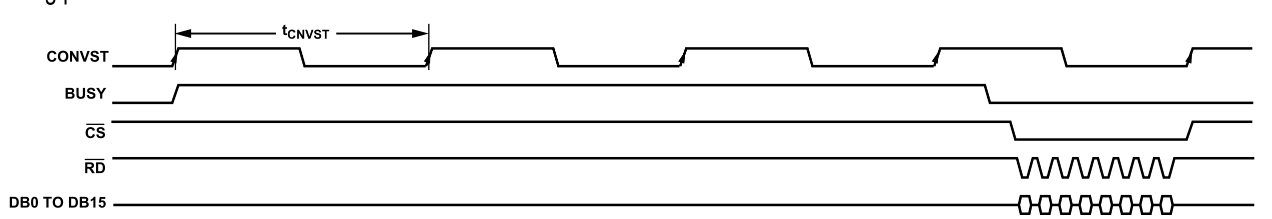


Figure 56. External OS Clock Applied on the CONVST Pin (OSR = 4), Parallel Interface

SYSTEM CALIBRATION FEATURES

The following system calibration features are available in software mode by writing to corresponding registers in the memory map:

- Phase calibration
- Gain calibration
- Offset calibration
- Analog input open circuit detection

SYSTEM PHASE CALIBRATION

When using an external filter, as shown in Figure 58, any mismatch on the discrete components, or in the sensor being used, can cause phase mismatch between channels. This phase mismatch can be compensated for in software mode, on a per channel basis, by delaying the sampling instant on individual channels.

The sampling instant on any particular channel can be delayed with regard to the CONVST signal rising edge, with a resolution of 1.25 µs, and up to 318.75 µs, by writing to the corresponding CHx_PHASE register (Address 0x19 through Address 0x20).

For example, if the CH4_PHASE register (Address 0x1C) is written with 10 (decimal), Channel 4 is effectively sampled 12.5 µs (t_{PHASE_REG}) after the CONVST signal rising edge, as shown in Figure 57.

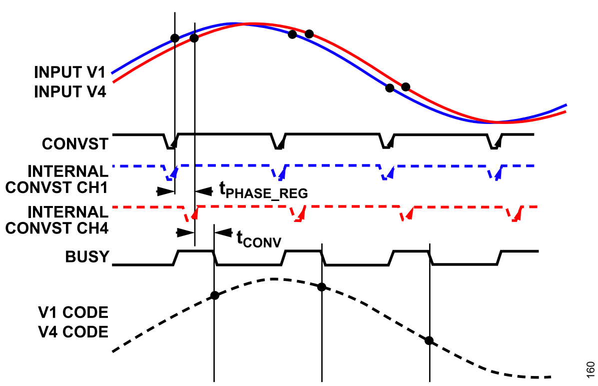


Figure 57. System Phase Calibration Functionality

The BUSY signal high time equals t_{CONV} plus t_{PHASE_REG}, as shown in Figure 57.

In the previously explained example and Figure 57, if only the CH4_PHASE register is programmed, t_{CONV} increases by 12.5 µs. Therefore, this scenario must be considered when running at higher throughput rates.

SYSTEM GAIN CALIBRATION

Using an external R_{FILTER}, as shown in Figure 58, generates a system gain error. This gain error can be compensated for in software mode, on a per channel basis, by writing the series resistor value used on the corresponding register, Address 0x09 through Address 0x10. These registers can compensate up to 65 kΩ series resistors, with a resolution of 1024 Ω.

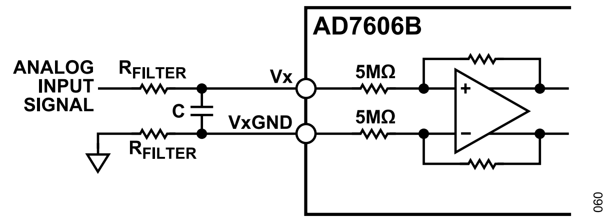


Figure 58. System Gain Error

For example, if a 27 kΩ resistor is placed in series to the analog input of Channel 5, the resistor generates a −170 LSB positive full-scale error on the system (at ±10 V range), as shown in Figure 59. In software mode, this error is eliminated by writing 27 (decimal) to the CH5_GAIN register (Address 0x0D), which keeps the error within 0.01% of FSR, no matter the R_{FILTER} value of the series resistor, as shown in Figure 60.

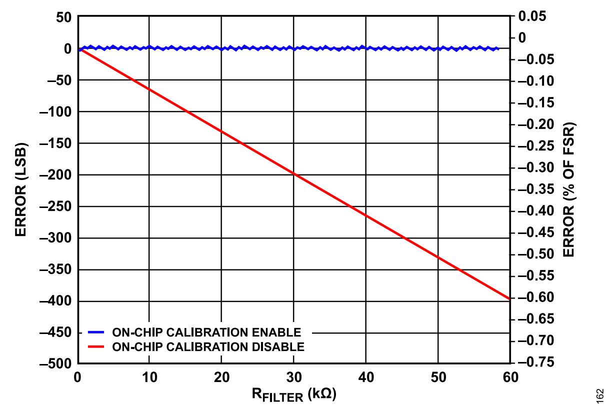


Figure 59. System Gain Calibration with and Without Calibration

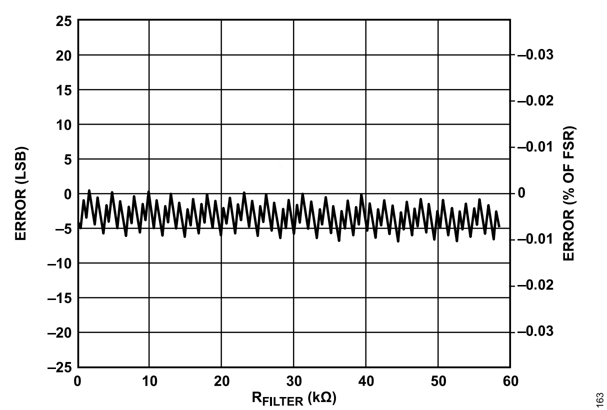


Figure 60. System Error with Gain Calibration Enabled

SYSTEM CALIBRATION FEATURES

SYSTEM OFFSET CALIBRATION

A potential offset on the sensor, or any offset caused by a mismatch between the R_{FILTER} pair placed on a particular channel (as described in the Analog Front End section), can be compensated in software mode, on a per channel basis. The CHx_OFFSET registers (Address 0x11 through Address 0x18) allow the ability to add or subtract up to 128 LSBs from the ADC code automatically, with a resolution of 1 LSB, as shown in Table 19.

For example, if the signal connected to Channel 3 has a 9 mV offset, and the analog input range is set to the ±10 V range (where LSB size = 305 μV) to compensate for this offset, program −30 LSB to the corresponding register. Writing 128 (decimal) − 30 (decimal) = 0x80 − 0x1E = 0x62 to the CH3_OFFSET register (Address 0x13) removes such offset.

Table 19. CHx_OFFSET Register Bit Decoding

CHx_OFFSET Register	Offset Calibration (LSB)
0x00	−128
0x45	−59
0x80 (Default)	0
0x83	3
0xFF	127

ANALOG INPUT OPEN CIRCUIT DETECTION

The AD7606B has an analog input open circuit detection feature available in software mode. To use this feature, R_{PD} must be placed as shown in Figure 61. If the analog input is disconnected, for example, if a switch opens in Figure 61, the source impedance changes from the burden resistor (R_{BURDEN}) to R_{PD}, as long as $R_{BURDEN} < R_{PD}$. It is recommended to use R_{PD} = 50 kΩ so that the AD7606B can detect changes in the source impedance by internally switching the PGA common-mode voltage. Analog input open circuit detection operates in manual mode or in automatic mode.

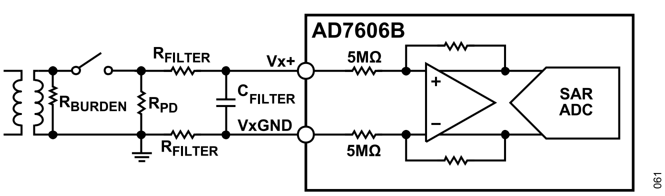


Figure 61. Analog Front End with R_{PD}

Manual Mode

In manual mode, enabled by writing 0x01 to OPEN_DETECT_QUEUE (Address 0x2C), each PGA common-mode voltage is controlled by the corresponding CHx_OPEN_DETECT_EN bit on the OPEN_DETECT_ENABLE register (Address 0x23). Setting this bit high shifts up the PGA common-mode voltage. If there is an open circuit on the analog input, the ADC output changes proportionally to the R_{PD} resistor, as shown in Figure 62. If there is no open circuit, any change on the PGA common-mode voltage has no effect on the ADC output.

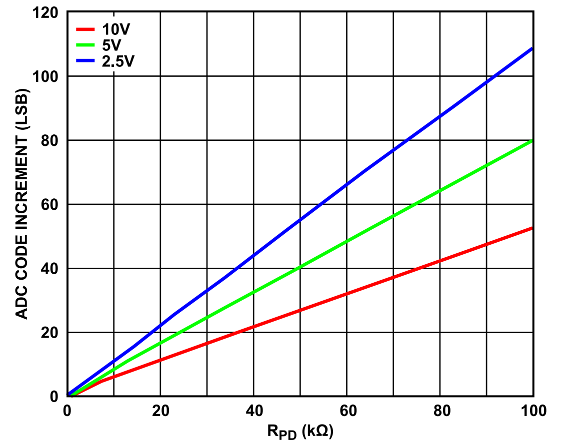


Figure 62. Open Circuit Code Error Increment, Dependent of R_{PD}

Automatic Mode

Automatic mode is enabled by writing any value greater than 0x01 to the OPEN_DETECT_QUEUE register (Address 0x2C), as shown in Table 20. If the AD7606B detects that the ADC reported a number (specified in the OPEN_DETECT_QUEUE register) of consecutive unchanged conversions, the analog input open circuit detection algorithm is performed internally and automatically. The analog input open circuit detection algorithm automatically changes the PGA common-mode voltage, checks the ADC output, and returns to the initial common-mode voltage, as shown in Figure 63. If the ADC code changes in any channel with the PGA common-mode change, this implies that there is no input signal connected to that analog input, and the corresponding flag asserts within the OPEN_DETECTED register (Address 0x24). Each channel can be individually enabled or disabled through the OPEN_DETECT_ENABLE register (Address 0x23).

SYSTEM CALIBRATION FEATURES

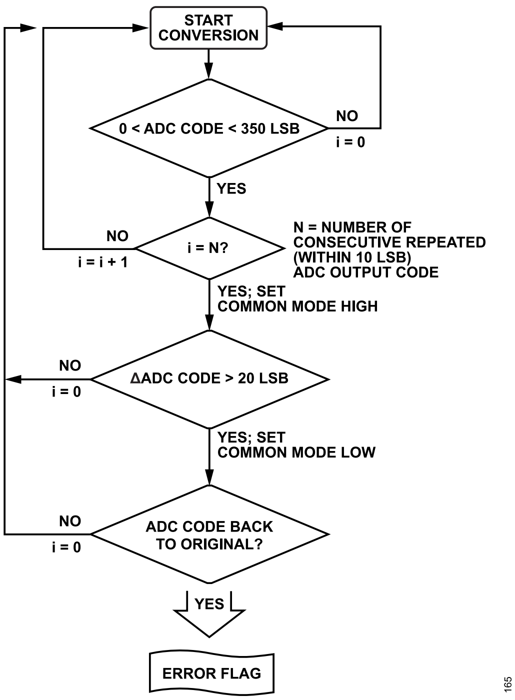


Figure 63. Automatic Analog Input Open Circuit Detect Flowchart

If no oversampling is used, the recommended minimum number of conversions to be programmed for the AD7606B to automatically detect an open circuit on the analog input is

$$OPEN\_DETECT\_QUEUE = 10 \times f_{SAMPLE}(R_{PD} + 2 \times R_{FILTER}) \times (C_{FILTER} + 10\text{pF}) \quad (6)$$

where C_{FILTER} is the capacitor shown in Figure 61.

However, when oversampling mode is enabled, the recommended minimum number of conversions to use is

$$OPEN\_DETECT\_QUEUE = 10 \times f_{SAMPLE} \times 2(R_{PD} + 2 \times R_{FILTER}) \times (C_{FILTER} + 10\text{pF}) \times OSR \quad (7)$$

Table 20. Analog Input Open Circuit Detect Mode Selection and Register Functionality

OPEN_DETECT_QUEUE (Address 0x2C)	Open Detect Mode	OPEN_DETECT_ENABLE (Address 0x23)
0x00 (Default)	Disabled	Not applicable
0x01	Manual mode	Sets common-mode voltage high or low, on a per channel basis
0x02 to 0xFF	Automatic; OPEN_DETECT_QUEUE is the number of consecutive conversions before asserting any CHx_OPEN flag; the minimum value for this register is 5	Enables or disables automatic analog input open circuit detection on a per channel basis

DIGITAL INTERFACE

The AD7606B provides two interface options: a parallel interface and a high speed serial interface. The required interface mode is selected through the $\overline{PAR}$/SER SEL pin.

Table 21. Interface Mode Selection

$\overline{PAR}$/SER SEL	Interface Mode
0	Parallel interface mode
1	Serial interface mode

Operation of the interface modes is discussed in the Hardware Mode section and the Software Mode section.

HARDWARE MODE

In hardware mode, only ADC read mode is available. ADC data can be read from the AD7606B through the parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals or through the serial interface with standard $\overline{CS}$, SCLK, and two $D_{OUT}x$ signals.

See the Reading Conversion Results (Parallel ADC Read Mode) section and the Reading Conversion Results (Serial ADC Read Mode) section for more details on how ADC read mode operates.

SOFTWARE MODE

In software mode, which is active only when all three OS pins are tied high, both ADC read mode and register mode are available. ADC data can be read from the AD7606B, and registers can also be read from and written to the AD7606B through the parallel data bus with standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ signals or through the serial interface with standard $\overline{CS}$, SCLK, SDI, and $D_{OUT}A$ lines.

See the Parallel Register Mode (Reading Register Data) section and the Parallel Register Mode (Writing Register Data) section for more details on how register mode operates.

Pin functions differ depending on the interface selected (parallel or serial) and the operation mode (hardware or software), as shown in Table 22.

Table 22. Data Interface Pin Function per Mode of Operation

		Parallel Interface			Serial Interface		
			Software Mode			Software mode	
Pin Mnemonic	Pin No.	Hardware Mode	ADC Mode	Register Mode	Hardware Mode	ADC Mode	Register mode
DB0 to DB6	16 to 22	DB0 to DB6		Register data	N/A[1]	N/A	
DB7/$D_{OUT}A$	24	DB7		Register data (MSB)	$D_{OUT}A$	$D_{OUT}A$	$D_{OUT}A$
DB8/$D_{OUT}B$	25	DB8		ADD0	$D_{OUT}B$	$D_{OUT}B$[2]	Unused
DB9/$D_{OUT}C$	27	DB9		ADD1	N/A	$D_{OUT}C$[3]	Unused
DB10/$D_{OUT}D$	28	DB10		ADD2	N/A	$D_{OUT}D$[3]	Unused
DB11/SDI	29	DB11		ADD3	N/A	Unused	SDI
DB12 to DB14	30 to 32	DB12 to DB14		ADD4 to ADD6	N/A		
DB15	33	DB15		R/$\overline{W}$	N/A		

1 N/A means not applicable. Tie all N/A pins to AGND.

2 Only used if 2 $D_{OUT}x$ or 4 $D_{OUT}x$ mode is selected in the CONFIG register. Otherwise, leave unconnected.

3 Only used if 4 $D_{OUT}x$ mode is selected in the CONFIG register. Otherwise, leave unconnected.

DIGITAL INTERFACE

PARALLEL INTERFACE

To read ADC data or to read and write the register content over the parallel interface, tie the PAR/SER SEL pin low.

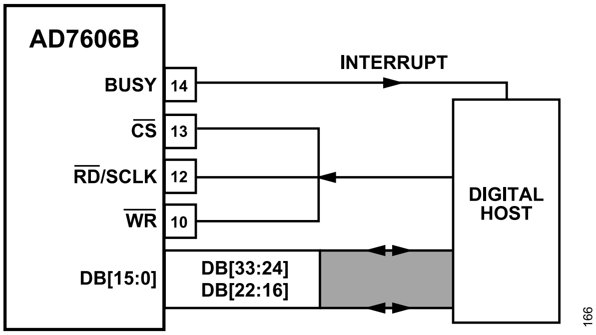


Figure 64. AD7606B Interface Diagram—One AD7606B Using the Parallel Bus, with CS and RD Shorted Together

The rising edge of the CS input signal moves the bus into three-state, and the falling edge of the CS input signal takes the bus out of the high impedance state. CS is the control signal that enables the data lines and it is the function that allows multiple AD7606B devices to share the same parallel data bus.

Reading Conversion Results (Parallel ADC Read Mode)

The falling edge of the RD pin reads data from the output conversion results register. Applying a sequence of RD pulses to the RD pin clocks the conversion results out from each channel to the parallel bus, Bits[DB15:DB0], in ascending order, from V1 to V8, as shown in Figure 66.

The CS signal can be permanently tied low, and the RD signal can access the conversion results, as shown in Figure 3. A read operation of new data can take place after the BUSY signal goes low (see Figure 2). Alternatively, a read operation of data from the previous conversion process can take place while the BUSY pin is high.

When there is only one AD7606B in a system and it does not share the parallel bus, data can be read using one control signal from the digital host. The CS and RD signals can be tied together, as shown in Figure 4. In this case, the falling edge of the CS and RD signals bring the data bus out of three-state and clocks out the data.

The FRSTDATA output signal indicates when the first channel, V1, is being read back, as shown in Figure 4. When the CS input is high, the FRSTDATA output pin is in three-state. The falling edge of CS takes the FRSTDATA pin out of three-state. The falling edge of the RD signal corresponding to the result of V1 sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA pin returns to a logic low following the next falling edge of RD.

Reading During Conversion

The data read operation from the AD7606B, as shown in Figure 65, can occur in the following scenarios:

- After conversion, such as when the BUSY line is low
- During conversion, such as when the BUSY line is high
- Starting while the BUSY line is low and ending while the following conversion, see Figure 2

Reading during conversion has little effect on the performance of the converter, and it allows a faster throughput rate to be achieved. Data can be read from the AD7606B at any time other than on the falling edge of the BUSY signal because this falling edge is when the output data registers are updated with the new conversion data. Any data read while the BUSY signal is high must be completed before the falling edge of the BUSY signal.

Parallel ADC Read Mode with CRC Enabled

In software mode, the parallel interface supports reading the ADC data with the CRC appended, when enabled through the INT_CRC_ERR_EN bit (Address 0x21, Bit 2). The CRC is 16 bits, and it is clocked out after reading all eight channel conversions, as shown in Figure 68. The CRC calculation includes all data on the DBx pins: data, status (when appended), and zeros. See the Diagnostics section for more details on the CRC.

Parallel ADC Read Mode with Status Enabled

In software mode, the 8-bit status header is enabled (see Table 24) by setting STATUS_HEADER in the CONFIG register (Address 0x02, Bit 6), and each channel then takes two frames of data:

- The first frame clocks the ADC data out through DBx.
- The second frame clocks out the status header of the channel on DB15 to DB8, DB15 being the MSB and DB8 the LSB, while DB7 to DB0 clock out zeros.

This sequence is shown in Figure 67. Table 24 explains the status header content and describes each bit.

Table 23. CH.IDx Bits Decoding in Status Header

CH.ID2	CH.ID1	CH.ID0	Channel Number
0	0	0	Channel 1 (V1)
0	0	1	Channel 2 (V2)
0	1	0	Channel 3 (V3)
0	1	1	Channel 4 (V4)
1	0	0	Channel 5 (V5)
1	0	1	Channel 6 (V6)
1	1	0	Channel 7 (V7)
1	1	1	Channel 8 (V8)

DIGITAL INTERFACE

Table 24. Status Header, Parallel Interface

Bit Details	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Content	RESET_DETECT	DIGITAL_ERROR	OPEN_DETECTED	AIN_OV_DIAG_ERR	AIN_UV_DIAG_ERR	CH.ID2	CH.ID1	CH.ID0
Meaning[1]	Reset detected	Error flag on Address 0x22	The analog input of this channel is open	Overvoltage detected on this channel	Undervoltage detected on this channel	Channel ID (see Table 23)		

[1] See the Diagnostics section for more information.

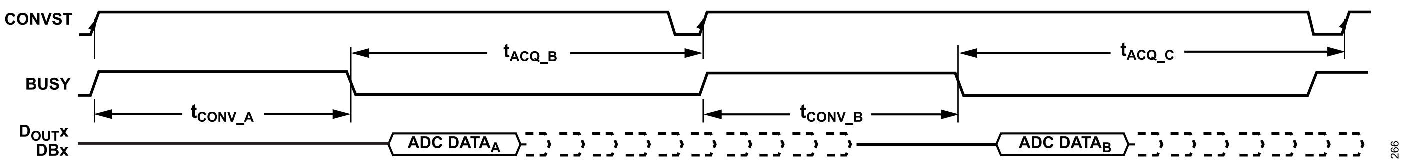


Figure 65. ADC Data Read Can Happen After Conversion and/or During the Following Conversion

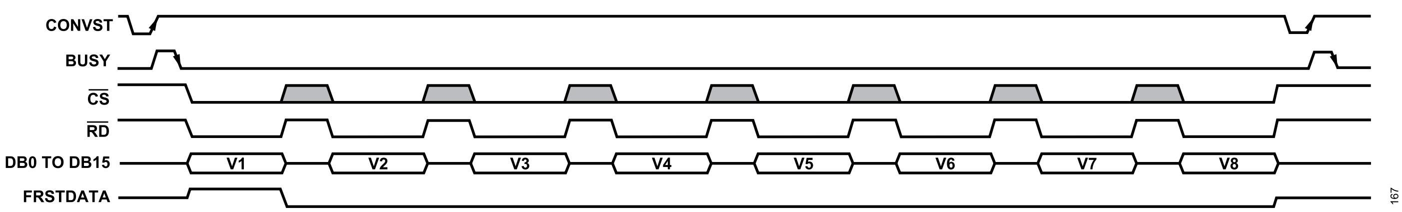


Figure 66. Parallel Interface, ADC Read Mode

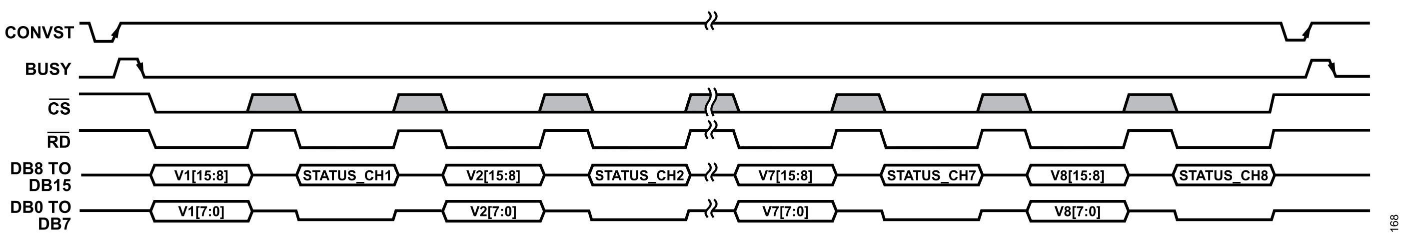


Figure 67. Parallel Interface, ADC Read Mode with Status Header Enabled

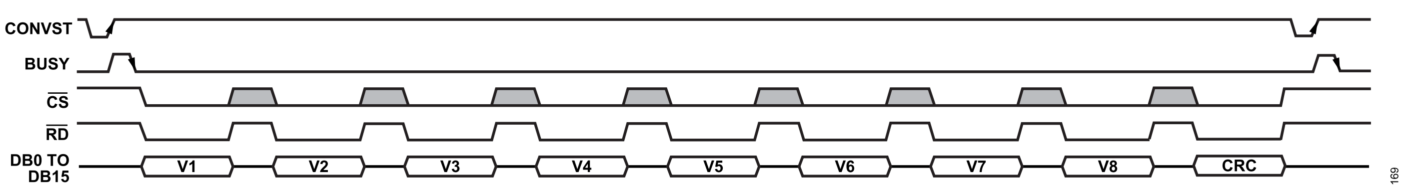


Figure 68. Parallel Interface, ADC Read Mode with CRC Enabled

DIGITAL INTERFACE

Parallel Register Mode (Reading Register Data)

In software mode, all the registers in Table 31 can be read over the parallel interface. Bits[DB15:DB0] leave a high impedance state when both the $\overline{CS}$ signal and $\overline{WR}$ signal are logic low for reading register content, or when both the $\overline{CS}$ signal and $\overline{RD}$ signal are logic low for writing register address and/or register content.

A register read is performed through two frames: first, a read command is sent to the AD7606B and second, the AD7606B clocks out the register content. The format for a register read command is shown in the leading two frames of Figure 69. On the first frame, the following occurs:

- Bit DB15 must be set to 1 to select a read command. The read command places the AD7606B in register mode.
- Bits [DB14:DB8] must contain the register address.
- The subsequent eight bits, Bits[DB7:DB0], are ignored.

The register address is latched on the AD7606B on the rising edge of the $\overline{WR}$ signal. The register content can then be read from the latched register by bringing the $\overline{RD}$ line low on the following frame, as follows:

- Bit DB15 is pulled to 0 by the AD7606B.
- Bits[DB14:DB8] provide the register address being read.
- The subsequent eight bits, Bits[DB7:DB0], provide the register content.

To revert to ADC read mode, write to Address 0x00, as shown in the Parallel Register Mode (Writing Register Data) section. No ADC data can be read while the device is in register mode.

Parallel Register Mode (Writing Register Data)

In software mode, all the R/W registers in Table 31 can be written to over the parallel interface. To write a sequence of registers, firstly exit ADC read mode (default mode) by reading any register on the memory map as explained in Parallel Register Mode (Reading Register Data) section. A register write command is performed by a single frame, through the parallel bus (Bits[DB15:DB0]), $\overline{CS}$ signal, and $\overline{WR}$ signal. The format of a write command, as shown in Figure 69, is structured as follows:

- Bit DB15 must be set to 0 to select a write command.
- Bits[DB14:DB8] contain the register address.
- The subsequent eight bits, Bits[DB7:DB0], contain the data to be written to the selected register.

Data is latched onto the device on the rising edge of the $\overline{WR}$ pin. To revert to ADC read mode, write to Address 0x00. No ADC data can be read while the device is in register mode.

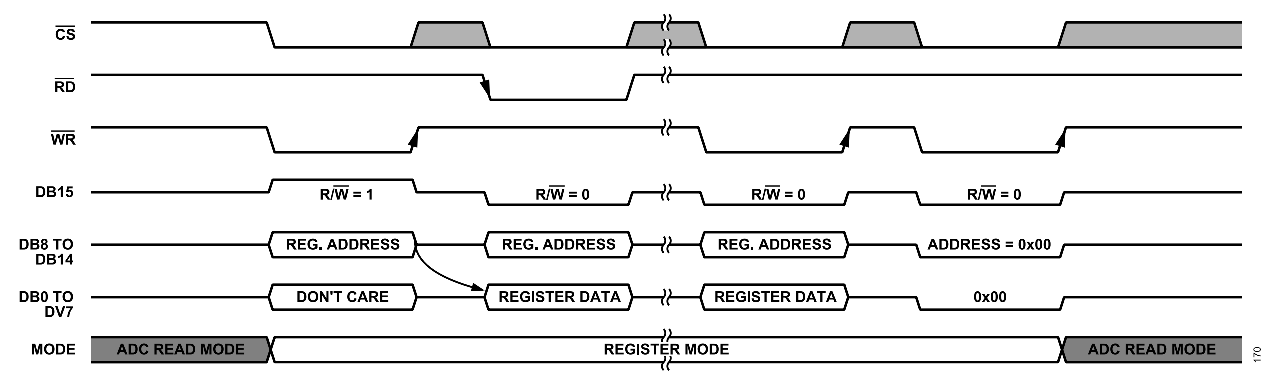


Figure 69. Parallel Interface Register Read Operation, Followed by a Write Operation

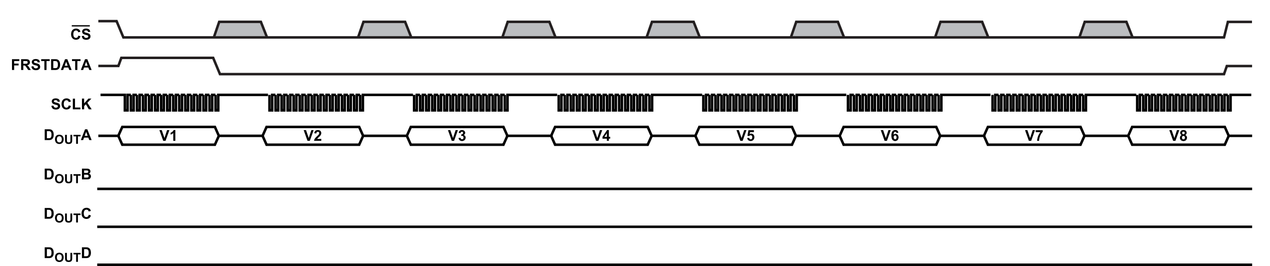


Figure 70. Serial Interface ADC Reading, One $D_{OUT}x$ Line

DIGITAL INTERFACE

SERIAL INTERFACE

To read ADC data or to read/write the content of the register over the serial interface, tie the $\overline{\text{PAR}}$/SER SEL pin high.

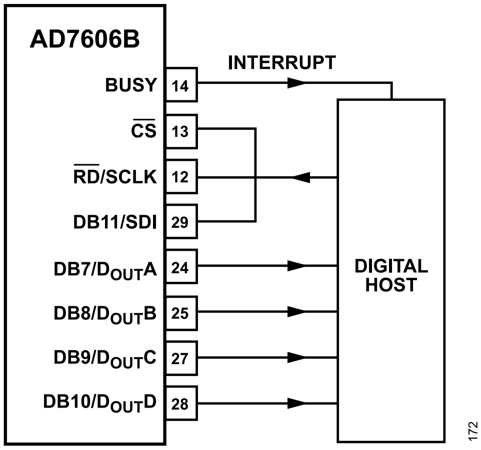


Figure 71. AD7606B Interface Diagram—One AD7606B Using the Serial Interface with Four D_{OUT}x Lines

Reading Conversion Results (Serial ADC Read Mode)

The AD7606B has four serial data output lines: D_{OUT}A, D_{OUT}B, D_{OUT}C, and D_{OUT}D. In software mode, data can be read back from the AD7606B using either one (see Figure 71), two (see Figure 72), four (see Figure 73), depending on the configuration set in the CONFIG register.

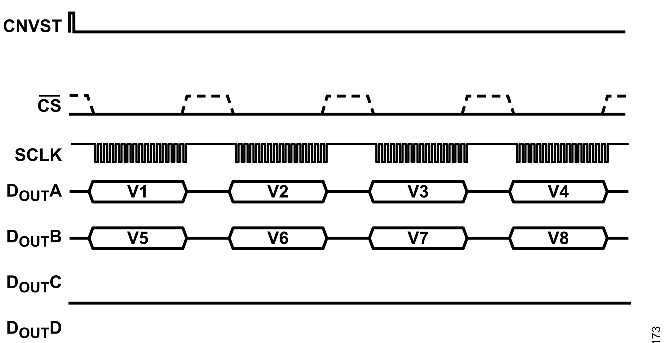


Figure 72. Serial Interface ADC Reading, Two D_{OUT}x Lines

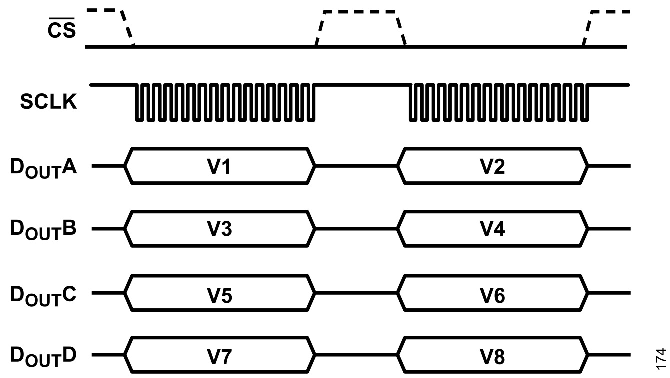


Figure 73. Serial Interface ADC Reading, Four D_{OUT}x Lines

Table 25. D_{OUT}x Format Selection, Using the CONFIG Register (Address 0x02)

D_{OUT}x Format	Address 0x02, Bit 4	Address 0x02, Bit 3
1 D_{OUT}x	0	0
2 D_{OUT}x	0	1
4 D_{OUT}x	1	0
1 D_{OUT}x	1	1

In hardware mode, only the 2 D_{OUT}x lines option is available. However, all channels can be read from D_{OUT}A by providing eight 16-bit SPI frames between two CONVST pulses.

The $\overline{\text{CS}}$ falling edge takes the data output lines, D_{OUT}A to D_{OUT}D, out of three-state and clocks out the MSB of the conversion result.

In 3-wire mode ($\overline{\text{CS}}$ tied low), instead of $\overline{\text{CS}}$ clocking out the MSB, the falling edge of the BUSY signal clocks out the MSB. The rising edge of the SCLK signal clocks all the subsequent data bits on the serial data outputs, D_{OUT}A to D_{OUT}D, as shown in Figure 6. The $\overline{\text{CS}}$ input can be held low for the entire serial read operation, or it can be pulsed to frame each channel read of 16 SCLK cycles (see Figure 72). However, if $\overline{\text{CS}}$ is pulsed during a channel conversion result transmission before reaching the LSB, the channel that was interrupted retransmits on the next frame, completely starting again from the MSB.

Data can also be clocked out using only the D_{OUT}A line, as shown in Figure 70. For the AD7606B to access all eight conversion results on one D_{OUT}x line, a total of 128 SCLK cycles is required. In hardware mode, these 128 SCLK cycles must be framed in groups of 16 SCLK cycles by the $\overline{\text{CS}}$ signal. The disadvantage of using just one D_{OUT}x line is that the throughput rate is reduced if reading occurs after conversion. Leave the unused D_{OUT}x lines unconnected in serial mode.

Figure 73 shows a read of eight simultaneous conversion results using four D_{OUT}x lines on the AD7606B, available in software mode. In this case, a 32 SCLK transfer accesses data from the AD7606B, and $\overline{\text{CS}}$ is either held low to frame the entire 32 SCLK cycles or is pulsed between two 16-bit frames. This mode is only available in software mode, and it is configured using the CONFIG register (Address 0x02).

DIGITAL INTERFACE

Figure 6 shows the timing diagram for reading one channel of data, framed by the $\overline{CS}$ signal, from the AD7606B in serial mode. The SCLK input signal provides the clock source for the serial read operation. The $\overline{CS}$ signal goes low to access the data from the AD7606B.

The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. In serial mode, the falling edge of the $\overline{CS}$ signal takes the FRSTDATA pin out of three-state and sets the FRSTDATA pin high if the BUSY line is already deasserted, indicating that the result from V1 is available on the $D_{OUT}A$ output data line. The FRSTDATA output returns to a logic low following the 16^{th} SCLK falling edge. If the $\overline{CS}$ pin is tied permanently low (3-wire mode), the falling edge of the BUSY line sets the FRSTDATA pin high when the result from V1 is available on $D_{OUT}A$.

If SDI is tied low or high, nothing is clocked to the AD7606B. Therefore, the device remains clocking out conversion results. When using the AD7606B in 3-wire mode, keep SDI at a high level. While in ADC read mode, single-write operations can be performed, as shown in Figure 74. For writing a sequence of registers, switch to register mode, as described in the Serial Register Mode (Writing Register Data) section.

Reading During Conversion—Serial Interface

The data read operation from the AD7606B, as shown in Figure 65, occurs in the following scenarios:

- After conversion, such as when the BUSY line is low
- During conversion, such as when the BUSY line is high
- Starts when the BUSY line is low and ends during the following conversion, see Figure 2.

Reading during conversion has little effect on the performance of the converter, and it allows a faster throughput rate to be achieved. Data can be read from the AD7606B at any time other than on the falling edge of the BUSY signal because this falling edge is when the output data registers are updated with the new conversion data. Any data read while the BUSY signal is high must be completed before the falling edge of the BUSY signal.

Serial ADC Read Mode with CRC Enabled

In software mode, the CRC can be enabled by writing to the register map. In this case, the CRC is appended on each $D_{OUT}x$ line after the last channel is clocked out, as shown in Figure 81. See the Interface CRC Checksum section for more information on how the CRC is calculated.

Serial ADC Read Mode with Status Enabled

In software mode, the 8-bit status header (see Table 26) can be turned on when using the serial interface so that it is appended after each 16-bit data conversion, extending the frame size to 24 bits per channel, as shown in Figure 74.

Serial Register Mode (Reading Register Data)

All the registers in Table 31 can be read over the serial interface. The format for a read command is shown in Figure 75. A read command consists of two 16-bit frames. On the first frame, perform the following:

- The first bit clocked in SDI must be set to 0 to enable writing the address.
- The second bit clocked in SDI must be set to 1 to select a read command.
- Bits[3:8] in SDI contain the register address to be clocked out on $D_{OUT}A$ on the following frame.
- The subsequent eight bits, Bits[9:16], clocked in SDI are ignored.

If the AD7606B is in ADC read mode, the serial data out (SDO) keeps clocking ADC data on Bits[9:16], and then the AD7606B switches to register mode.

If the AD7606B is in register mode, the SDO reads back the content from the previous addressed register, no matter if the previous frame was a read or a write command. To exit register mode write to Address 0x00 is required, as shown in Figure 76.

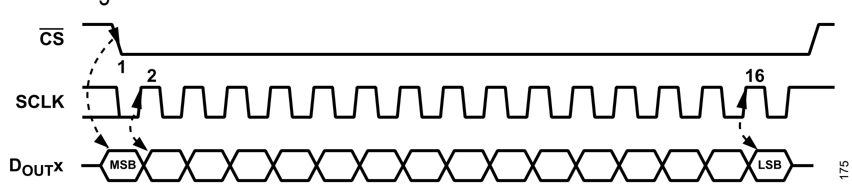


Figure 74. Serial Interface, ADC Read Mode

DIGITAL INTERFACE

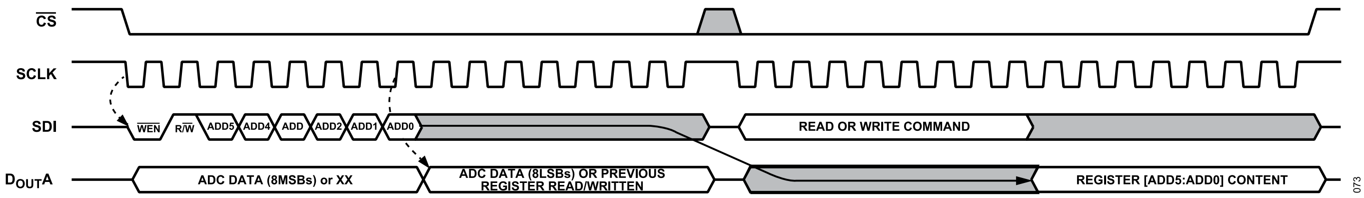


Figure 75. Serial Interface Read Command, First Frame Points the Address, Second Frame Provides the Register Content

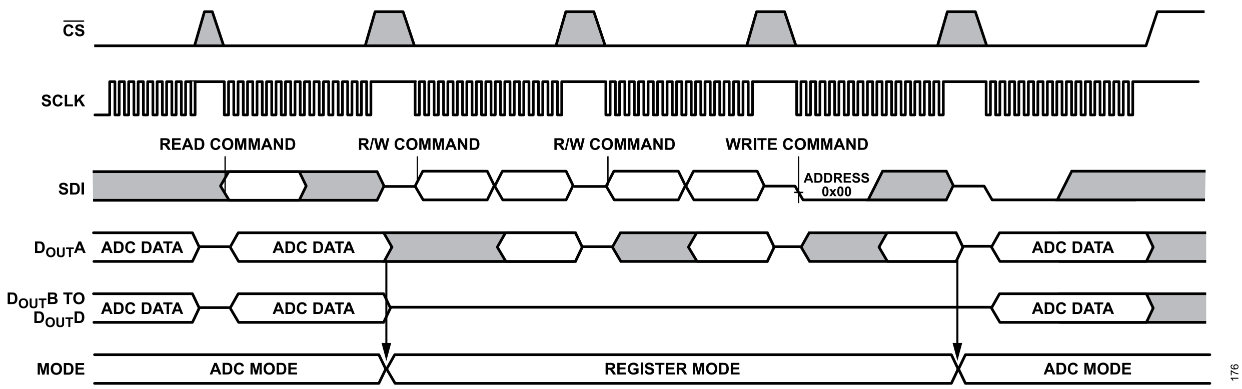


Figure 76. AD7606B Register Mode

Table 26. Status Header, Serial Interface

Bit Details	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Content	RESET_DETECT	DIGITAL_ERROR	OPEN_DETECTED	AIN_OV_DIAG_ERR	AIN_UV_DIAG_ERR	CH.ID 2	CH.ID 1	CH.ID 0
Meaning[1]	Reset detected	Error flag on Address 0x22	At least one analog input is open on a channel	Overvoltage detected on a channel	Undervoltage detected on a channel	Channel ID (see Table 23)		

[1] See the Diagnostics section for more information.

DIGITAL INTERFACE

Serial Register Mode (Writing Register Data)

In software mode, all the read/write registers in Table 31 can be written to the serial interface. To write a sequence of registers, exit ADC read mode (default mode) by reading any register on the memory map. A register write command is performed by a single 16-bit SPI access. The format for a write command is shown in Figure 77, and is structured as follows:

- The first bit clocked in SDI must be set to 0 to enable a write command.
- The second bit clocked in SDI, the R/W̄ bit, must be cleared to 0.
- Bit ADD5 to Bit ADD0 clocked in SDI contain the register address to be written.
- The subsequent eight bits (Bits[DIN7:DIN0]) contain the data to be written to the selected register. Data is clocked in from SDI on the falling edge of SCLK, while data is clocked out on $D_{OUT}A$ on the rising edge of SCLK.

When writing continuously to the device, the data that appears on $D_{OUT}A$ is from the register address that was written to on the previous frame, as shown in Figure 77. The $D_{OUT}B$, $D_{OUT}C$, and $D_{OUT}D$ lines are kept low during the transmission.

While in register mode, no ADC data is clocked out because the $D_{OUT}x$ lines are used to clock out register content. When finished writing all needed registers, a write to Address 0x00 returns the AD7606B to ADC read mode, where the ADC data is again clocked out on the $D_{OUT}x$ lines, as shown in Figure 76.

In software mode, when the CRC is turned on, eight additional bits are clocked in and out on each frame. Therefore, 24-bit frames are required.

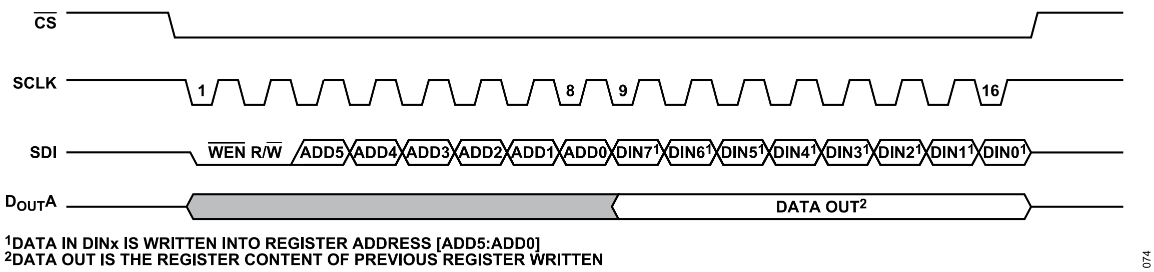


Figure 77. AD7606B Serial Interface, Single Write Command, SDI Clocks in the Address Bit ADD5 to Bit ADD0 and the Register Content Bit DIN7 to Bit DIN0 During the Same Frame, $D_{OUT}A$ Provides Register Content Requested on the Previous Frame

DIGITAL INTERFACE

Serial Register Mode with CRC

Registers can be written to and read from the AD7606B with cyclic redundancy check (CRC) enabled in software mode, by asserting the INT_CRC_ ERR_EN bit (Address 0x21, Bit 2).

When reading a register, the AD7606B provides eight additional bits on the $D_{OUT}A$ line with the CRC resultant of the data shifted out previously on the same frame. The controller can then check whether the data received is correct by applying the following polynomial:

$x^8 + x^2 + x + 1$

With the CRC enabled, the SPI frames extend to 24 bits in length, as shown in Figure 78.

When writing a register, the controller must clock the data (register address plus register content) in the AD7606B followed by an 8-bit CRC word, calculated from the previous 16 bits using the previously described polynomial. The AD7606B reads the register address and the register content, calculates the corresponding 8-bit CRC word, and asserts the INT_CRC_ERR bit (Address 0x22, Bit 2) if the calculated CRC word does not match the CRC word received between the 17th and 24th bit through SDI, as shown in Figure 79.

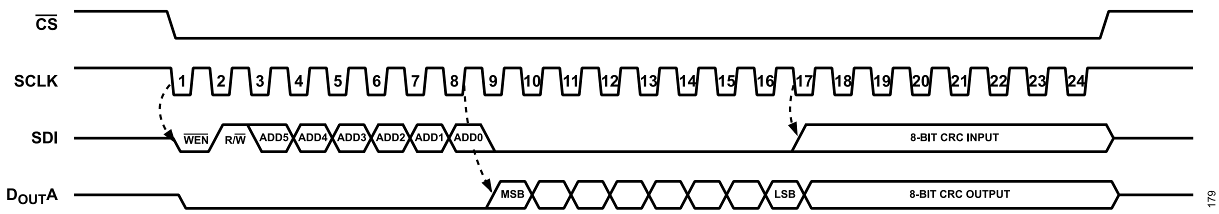


Figure 78. Reading Registers Through the SPI Interface with CRC Enabled

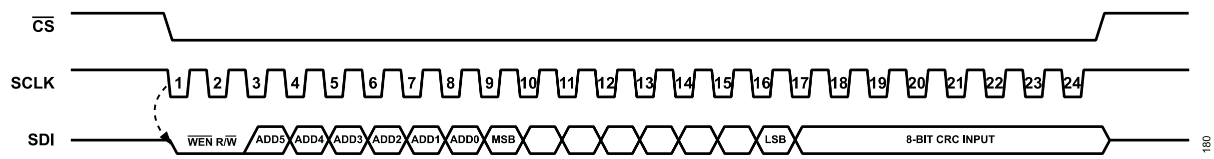


Figure 79. Writing Registers Through the SPI Interface with CRC Enabled

DIAGNOSTICS

Diagnostic features are available in software mode to verify correct operation of the AD7606B. The list of diagnostic monitors includes reset detection, overvoltage detection, undervoltage detection, analog input open circuit detection, and digital error detection.

If an error is detected, a flag asserts on the status header, if enabled, as described in the Digital Interface section. This flag points to the registers on which the error is located, as explained in the following sections.

In addition, a diagnostic multiplexer can dedicate any channel to verify a series of internal nodes, as explained in the Diagnostics Multiplexer section.

RESET DETECTION

The RESET_DETECT bit on the status register (Address 0x01, Bit 7) asserts if either a partial reset or full reset pulse is applied to the AD7606B. On power-up, a full reset is required. This reset asserts the RESET_DETECT bit, indicating that the power-on reset (POR) initialized correctly on the device.

The POR monitors the REGCAP voltage and issues a full reset if the voltage drops under a certain threshold.

The RESET_DETECT bit can be used to detect an unexpected device reset or a large glitch on the RESET pin, or a voltage drop on the supplies.

The RESET_DETECT bit is only cleared by reading the status register.

OVERVOLTAGE AND UNDERVOLTAGE EVENTS

The AD7606B includes on-chip overvoltage and undervoltage circuitry on each analog input pin. These comparators can be enabled or disabled using the AIN_OV_UV_DIAG_ ENABLE register (Address 0x25).

After this register is enabled, when the voltage on any analog input pin goes above the overvoltage threshold shown in Table 27, the AIN_OV_DIAG_ERROR register (Address 0x26) shows which channel or channels have an overvoltage event. When a bit within the AIN_OV_DIAG_ERROR register asserts, it stays at a high state even after the overvoltage event disappears. To clear the error bit, the error bit must be overwritten to 1 or the error checker must be disabled.

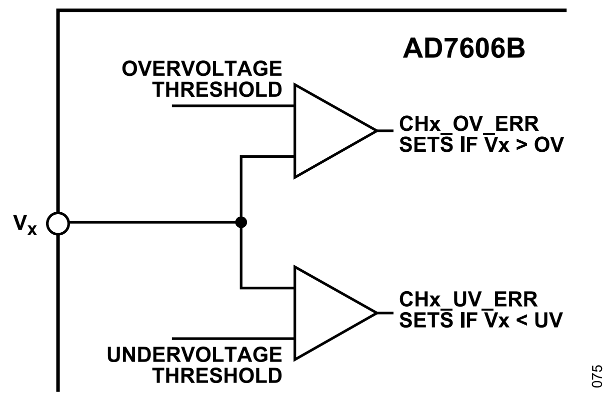


Figure 80. Overvoltage and Undervoltage Circuitry on Each Analog Input

When the voltage on any analog input pin goes below the undervoltage threshold shown in Table 27, the AIN_UV_ DIAG_ERROR register (Address 0x27) shows which channel or channels have an undervoltage event. When a bit within the AIN_UV_DIAG_ERROR register asserts, it stays at a high state after the undervoltage event disappears. To clear the error bit, the error bit must be overwritten to 1 or the error checker must be disabled.

Table 27. Overvoltage and Undervoltage Thresholds

Analog Input Range (V)	Overvoltage Threshold (V)	Undervoltage Threshold (V)
±2.5	+6.5	−3
±5	+8	−5.5
±10	+12	−11

DIGITAL ERROR

Both the status register and status header contain a DIGITAL_ERROR bit. This bit asserts when any of the following monitors trigger:

- Memory map CRC, read only memory (ROM) CRC, and digital interface CRC
- SPI invalid read or write
- BUSY stuck high

To find out which monitor triggered the DIGITAL_ERROR bit, the DIGITAL_DIAG_ERR address (Address 0x22) has a bit dedicated for each monitor, as explained in the following sections.

ROM CRC

The ROM stores the factory trimming settings for the AD7606B. After power-up, the ROM content is loaded to registers during device initialization. After the load, a CRC is calculated on the loaded data and verified if the result matches the CRC stored in the ROM.

The AD7606B uses the following 16- bit CRC polynomial to calculate the CRC checksum value on the memory map:

$$x^{16}+x^{14}+x^{12}+x^{10}+x^{8}+x^{6}+x^{4}+x^{3}+x+1 \text{ (0xBAAD)} \quad (8)$$

DIAGNOSTICS

If the calculated and stored CRC values do not match, the error checking and correction (ECC) block can detect up to 3-bit errors (hamming distance of 4). Otherwise, the ROM_CRC_ERR (Address 0x22, Bit 0) asserts. When ROM_CRC_ERR asserts after power-up, it is recommended to issue a full reset to reload all factory settings.

This ROM CRC monitoring feature is enabled by default but can be disabled by clearing the ROM_CRC_ERR_EN bit (Address 0x21, Bit 0).

Memory Map CRC

For added robustness, a CRC calculation is performed on the on-chip registers. The memory map CRC is disabled by default. After the AD7606B is configured in software mode through writing the required registers, the memory map CRC can be enabled through the MM_CRC_ERR_EN bit (Address 0x21, Bit 1). When enabled, the CRC calculation is performed on the entire memory map and stored. Every time the memory map is written, the CRC is recalculated and the new value stored.

The AD7606B uses the following 16-bit CRC polynomial to calculate the CRC checksum value on the memory map:

$$x^{16}+x^{14}+x^{12}+x^{10}+x^{8}+x^{6}+x^{4}+x^{3}+x+1 \text{ (0xBAAD)} \quad (9)$$

The ECC block can detect up to three bits of errors (Hamming distance of four bits) within the memory map. Moreover, every 4 μs, the CRC on the memory map is recalculated and compared to the stored CRC value. If the calculated and the stored CRC values do not match, the memory map is corrupted and the MM_CRC_ERR bit asserts.

If the MM_CRC_ERR bit asserts, it is recommended to write to the memory map to recalculate the CRC. If the MM_CRC_ERR persists, it is recommended to issue a full reset to restore the default contents of the memory map.

Interface CRC Checksum

The AD7606B has a CRC checksum mode to improve interface robustness by detecting errors in data transmission. The CRC feature is available in both ADC read modes (serial and parallel) and register mode (serial only).

The AD7606B uses the following 16-bit CRC polynomial to calculate the CRC checksum value:

$$x^{16}+x^{14}+x^{12}+x^{10}+x^{8}+x^{6}+x^{4}+x^{3}+x+1 \text{ (0xBAAD)} \quad (10)$$

To replicate the polynomial division in hardware, the data shifts left by 16 bits to create a number ending in 16 Logic 0s. The polynomial is aligned so that the MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure repeats. This process repeats until the original data is reduced to a value less than the polynomial, the 16-bit checksum.

An example of the CRC calculation for the 16-bit data is shown in Table 28. The CRC corresponding to the data 0x064E, using the previously described polynomial, is 0x2137.

The serial interface supports the CRC when enabled via the INT_CRC_ERR_EN bit (Address 0x21, Bit 2). The CRC is a 16-bit word that is appended to the end of each $D_{OUT}x$ in use, after reading all the channels. An example using four $D_{OUT}x$ lines is shown in Figure 81.

If using two $D_{OUT}x$ lines ($D_{OUT}A$ and $D_{OUT}B$), each 16-bit CRC word is calculated using data from four channels, that is 64 bits, as shown in Figure 82. If using only one $D_{OUT}x$ line, all eight channels are clocked out through $D_{OUT}A$, followed by the 16-bit CRC word calculated using data from the eight channels, that is, 128 bits.

If using four $D_{OUT}x$ lines, each 16-bit CRC word is calculated using data from two channels 32 bits. If using eight $D_{OUT}x$ lines, each 16-bit CRC word is calculated using data from one channel 16 bits.

Table 28. Example CRC Calculation for 16-Bit Data[1]

Data[2]	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Process Data	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Polynomial						1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1										
						0	1	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	0									
							1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1									
							0	1	0	1	1	1	0	0	0	1	1	1	0	1	1	0	1	0								
								1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1								
								0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0		
														1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1		
														0	0	1	0	1	0	1	0	1	0	0	0	1	1	0	1	1	0	0

DIAGNOSTICS

Table 28. Example CRC Calculation for 16-Bit Data[1] (Continued)

Data[2]	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Process Data	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
																1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1
CRC																	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1

1 Table 28 represents the division of the data. Blank cells are for formatting purposes.

2 X means don't care.

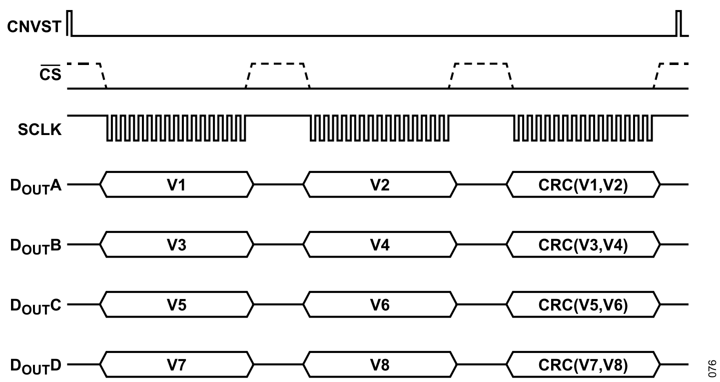


Figure 81. Serial Interface ADC Reading with CRC On, Four D_{OUT}x Lines

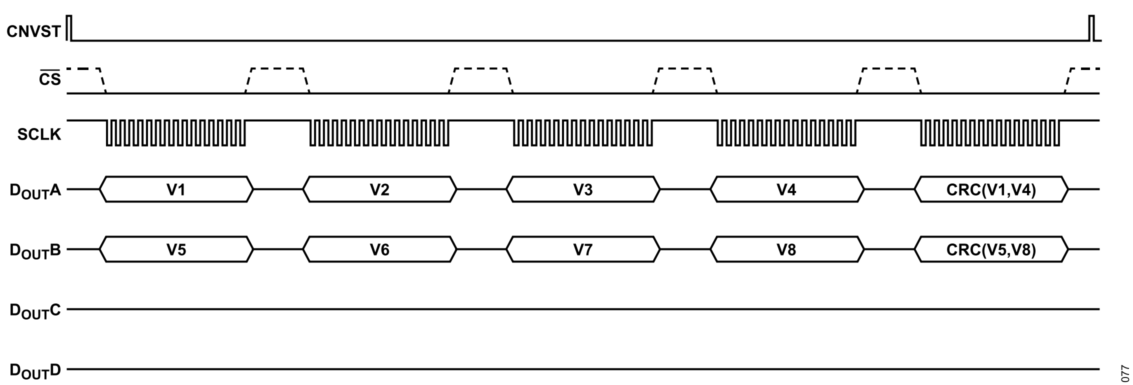


Figure 82. Serial Interface ADC Reading with CRC On, Two D_{OUT}x Lines

DIAGNOSTICS

When the AD7606B is in register mode, that is, when registers are being read or written, the CRC polynomial used is $x^8 + x^2 + x + 1$. When reading a register, and CRC is enabled, each SPI frame is 24 bits long and the CRC 8-bit word is clocked out from the 17th to 24th SCLK cycle. Similarly, when writing a register, a CRC word can be appended on the SDI line, as shown in Figure 83 and the AD7606B checks and triggers an error, INT_CRC_ERR (Address 0x22, Bit 2), if the CRC given and the internally calculated do not match.

The parallel interface also supports CRC in ADC mode only, and it is clocked out through DB15 to DB0 after Channel 8, as shown in Figure 68. The 16-bit CRC word calculated using data from the eight channels, that is, 128 bits.

Interface Check

The integrity of the digital interface can be checked by setting the INTERFACE_CHECK_EN bit (Address 0x21, Bit 7). Selecting the interface check forces the conversion result registers to a known value, as shown in Table 29.

Verifying that the controller receives the data shown in Table 29 ensures that the interface between the AD7606B and the controller operates properly. If the interface CRC is enabled because the data transmitted is known, this mode verifies that the controller performs the CRC calculation properly.

Table 29. Interface Check Conversion Results

Channel Number	Conversion Result Forced (Hexadecimal)
V1	0xACCA
V2	0x5CC5
V3	0xA33A
V4	0x5335
V5	0xCAAC
V6	0xC55C
V7	0x3AA3
V8	0x3553

SPI Invalid Read/Write

When attempting to read back an invalid register address, the SPI_READ_ERR bit (Address 0x22, Bit 4) is set. The invalid readback address detection can be enabled by setting the SPI_READ_ERR_EN bit (Address 0x21, Bit 4). If an SPI read error is triggered, it is cleared by overwriting that bit or disabling the checker.

When attempting to write to an invalid register address or a read only register, the SPI_WRITE_ERR bit (Address 0x22, Bit 3) is set. The invalid write address detection can be enabled by setting the SPI_WRITE _ERR bit (Address 0x21, Bit 3). If an SPI write error is triggered, it is cleared by overwriting that bit or disabling the checker.

BUSY Stuck High

BUSY stuck high monitoring is enabled by setting the BUSY_STUCK_HIGH_ERR_EN bit (Address 0x21, Bit 5). After this bit is enabled, the conversion time (t_{CONV} in Table 3) is monitored internally with an independent clock. If t_{CONV} exceeds 4 μs, the AD7606B automatically issues a partial reset and asserts the BUSY_STUCK_HIGH_ERR bit (Address 0x22, Bit 5). To clear this error flag, the BUSY_STUCK_HIGH_ERR bit must be overwritten with a 1.

When oversampling mode is enabled, the individual conversion time for each internal conversion is monitored.

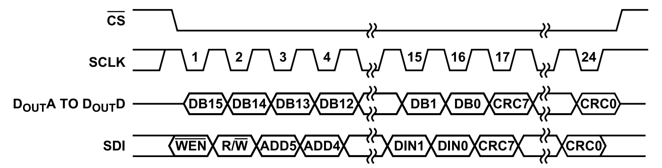


Figure 83. Register Write with CRC On

Internal Clock Counters

The AD7606B uses an internal clock related to functional safety features (FS_CLK) and an internal clock for oversampling (OS_CLK). Both internal clocks run at 16 MHz. To verify the clocks are correctly operating, enable the clock counter through the CLK_FS_OS_COUNTER_EN bit in Register 0x21, Bit 6. These clock counters increment by 1 every time 64 clocks are counted. Therefore, if either the FS_CLK_COUNTER register (Address 0x2D) or the OS_CLK_COUNTER register (Address 0x2E) is read after a certain known delay that corresponds to the chosen feature, the register values must match the equivalent count for the time elapsed.

For example, if the clock counter is enabled and the FS_CLK_COUNTER register is read after 20 μs between the write and read operations, the value must equal to 0x05. The following equation calculates the FS_CLK_COUNTER value:

$$FS\_CLK\_COUNTER = Delay \times \frac{16\ \text{MHz}}{64} \tag{11}$$

where *Delay* is the delay shown in Figure 85.

DIAGNOSTICS

DIAGNOSTICS MULTIPLEXER

All eight input channels contain a diagnostics multiplexer in front of the PGA that allows monitoring of the internal nodes described in Table 30 to ensure the correct operation of the AD7606B. For accurate measurements, it is recommended to use only Channel 8. Connecting more channels to the diagnostic multiplexer simultaneously degrades the performance.

Table 30 shows the bit decoding for the diagnostic mux register on Channel 1, as an example. When an internal node is selected, the input voltage at input pins are deselected from the PGA, as shown in Figure 84.

Each diagnostic multiplexer configuration is accessed, in software mode through the corresponding register (Address 0x28 to Address 0x2B). To use the multiplexer on one channel, the ±10 V range must be selected on that channel.

Table 30. Diagnostic Mux Register Bit Decoding of Channel 1

Address 0x28			
Bit 2	**Bit 1**	**Bit 0**	**Signal on Channel 1**
0	0	0	V1
0	0	1	Temperature sensor
0	1	0	4 × V_{REF}
0	1	1	4 × ALDO
1	0	0	4 × DLDO
1	0	1	V_{DRIVE}
1	1	0	AGND
1	1	1	AV_{CC}

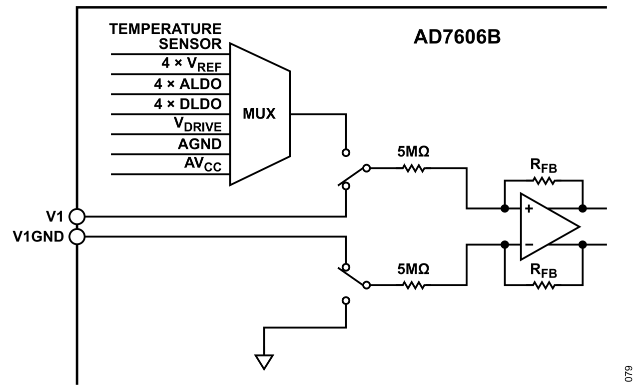


Figure 84. Diagnostic Multiplexer (Channel 1 Shown as an Example) (R_{FB} = Feedback Resistor)

Temperature Sensor

The temperature sensor can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 84. The temperature sensor voltage is measured and is proportional to the die temperature, as per the following equation:

$$Temperature(°C) = \frac{ADC_{OUT}(V) - 0.68323(V)}{0.001633(V/°C)} + 25(°C)$$

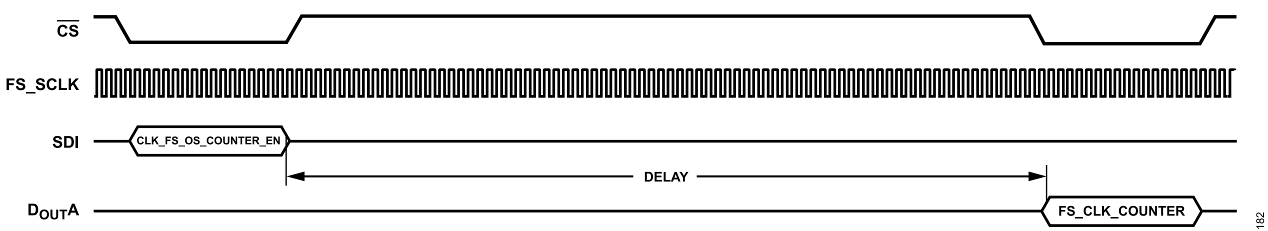


Figure 85. FS_CLK_COUNTER Functionality

DIAGNOSTICS

Reference Voltage

The reference voltage can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 86. The internal or external reference is selected as the input to the diagnostic multiplexer based on the REF SELECT pin. Ideally, the ADC output follows the voltage reference level ratiometrically. Therefore, if the ADC output goes beyond the expected 2.5 V, either the reference buffer or the PGA is malfunctioning.

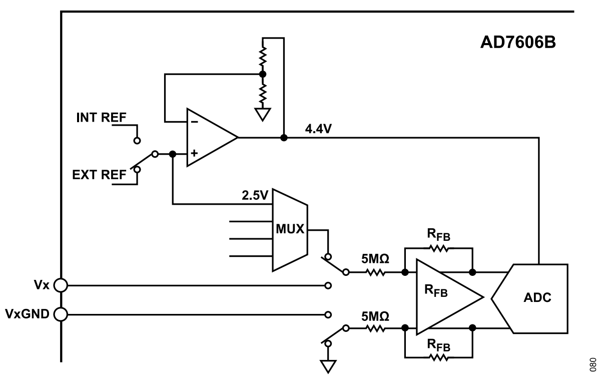


Figure 86. Reference Voltage Signal Path Through the Diagnostic Multiplexer

Internal LDOs

The analog and digital LDO (REGCAP pins) can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 84. The ADC output is four times the voltage on the REGCAPA and REGCAPD pins for the ALDO and DLDO, respectively. This measurement verifies that each LDO is at the correct operating voltage so that the internal circuitry is biased correctly.

Supply Voltages

AV_{CC}, V_{DRIVE}, and AGND can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 84. This setup ensures the voltage and grounds are applied to the device for correct operation.

If V_{DRIVE} is below 4.3 V, the following correction factor is needed to measure AV_{CC} properly:

$$AVCC(\text{V}) = ADC_{OUT}(\text{V}) - 0.1637 \times V_{DRIVE} + 0.6864(\text{V}) \quad (12)$$

TYPICAL CONNECTION DIAGRAM

There are four AV_{CC} supply pins on the device. It is recommended that each of the four pins is decoupled using a 100 nF capacitor at each supply pin and a 10 μF capacitor at the supply source. The AD7606B can operate with the internal reference or an externally applied reference. When using a single AD7606B device on the board, decouple the REFIN/REFOUT pin with a 100 nF capacitor. Refer to the Reference section when using an application with multiple AD7606B devices. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 μF ceramic capacitor.

The V_{DRIVE} supply is connected to the same supply as the processor. The V_{DRIVE} voltage controls the voltage value of the output logic signals. For more information on layout, decoupling, and grounding, see the Layout Guidelines section.

After supplies are applied to the AD7606B, apply a reset to the AD7606B to ensure that it is configured for the correct mode of operation.

In Figure 87, the AD7606B is configured in hardware mode and is operating with the internal reference because the REF SELECT pin is set to logic high. In this example, the device also uses the parallel interface because the $\overline{\text{PAR}}$/SER SEL pin is tied to AGND. The analog input range for all eight channels is ±10 V, provided the RANGE pin is tied to a high level and the oversampling ratio is controlled through the OSx pins by the controller.

In Figure 88, the AD7606B is configured in software mode, because all three OS2, OS1, and OS0 pins are at logic level high. The oversampling ratio, as well as each channel range, are configured through accessing the memory map. In this example, the $\overline{\text{PAR}}$/SER SEL pin is at logic level high. Therefore, the serial interface is used for both reading the ADC data and reading and writing the memory map. The REF SELECT pin is tied to AGND. Therefore, the internal reference is disabled and an external reference is connected externally to the REFIN/REFOUT pin and decoupled through a 100 nF capacitor.

Figure 87 and Figure 88 are examples of typical connection diagrams. Other combinations of reference, data interface, and operation mode are also possible, depending on the logic levels applied to each configuration pin.

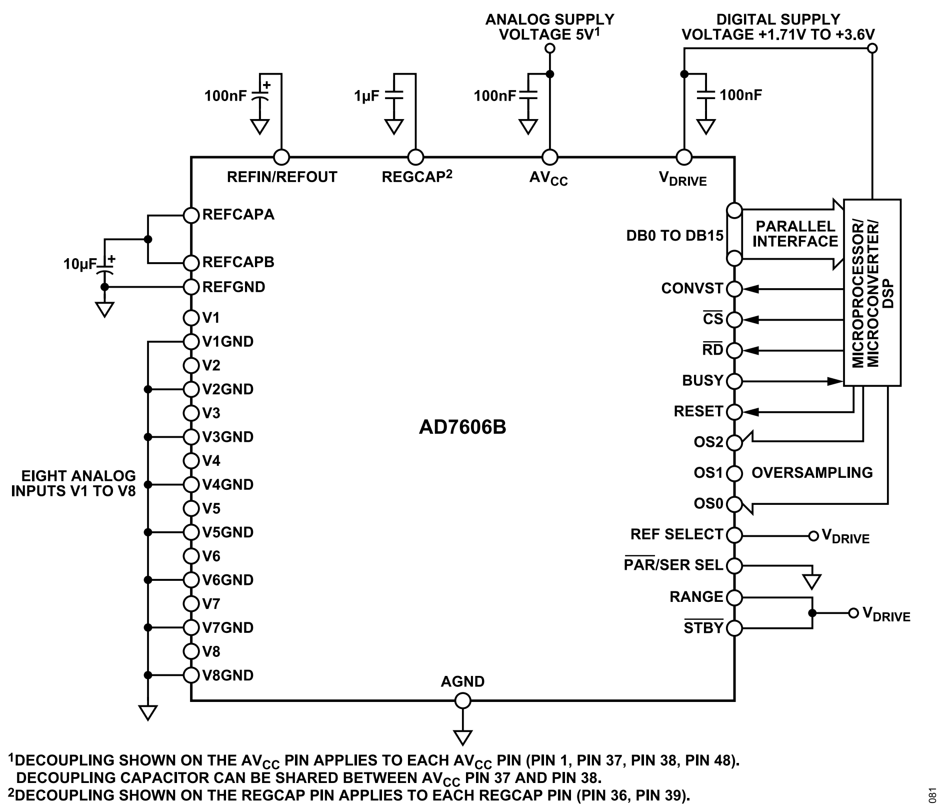
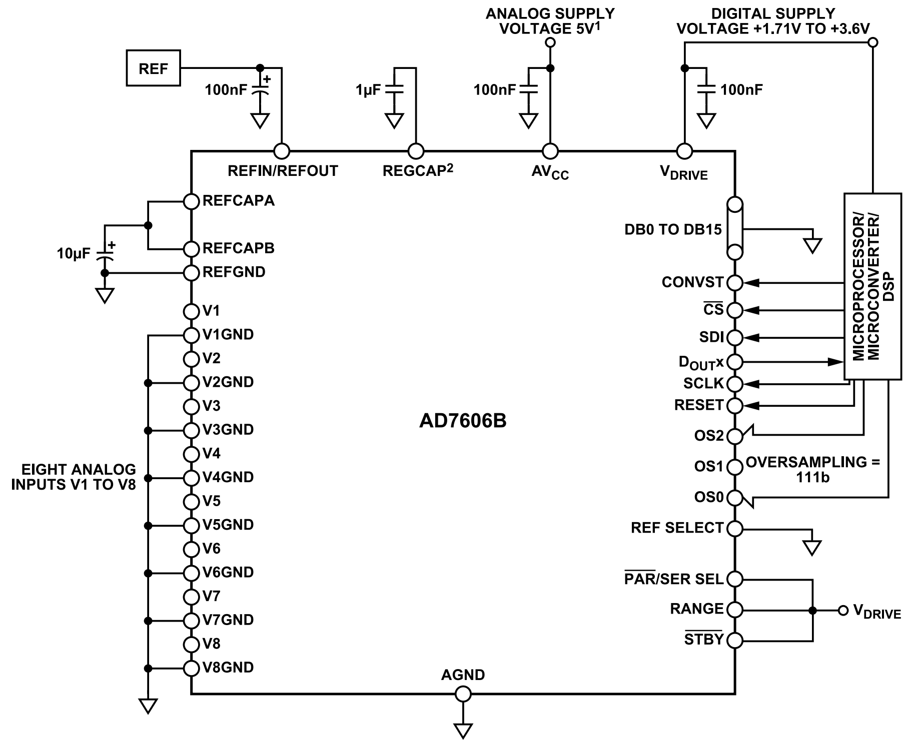


Figure 87. AD7606B Typical Connection Diagram, Hardware Mode

TYPICAL CONNECTION DIAGRAM



[1]DECOUPLING SHOWN ON THE AV_{CC} PIN APPLIES TO EACH AV_{CC} PIN (PIN 1, PIN 37, PIN 38, PIN 48).
DECOUPLING CAPACITOR CAN BE SHARED BETWEEN AV_{CC} PIN 37 AND PIN 38.
[2]DECOUPLING SHOWN ON THE REGCAP PIN APPLIES TO EACH REGCAP PIN (PIN 36, PIN 39).

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Figure 88. Typical Connection Diagram, Software Mode

APPLICATIONS INFORMATION

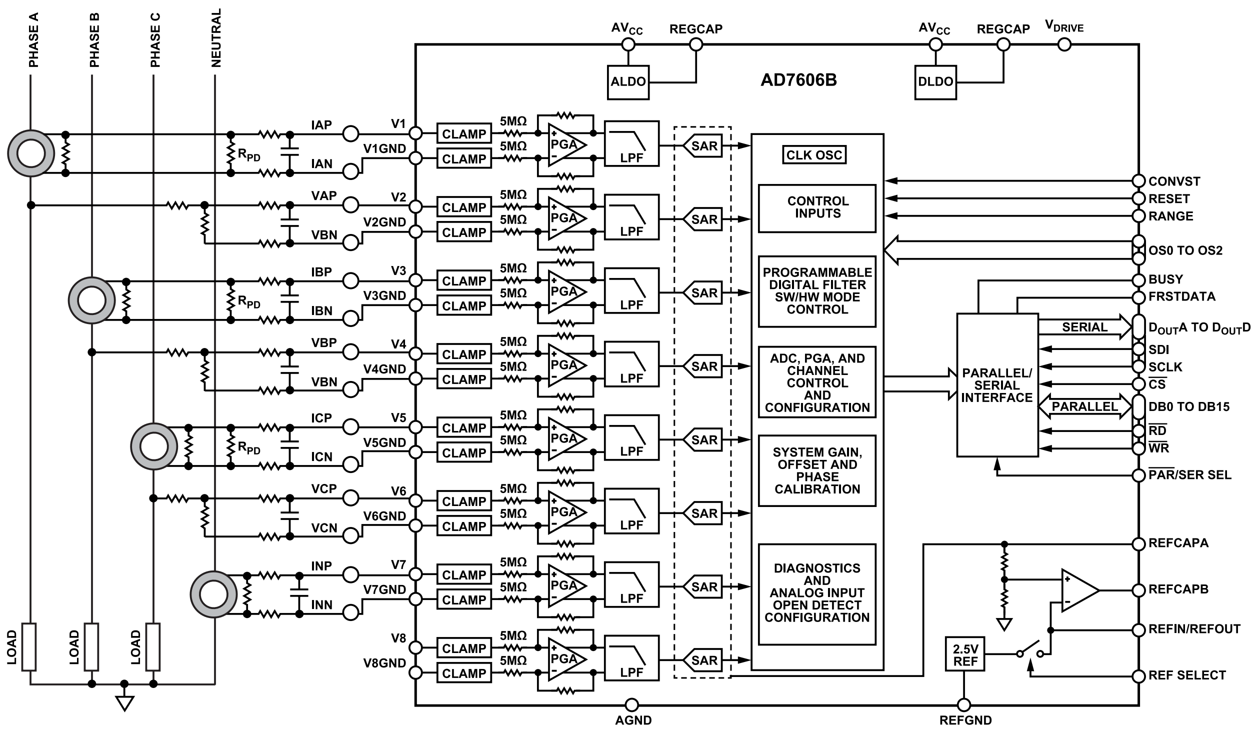
The fully integrated, 16-bit data acquisition system (DAS) of the AD7606B enables simultaneous, high precision measurement of up to eight analog channels without requiring additional active circuits.

The AD7606B is suitable for power monitoring applications. Measure the electrical variables accurately on a power line for information about the operating status of the grid. Monitor the voltage and current amplitude, frequency, and phase to detect anomalies and faults to prevent major disruptions on the electrical service and to enable power quality analysis, power factor calculation, and harmonic analysis (among other applications).

Each channel contains analog input clamp protection, a PGA, a low-pass filter, and a 16-bit SAR ADC. The analog input impedance of the AD7606B is typically 5 MΩ to allow a direct sensor interface to current transformers and power transformers, as shown in Figure 89, without requiring external ADC driver circuits and to accommodate ±10 V, ±5 V, or ±2.5 V.

Although transformers provide isolation from the power lines being monitored, place a series resistor in series to the analog input to prevent input currents beyond the absolute maximum ratings (see Table 6). On power line protection applications where overvoltages occur, the internal ±21 V clamp protects against damage and performance impacts on adjacent channels.

In case there are analog input channels beyond these limits, users are recommended to use external transient voltage suppressors (TVS) diodes.



NOTES
1. IxP AND IxN REPRESENT THE CURRENTS IN PHASE x, WHERE x = A, B, C, OR N. VxN/VxP REPRESENT THE VOLTAGES AT THESE TWO LINES. FOR EXAMPLE, IAP (POSITIVE PATH) AND IAN (NEGATIVE PATH) REPRESENT THE CURRENTS IN PHASE A.

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Figure 89. 8-Channel DAS for Power Line Monitoring

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

The following layout guidelines are recommended when designing the PCB that houses the AD7606B:

- If the AD7606B is in a system where multiple devices require analog-to-digital ground connections, use a solid ground plane (without splitting between analog and digital grounds).
- Make stable connections to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin. In the case of a split plane, join the digital and analog ground planes in only one place, preferably as close as possible to the AD7606B.
- Avoid running digital lines under the devices because doing so couples noise on the die. Allow the analog ground plane to run under the AD7606B to avoid noise coupling.
- Shield fast switching signals like CONVST or clocks with digital ground to avoid radiating noise to other sections of the board and ensure that they never run near analog signal paths.
- Avoid crossover of digital and analog signals.
- Ensure traces on layers in close proximity on the board run at right angles to each other to reduce the effect of feedthrough through the board.
- Ensure power supply lines to the AV_{CC} and V_{DRIVE} pins on the AD7606B. Use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Where possible, use supply planes and make stable connections between the AD7606B supply pins and the power tracks on the board. Use a single via or multiple vias for each supply pin.
- Place the decoupling capacitors close to (ideally, directly against) the supply pins and their corresponding ground pins. Place the decoupling capacitors for the REFIN/REFOUT pin and the REFCAPA pin and REFCAPB pin as close as possible to their respective AD7606B pins. Where possible, place the pins on the same side of the board as the AD7606B device.

Figure 90 shows the recommended decoupling on the top layer of the AD7606B board. Figure 91 shows the bottom layer decoupling, which is used for the four AV_{CC} pins and the V_{DRIVE} pin decoupling. Where the ceramic 100 nF caps for the AV_{CC} pins are placed close to their respective device pins, a single 100 nF capacitor can be shared between Pin 37 and Pin 38.

To ensure stable device-to-device performance matching in a system that contains multiple AD7606B devices, a symmetrical layout between the AD7606B devices is important.

Figure 92 shows a layout with two AD7606B devices. The AV_{CC} supply plane runs to the right of both devices, and the V_{DRIVE} supply track runs to the left of the two devices. The reference chip is positioned between the two devices, and the reference voltage track runs north to Pin 42 of U1 and south to Pin 42 of U2. A solid ground plane is used.

These symmetrical layout principles can also be applied to a system that contains more than two AD7606B devices. The AD7606B devices can be placed in a north to south direction, with the reference voltage located midway between the devices and the reference track running in the northsouth direction, similar to Figure 92.

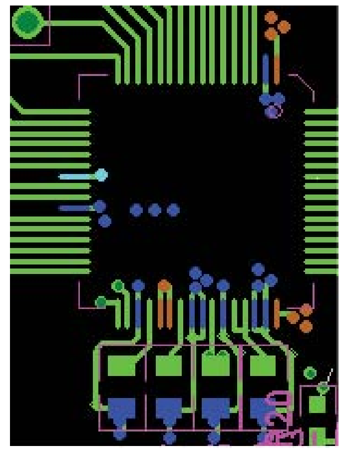

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Figure 90. Top Layer Decoupling REFIN/REFOUT, REFCAPA, REFCAPB, and REGCAP Pins

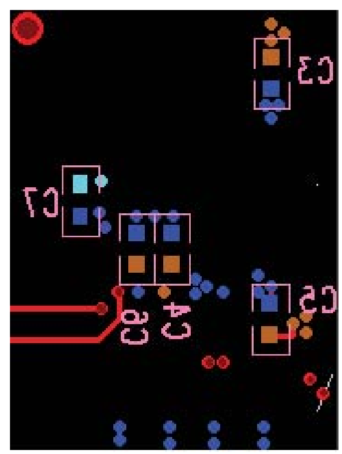

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Figure 91. Bottom Layer Decoupling

APPLICATIONS INFORMATION

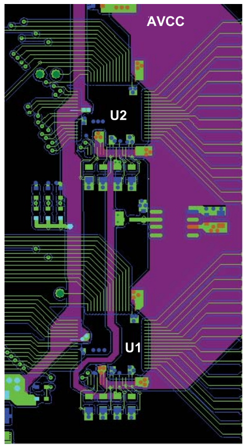


Figure 92. Layout for Multiple AD7606B Devices—Top Layer and Supply Plane Layer

REGISTER SUMMARY

Table 31. Register Summary

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	STATUS	RESET_ DETECT	DIGITAL_ ERROR	RESERVED	RESERVED					0x00	R
0x02	CONFIG	RESERVED	STATUS_ HEADER	EXT_OS_CLOCK	DOUT_FORMAT		RESERVED	OPERATION_MODE		0x08	R/W
0x03	RANGE_CH1_ CH2	CH2_RANGE				CH1_RANGE				0x33	R/W
0x04	RANGE_CH3_ CH4	CH4_RANGE				CH3_RANGE				0x33	R/W
0x05	RANGE_CH5_ CH6	CH6_RANGE				CH5_RANGE				0x33	R/W
0x06	RANGE_CH7_ CH8	CH8_RANGE				CH7_RANGE				0x33	R/W
0x08	OVERSAM PLING	OS_PAD				OS_RATIO				0x00	R/W
0x09	CH1_GAIN	RESERVED		CH1_GAIN						0x00	R/W
0x0A	CH2_GAIN	RESERVED		CH2_GAIN						0x00	R/W
0x0B	CH3_GAIN	RESERVED		CH3_GAIN						0x00	R/W
0x0C	CH4_GAIN	RESERVED		CH4_GAIN						0x00	R/W
0x0D	CH5_GAIN	RESERVED		CH5_GAIN						0x00	R/W
0x0E	CH6_GAIN	RESERVED		CH6_GAIN						0x00	R/W
0x0F	CH7_GAIN	RESERVED		CH7_GAIN						0x00	R/W
0x10	CH8_GAIN	RESERVED		CH8_GAIN						0x00	R/W
0x11	CH1_OFFSET	CH1_OFFSET								0x80	R/W
0x12	CH2_OFFSET	CH2_OFFSET								0x80	R/W
0x13	CH3_OFFSET	CH3_OFFSET								0x80	R/W
0x14	CH4_OFFSET	CH4_OFFSET								0x80	R/W
0x15	CH5_OFFSET	CH5_OFFSET								0x80	R/W
0x16	CH6_OFFSET	CH6_OFFSET								0x80	R/W
0x17	CH7_OFFSET	CH7_OFFSET								0x80	R/W
0x18	CH8_OFFSET	CH8_OFFSET								0x80	R/W
0x19	CH1_PHASE	CH1_PHASE_OFFSET								0x00	R/W
0x1A	CH2_PHASE	CH2_PHASE_OFFSET								0x00	R/W
0x1B	CH3_PHASE	CH3_PHASE_OFFSET								0x00	R/W
0x1C	CH4_PHASE	CH4_PHASE_OFFSET								0x00	R/W
0x1D	CH5_PHASE	CH5_PHASE_OFFSET								0x00	R/W
0x1E	CH6_PHASE	CH6_PHASE_OFFSET								0x00	R/W
0x1F	CH7_PHASE	CH7_PHASE_OFFSET								0x00	R/W
0x20	CH8_PHASE	CH8_PHASE_OFFSET								0x00	R/W
0x21	DIGITAL_DIAG _ENABLE	INTERFACE_ CHECK_EN	CLK_FS_OS_ COUNTER_EN	BUSY_STUCK_ HIGH_ERR_EN	SPI_READ_ ERR_EN	SPI_WRITE_ ERR_EN	INT_CRC_ ERR_EN	MM_CRC_ ERR_EN	ROM_ CRC_ ERR _EN	0x01	R/W
0x22	DIGITAL_DIAG _ERR	RESERVED		BUSY_STUCK_ HIGH_ERR	SPI_READ_ ERR	SPI_WRITE_ ERR	INT_CRC_ ERR	MM_CRC_ ERR	ROM_ CRC_ ERR	0x00	R/W
0x23	OPEN_ DETECT_ ENABLE	CH8_OPEN_ DETECT_EN	CH7_OPEN_ DETECT_EN	CH6_OPEN_ DETECT_EN	CH5_OPEN_ DETECT_EN	CH4_OPEN_ DETECT_EN	CH3_OPEN_ DETECT_EN	CH2_OPEN_ DETECT_EN	CH1_OP EN_DET ECT_EN	0x00	R/W

REGISTER SUMMARY

Table 31. Register Summary (Continued)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x24	OPEN_ DETECTED	CH8_OPEN	CH7_OPEN	CH6_OPEN	CH5_OPEN	CH4_OPEN	CH3_OPEN	CH2_OPEN	CH1_ OPEN	0x00	R/W
0x25	AIN_OV_UV_ DIAG_ENABLE	CH8_OV_ UV_EN	CH7_OV_ UV_EN	CH6_OV_ UV_EN	CH5_OV_ UV_EN	CH4_OV_ UV_EN	CH3_OV_ UV_EN	CH2_OV_ UV_EN	CH1_OV _ UV_EN	0x00	R/W
0x26	AIN_OV_DIAG _ERROR	CH8_OV_ ERR	CH7_OV_ ERR	CH6_OV_ ERR	CH5_OV_ ERR	CH4_OV_ ERR	CH3_OV_ ERR	CH2_OV_ ERR	CH1_ OV_ERR	0x00	R/W
0x27	AIN_UV_DIAG _ERROR	CH8_UV_ER R	CH7_UV_ERR	CH6_UV_ERR	CH5_UV_ER R	CH4_UV_ER R	CH3_UV_ER R	CH2_UV_ER R	CH1_ UV_ERR	0x00	R/W
0x28	DIAGNOSTIC_ MUX_CH1_2	RESERVED		CH2_DIAG_MUX_CTRL			CH1_DIAG_MUX_CTRL			0x00	R/W
0x29	DIAGNOSTIC_ MUX_CH3_4	RESERVED		CH4_DIAG_MUX_CTRL			CH3_DIAG_MUX_CTRL			0x00	R/W
0x2A	DIAGNOSTIC_ MUX_CH5_6	RESERVED		CH6_DIAG_MUX_CTRL			CH5_DIAG_MUX_CTRL			0x00	R/W
0x2B	DIAGNOSTIC_ MUX_CH7_8	RESERVED		CH8_DIAG_MUX_CTRL			CH7_DIAG_MUX_CTRL			0x00	R/W
0x2C	OPEN_ DETECT_ QUEUE	OPEN_DETECT_QUEUE								0x00	R/W
0x2D	FS_CLK_ COUNTER	CLK_FS_COUNTER								0x00	R
0x2E	OS_CLK_ COUNTER	CLK_OS_COUNTER								0x00	R
0x2F	ID	DEVICE_ID				SILICON_REVISION				0x15	R

REGISTER DETAILS

Address: 0x01, Reset: 0x00, Name: STATUS

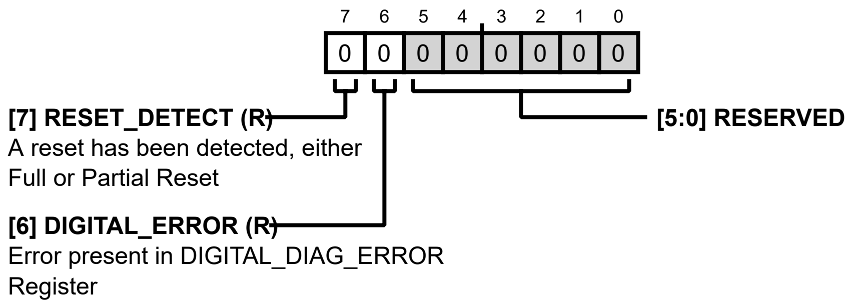


Table 32. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
7	RESET_DETECT	A reset has been detected, either full or partial reset.	0x0	R
6	DIGITAL_ERROR	Error present in DIGITAL_DIAG_ERROR register.	0x0	R
[5:0]	RESERVED	Reserved.	0x0	R

Address: 0x02, Reset: 0x08, Name: CONFIG

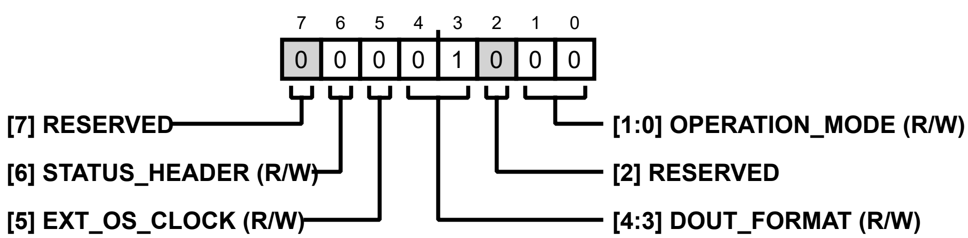


Table 33. Bit Descriptions for CONFIG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
6	STATUS_HEADER	Enable STATUS header to be appended to ADC data in both serial and parallel interface.	0x0	R/W
5	EXT_OS_CLOCK	In oversampling mode, enable external oversampling clock. Oversampling conversions are triggered through a clock signal applied to CONVST pin, instead of managed by the internal oversampling clock.	0x0	R/W
[4:3]	DOUT_FORMAT	Number of D_{OUT}x lines used in serial mode when reading conversions. 00: 1 D_{OUT}x. 01: 2 D_{OUT}x. 10: 4 D_{OUT}x. 11: 1 D_{OUT}x.	0x1	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	OPERATION_MODE	Operation mode. 00: normal mode. 01: standby mode. 10: autostandby mode. 11: shutdown mode.	0x0	R/W

Address: 0x03, Reset: 0x33, Name: RANGE_CH1_CH2

REGISTER DETAILS

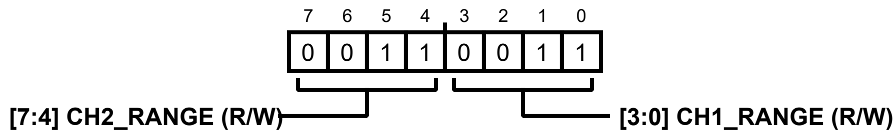
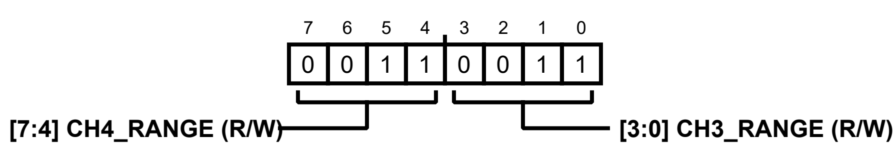


Table 34. Bit Descriptions for RANGE_CH1_CH2

Bits	Bit Name	Description	Reset	Access
[7:4]	CH2_RANGE	Range options for Channel 2. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range. 0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V single-ended range. 0111: ±10 V single-ended range. 1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.	0x3	R/W
[3:0]	CH1_RANGE	Range options for Channel 1. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range. 0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V single-ended range. 0111: ±10 V single-ended range. 1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.	0x3	R/W

Address: 0x04, Reset: 0x33, Name: RANGE_CH3_CH4



REGISTER DETAILS

Table 35. Bit Descriptions for RANGE_CH3_CH4

Bits	Bit Name	Description	Reset	Access
[7:4]	CH4_RANGE	Range options for Channel 4. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range. 0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V single-ended range. 0111: ±10 V single-ended range. 1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.	0x3	R/W
[3:0]	CH3_RANGE	Range options for Channel 3. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range. 0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V V single-ended range. 0111: ±10 V V single-ended range. 1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.	0x3	R/W

Address: 0x05, Reset: 0x33, Name: RANGE_CH5_CH6

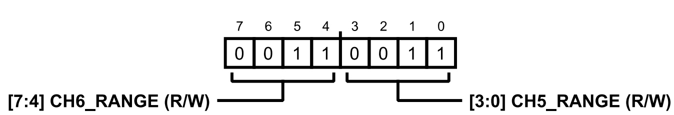


Table 36. Bit Descriptions for RANGE_CH5_CH6

Bits	Bit Name	Description	Reset	Access
[7:4]	CH6_RANGE	Range options for Channel 6. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range.	0x3	R/W

REGISTER DETAILS

Table 36. Bit Descriptions for RANGE_CH5_CH6 (Continued)

Bits	Bit Name	Description	Reset	Access
		0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V single-ended range. 0111: ±10 V single-ended range. 1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.		
[3:0]	CH5_RANGE	Range options for Channel 5. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range. 0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V V single-ended range. 0111: ±10 V V single-ended range. 1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.	0x3	R/W

Address: 0x06, Reset: 0x33, Name: RANGE_CH7_CH8

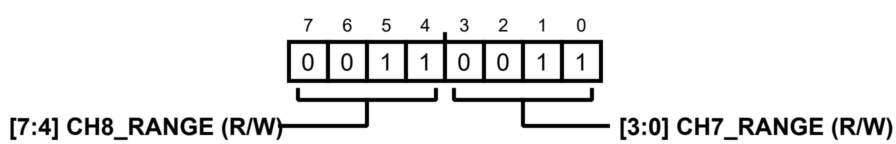


Table 37. Bit Descriptions for RANGE_CH7_CH8

Bits	Bit Name	Description	Reset	Access
[7:4]	CH8_RANGE	Range options for Channel 8. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range. 0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V single-ended range. 0111: ±10 V single-ended range.	0x3	R/W

REGISTER DETAILS

Table 37. Bit Descriptions for RANGE_CH7_CH8 (Continued)

Bits	Bit Name	Description	Reset	Access
		1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.		
[3:0]	CH7_RANGE	Range options for Channel 7. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±10 V single-ended range. 0011: ±10 V single-ended range. 0100: ±10 V single-ended range. 0101: ±10 V single-ended range. 0110: ±10 V single-ended range. 0111: ±10 V single-ended range. 1000: ±10 V single-ended range. 1001: ±10 V single-ended range. 1010: ±10 V single-ended range. 1011: ±10 V single-ended range. 1100: reserved. 1101: reserved. 1110: reserved. 1111: reserved.	0x3	R/W

Address: 0x08, Reset: 0x00, Name: OVERSAMPLING

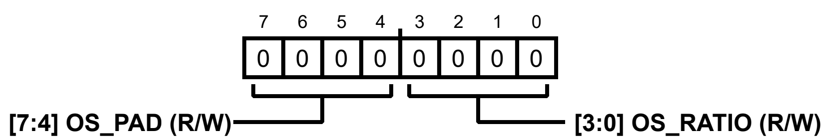


Table 38. Bit Descriptions for OVERSAMPLING

Bits	Bit Name	Description	Reset	Access
[7:4]	OS_PAD	Oversampling padding, extend the internal oversampling period allowing evenly spaced sampling between CONVST rising edges.	0x0	R/W
[3:0]	OS_RATIO	Oversampling ratio. 0: no oversampling. 1: oversampling by 2. 10: oversampling by 4. 11: oversampling by 8. 100: oversampling by 16. 101: oversampling by 32. 110: oversampling by 64. 111: oversampling by 128. 1000: oversampling by 256.	0x0	R/W

REGISTER DETAILS

Table 38. Bit Descriptions for OVERSAMPLING (Continued)

Bits	Bit Name	Description	Reset	Access
		1001: oversampling off. 1010: oversampling off. 1011: oversampling off. 1100: oversampling off. 1101: oversampling off. 1110: oversampling off. 1111: oversampling off.		

Address: 0x09, Reset: 0x00, Name: CH1_GAIN

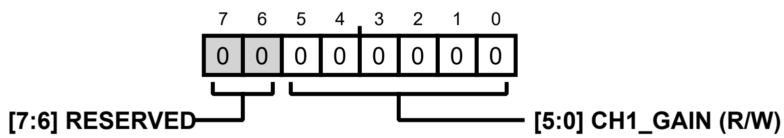


Table 39. Bit Descriptions for CH1_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH1_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0A, Reset: 0x00, Name: CH2_GAIN

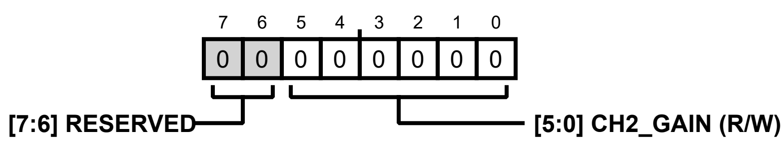


Table 40. Bit Descriptions for CH2_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH2_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0B, Reset: 0x00, Name: CH3_GAIN

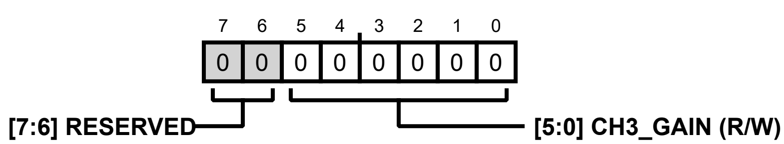


Table 41. Bit Descriptions for CH3_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH3_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0C, Reset: 0x00, Name: CH4_GAIN

REGISTER DETAILS

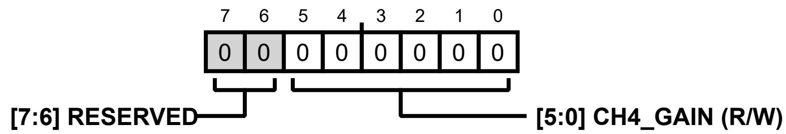


Table 42. Bit Descriptions for CH4_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH4_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0D, Reset: 0x00, Name: CH5_GAIN

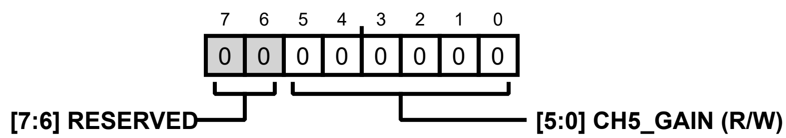


Table 43. Bit Descriptions for CH5_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH5_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0E, Reset: 0x00, Name: CH6_GAIN

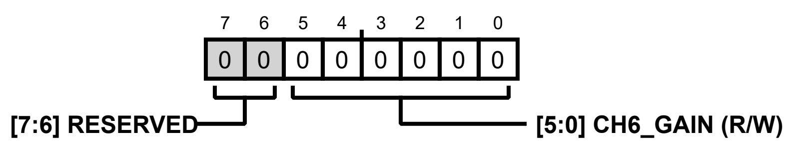


Table 44. Bit Descriptions for CH6_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH6_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0F, Reset: 0x00, Name: CH7_GAIN

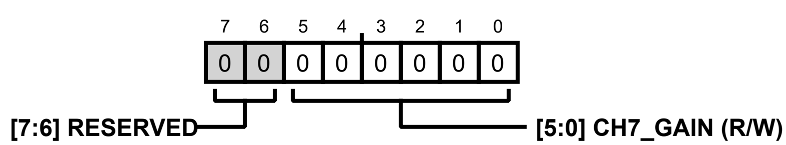


Table 45. Bit Descriptions for CH7_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH7_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

REGISTER DETAILS

Address: 0x10, Reset: 0x00, Name: CH8_GAIN

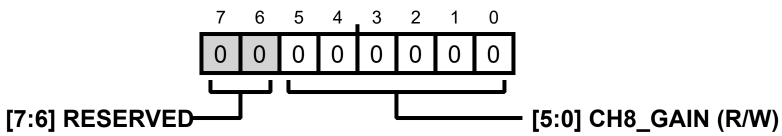


Table 46. Bit Descriptions for CH8_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH8_GAIN	R_{FILTER} calibration register. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x11, Reset: 0x80, Name: CH1_OFFSET

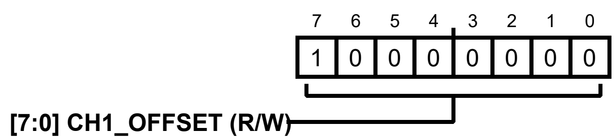


Table 47. Bit Descriptions for CH1_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB.	0x80	R/W

Address: 0x12, Reset: 0x80, Name: CH2_OFFSET

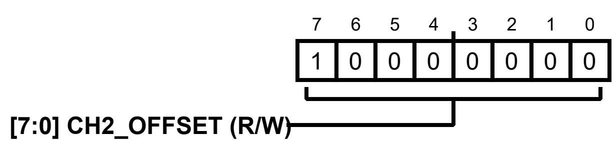


Table 48. Bit Descriptions for CH2_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH2_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB	0x80	R/W

Address: 0x13, Reset: 0x80, Name: CH3_OFFSET

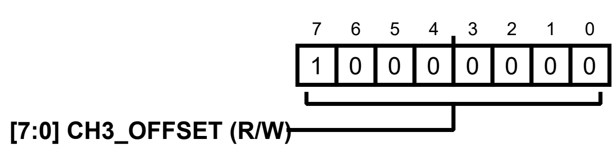


Table 49. Bit Descriptions for CH3_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH3_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB	0x80	R/W

Address: 0x14, Reset: 0x80, Name: CH4_OFFSET

REGISTER DETAILS

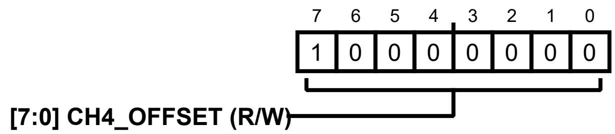


Table 50. Bit Descriptions for CH4_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH4_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB	0x80	R/W

Address: 0x15, Reset: 0x80, Name: CH5_OFFSET

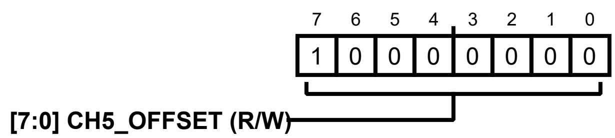


Table 51. Bit Descriptions for CH5_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH5_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB	0x80	R/W

Address: 0x16, Reset: 0x80, Name: CH6_OFFSET

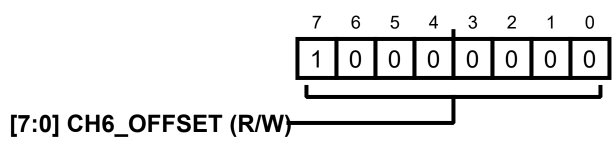


Table 52. Bit Descriptions for CH6_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH6_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB	0x80	R/W

Address: 0x17, Reset: 0x80, Name: CH7_OFFSET

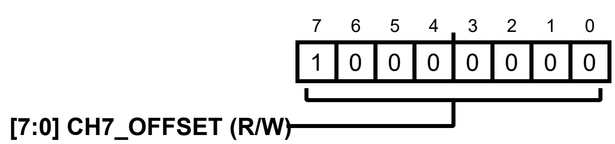


Table 53. Bit Descriptions for CH7_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH7_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB	0x80	R/W

Address: 0x18, Reset: 0x80, Name: CH8_OFFSET

REGISTER DETAILS

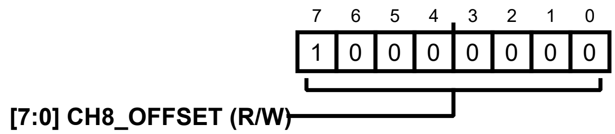


Table 54. Bit Descriptions for CH8_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH8_OFFSET	Offset register to remove external system offset errors. Range from −128 LSB to +127 LSB	0x80	R/W

Address: 0x19, Reset: 0x00, Name: CH1_PHASE

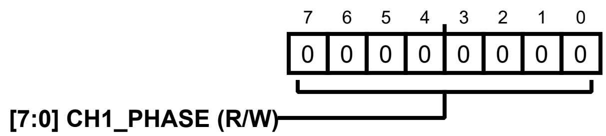


Table 55. Bit Descriptions for CH1_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_PHASE_OFFSET	Phase delay from 0 µs to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1A, Reset: 0x00, Name: CH2_PHASE

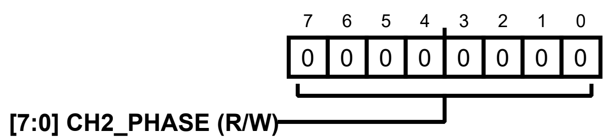


Table 56. Bit Descriptions for CH2_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH2_PHASE_OFFSET	Phase delay from 0 µs to 318.75 µs in steps of 1.25 µs.	0x0	R/W

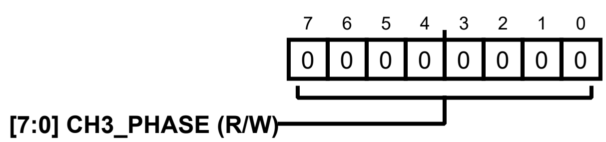


Table 57. Bit Descriptions for CH3_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH3_PHASE_OFFSET	Phase delay from 0 µs to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x1C, Reset: 0x00, Name: CH4_PHASE

REGISTER DETAILS

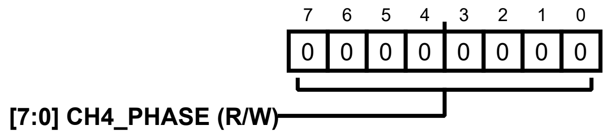


Table 58. Bit Descriptions for CH4_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH4_PHASE_OFFSET	Phase delay from 0 μs to 318.75 μs in steps of 1.25 μs.	0x0	R/W

Address: 0x1D, Reset: 0x00, Name: CH5_PHASE

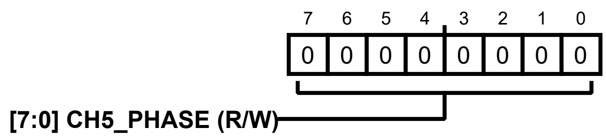


Table 59. Bit Descriptions for CH5_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH5_PHASE_OFFSET	Phase delay from 0 μs to 318.75 μs in steps of 1.25 μs.	0x0	R/W

Address: 0x1E, Reset: 0x00, Name: CH6_PHASE

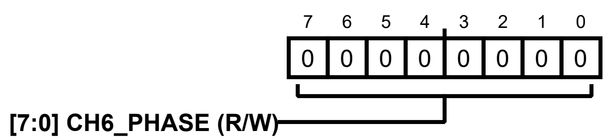


Table 60. Bit Descriptions for CH6_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH6_PHASE_OFFSET	Phase delay from 0 μs to 318.75 μs in steps of 1.25 μs.	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: CH7_PHASE

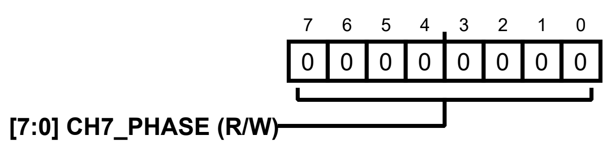


Table 61. Bit Descriptions for CH7_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH7_PHASE_OFFSET	Phase delay from 0 μs to 318.75 μs in steps of 1.25 μs.	0x0	R/W

Address: 0x20, Reset: 0x00, Name: CH8_PHASE

REGISTER DETAILS

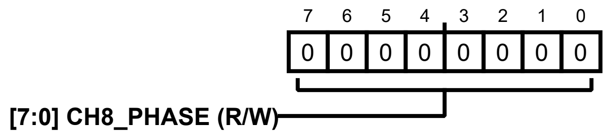


Table 62. Bit Descriptions for CH8_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH8_PHASE_OFFSET	Phase delay from 0 µs to 318.75 µs in steps of 1.25 µs.	0x0	R/W

Address: 0x21, Reset: 0x01, Name: DIGITAL_DIAG_ENABLE

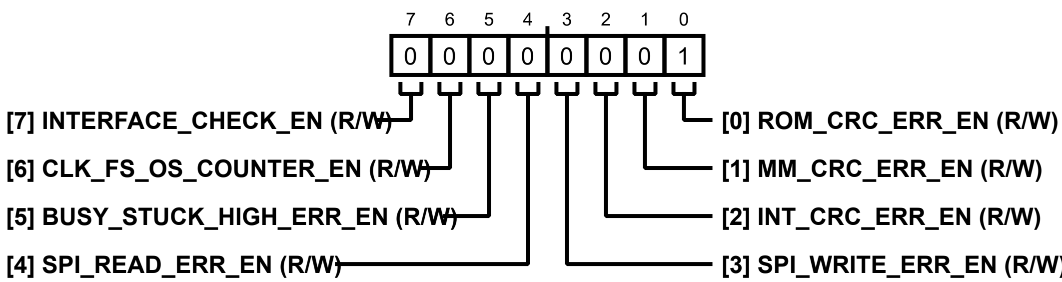


Table 63. Bit Descriptions for DIGITAL_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
7	INTERFACE_CHECK_EN	Enable interface check. Provides a fixed data on each channel when reading ADC data.	0x0	R/W
6	CLK_FS_OS_COUNTER_EN	Enable FS and OS clock counter.	0x0	R/W
5	BUSY_STUCK_HIGH_ERR_EN	Enable busy stuck high check.	0x0	R/W
4	SPI_READ_ERR_EN	Enable checking if attempting to read from an invalid address.	0x0	R/W
3	SPI_WRITE_ERR_EN	Enable checking if attempting to write to an invalid address.	0x0	R/W
2	INT_CRC_ERR_EN	Enable interface CRC check.	0x0	R/W
1	MM_CRC_ERR_EN	Enable memory map CRC check.	0x0	R/W
0	ROM_CRC_ERR_EN	Enable ROM CRC check.	0x1	R/W

Address: 0x22, Reset: 0x00, Name: DIGITAL_DIAG_ERR

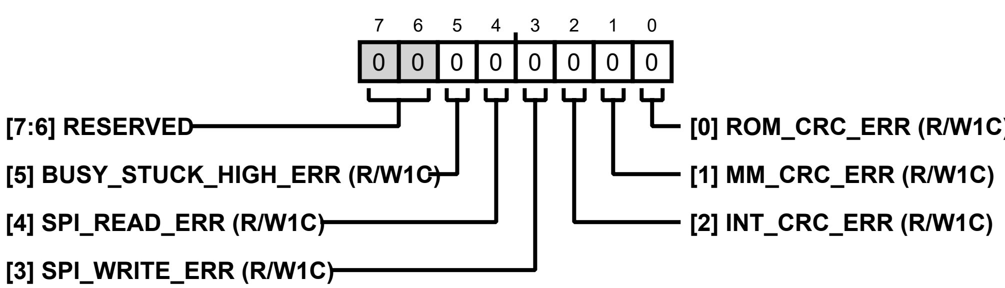


Table 64. Bit Descriptions for DIGITAL_DIAG_ERR

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	BUSY_STUCK_HIGH_ERR	Busy stuck high error. Busy line has been at high logic level for longer than 4 µs.	0x0	R/W1C

REGISTER DETAILS

Table 64. Bit Descriptions for DIGITAL_DIAG_ERR (Continued)

Bits	Bit Name	Description	Reset	Access
4	SPI_READ_ERR	SPI invalid read address.	0x0	R/W1C
3	SPI_WRITE_ERR	SPI invalid write address.	0x0	R/W1C
2	INT_CRC_ERR	Interface CRC error.	0x0	R/W1C
1	MM_CRC_ERR	Memory map CRC error.	0x0	R/W1C
0	ROM_CRC_ERR	ROM CRC error.	0x0	R/W1C

Address: 0x23, Reset: 0x00, Name: OPEN_DETECT_ENABLE

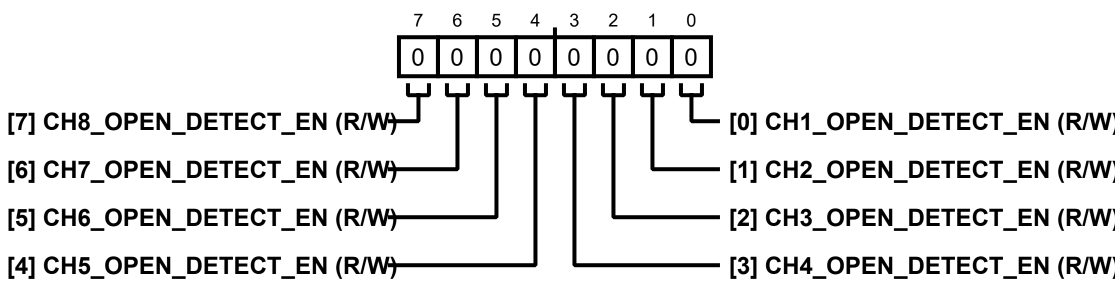
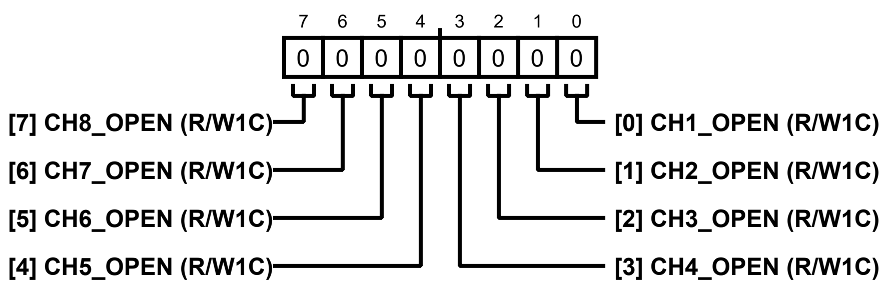


Table 65. Bit Descriptions for OPEN_DETECT_ENABLE

Bits	Bit Name	Description	Reset	Access
7	CH8_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 8. In manual mode, sets the PGA common mode to high.	0x0	R/W
6	CH7_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 7. In manual mode, sets the PGA common mode to high.	0x0	R/W
5	CH6_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 6. In manual mode, sets the PGA common mode to high.	0x0	R/W
4	CH5_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 5. In manual mode, sets the PGA common mode to high.	0x0	R/W
3	CH4_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 4. In manual mode, sets the PGA common mode to high.	0x0	R/W
2	CH3_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 3. In manual mode, sets the PGA common mode to high.	0x0	R/W
1	CH2_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 2. In manual mode, sets the PGA common mode to high.	0x0	R/W
0	CH1_OPEN_DETECT_EN	In automatic mode, enables analog input open detection for Channel 1. In manual mode, sets the PGA common mode to high.	0x0	R/W

Address: 0x24, Reset: 0x00, Name: OPEN_DETECTED



REGISTER DETAILS

Table 66. Bit Descriptions for OPEN_DETECTED

Bits	Bit Name	Description	Reset	Access
7	CH8_OPEN	Analog Input 8 open detected.	0x0	R/W1C
6	CH7_OPEN	Analog Input 7 open detected.	0x0	R/W1C
5	CH6_OPEN	Analog Input 6 open detected.	0x0	R/W1C
4	CH5_OPEN	Analog Input 5 open detected.	0x0	R/W1C
3	CH4_OPEN	Analog Input 4 open detected.	0x0	R/W1C
2	CH3_OPEN	Analog Input 3 open detected.	0x0	R/W1C
1	CH2_OPEN	Analog Input 2 open detected.	0x0	R/W1C
0	CH1_OPEN	Analog Input 1 open detected.	0x0	R/W1C

Address: 0x25, Reset: 0x00, Name: AIN_OV_UV_DIAG_ENABLE

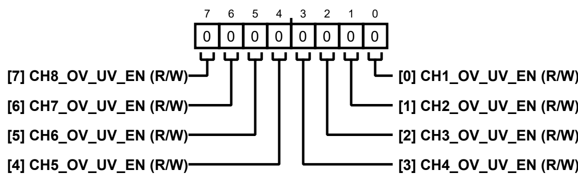


Table 67. Bit Descriptions for AIN_OV_UV_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
7	CH8_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 8.	0x0	R/W
6	CH7_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 7.	0x0	R/W
5	CH6_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 6.	0x0	R/W
4	CH5_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 5.	0x0	R/W
3	CH4_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 4.	0x0	R/W
2	CH3_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 3.	0x0	R/W
1	CH2_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 2.	0x0	R/W
0	CH1_OV_UV_EN	Enable overvoltage/undervoltage error check on Channel 1.	0x0	R/W

Address: 0x26, Reset: 0x00, Name: AIN_OV_DIAG_ERROR

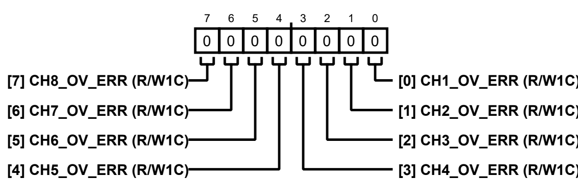


Table 68. Bit Descriptions for AIN_OV_DIAG_ERROR

Bits	Bit Name	Description	Reset	Access
7	CH8_OV_ERR	Overvoltage error on Channel 8.	0x0	R/W1C
6	CH7_OV_ERR	Overvoltage error on Channel 7.	0x0	R/W1C
5	CH6_OV_ERR	Overvoltage error on Channel 6.	0x0	R/W1C
4	CH5_OV_ERR	Overvoltage error on Channel 5.	0x0	R/W1C
3	CH4_OV_ERR	Overvoltage error on Channel 4.	0x0	R/W1C
2	CH3_OV_ERR	Overvoltage error on Channel 3.	0x0	R/W1C
1	CH2_OV_ERR	Overvoltage error on Channel 2.	0x0	R/W1C
0	CH1_OV_ERR	Overvoltage error on Channel 1.	0x0	R/W1C

REGISTER DETAILS

Address: 0x27, Reset: 0x00, Name: AIN_UV_DIAG_ERROR

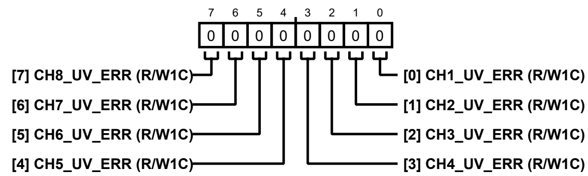


Table 69. Bit Descriptions for AIN_UV_DIAG_ERROR

Bits	Bit Name	Description	Reset	Access
7	CH8_UV_ERR	Undervoltage error on Channel 8.	0x0	R/W1C
6	CH7_UV_ERR	Undervoltage error on Channel 7.	0x0	R/W1C
5	CH6_UV_ERR	Undervoltage error on Channel 6.	0x0	R/W1C
4	CH5_UV_ERR	Undervoltage error on Channel 5.	0x0	R/W1C
3	CH4_UV_ERR	Undervoltage error on Channel 4.	0x0	R/W1C
2	CH3_UV_ERR	Undervoltage error on Channel 3.	0x0	R/W1C
1	CH2_UV_ERR	Undervoltage error on Channel 2.	0x0	R/W1C
0	CH1_UV_ERR	Undervoltage error on Channel 1.	0x0	R/W1C

Address: 0x28, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH1_2

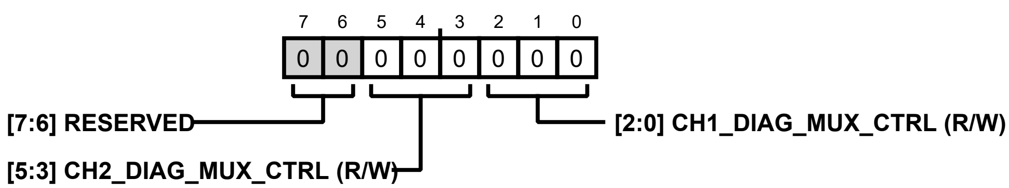


Table 70. Bit Descriptions for DIAGNOSTIC_MUX_CH1_2

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH2_DIAG_MUX_CTRL	Channel 2 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: ALDO 1.8 V × 4. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W
[2:0]	CH1_DIAG_MUX_CTRL	Channel 1 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: DLDO 1.8 V × 4. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

REGISTER DETAILS

Address: 0x29, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH3_4

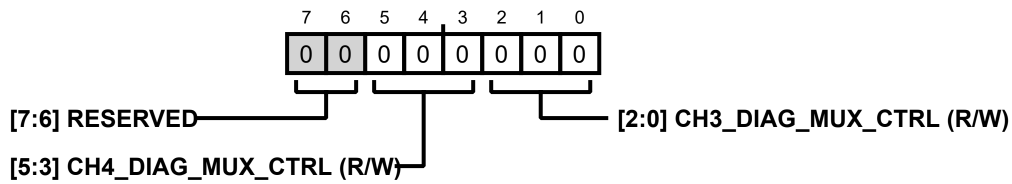


Table 71. Bit Descriptions for DIAGNOSTIC_MUX_CH3_4

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH4_DIAG_MUX_CTRL	Channel 4 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: ALDO 1.8 V × 4. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W
[2:0]	CH3_DIAG_MUX_CTRL	Channel 3 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: DLDO 1.8 V × 4. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

Address: 0x2A, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH5_6

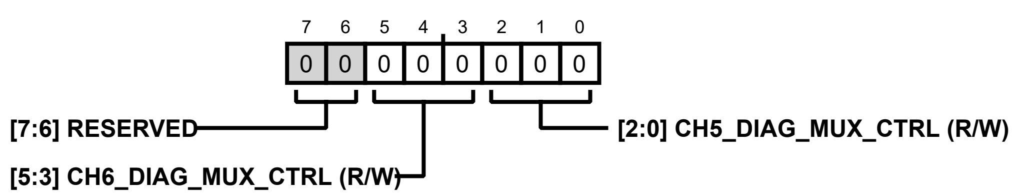


Table 72. Bit Descriptions for DIAGNOSTIC_MUX_CH5_6

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH6_DIAG_MUX_CTRL	Channel 6 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: ALDO 1.8 V × 4. 101: V_{DRIVE}.	0x0	R/W

REGISTER DETAILS

Table 72. Bit Descriptions for DIAGNOSTIC_MUX_CH5_6 (Continued)

Bits	Bit Name	Description	Reset	Access
		110: AGND. 111: AV_{CC}.		
[2:0]	CH5_DIAG_MUX_CTRL	Channel 5 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: DLDO 1.8 V × 4. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

Address: 0x2B, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH7_8

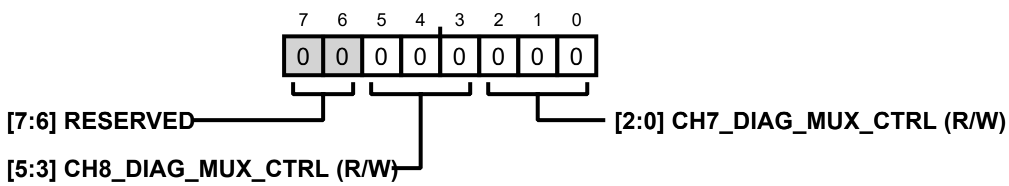


Table 73. Bit Descriptions for DIAGNOSTIC_MUX_CH7_8

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH8_DIAG_MUX_CTRL	Channel 8 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: ALDO 1.8 V × 4. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W
[2:0]	CH7_DIAG_MUX_CTRL	Channel 7 diagnostic mux control. Select ±10 V range. 000: Analog input pin. 001: Die temperature. 010: 2.5 V Reference × 4. 011: ALDO 1.8 V × 4. 100: DLDO 1.8 V × 4. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

Address: 0x2C, Reset: 0x00, Name: OPEN_DETECT_QUEUE

REGISTER DETAILS

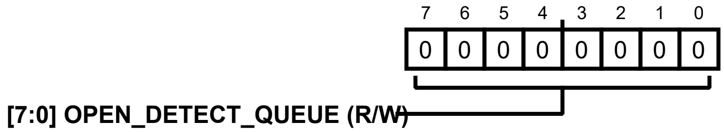


Table 74. Bit Descriptions for OPEN_DETECT_QUEUE

Bits	Bit Name	Description	Reset	Access
[7:0]	OPEN_DETECT_QUEUE	Open Detect Queue. When set to 1, open detect is configured in manual mode. When set to >1, open detect operates in automatic mode and the value set in this register specifies the number of conversions when there is no change in output code before the PGA common mode is switched.	0x0	R/W

Address: 0x2D, Reset: 0x00, Name: FS_CLK_COUNTER

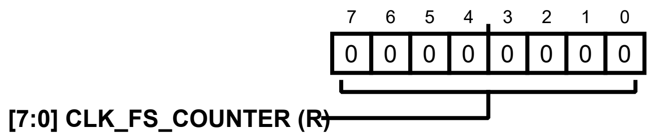


Table 75. Bit Descriptions for FS_CLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	CLK_FS_COUNTER	A counter that is incremented at a frequency of 16 Meg/64. Reading this register verifies the operation and frequency of the FS_CLOCK.	0x0	R

Address: 0x2E, Reset: 0x00, Name: OS_CLK_COUNTER

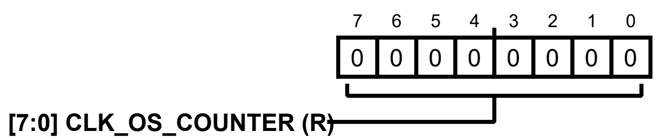


Table 76. Bit Descriptions for OS_CLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	CLK_OS_COUNTER	A counter that is incremented at a frequency of 12.5 Meg/64. Reading this register verifies the operation and frequency of the oversampling clock.	0x0	R

Address: 0x2F, Reset: 0x15, Name: ID

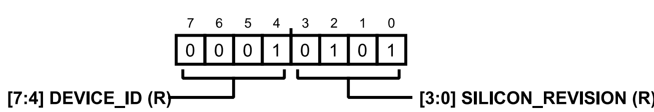


Table 77. Bit Descriptions for ID

Bits	Bit Name	Description	Reset	Access
[7:4]	DEVICE_ID	Generic. 0000: reserved. 0001: AD7606B generic.	0x1	R
[3:0]	SILICON_REVISION	Silicon revision.	0x5	R

OUTLINE DIMENSIONS

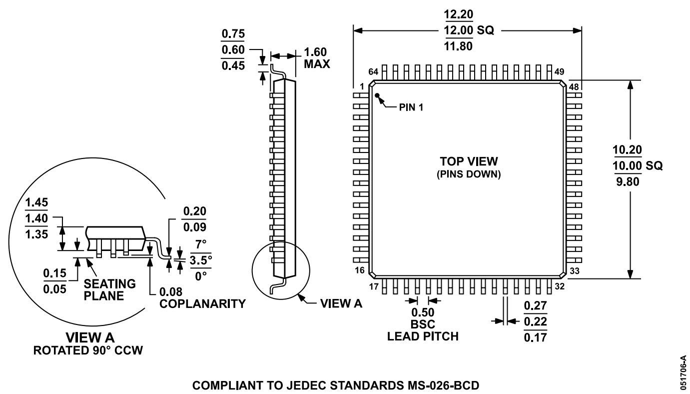


Figure 93. 64-Lead Low Profile Quad Flat Package [LQFP] (ST-64-2) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7606BBSTZ	−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606BBSTZ-RL	−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2

1 Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD7606C16FMCZ	Evaluation Board for the AD7606B
EVAL-SDP-CH1Z	Evaluation Controller Board

1 Z = RoHS Compliant Part.