ANALOG DEVICES

Data Sheet

AD9088

Apollo MxFE Octal, 16-Bit, 16GSPS RF DAC and Octal, 12-Bit, 8GSPS RF ADC

FEATURES

- Reconfigurable mixed signal platform design
- eight 16-bit RF DACs and eight 12-bit RF ADCs (8T8R)
- Usable RF analog bandwidth up to 16GHz
- Fast detect with low latency for fast AGC
- Spectrum sniffer and monitor
- Signal monitor for slow AGC
- Multiple loopback (ADC to DAC)
- Power amplifier downstream protection circuitry
- Maximum DAC/ADC sample rate up to 16GSPS/8GSPS
- Versatile digital features
- Maximum instantaneous bandwidth of 3.2GHz per channel (6T6R) or 2.7GHz per channel (8T8R)
- Programmable FIR filters at full ADC and DAC sample rates
- Configurable fine and coarse DDCs and DUCs
- Fast frequency hopping with profiles
- Dynamic configuration through SPI, HSCI, GPIO, or external trigger (TRIG)
- JESD204B and JESD204C: 20Gbps and 28.21Gbps
- On-chip temperature monitoring unit
- Package: 24mm × 26mm, 899-ball BGA_ED with 0.80mm pitch

APPLICATIONS

- Radar and phased-array systems
- Seeker front end
- Tactical defense radio infrastructure
- Electronic warfare and signal intelligence
- Wireless communications infrastructure
- Wireless communications test (5G mmWave, 5G C band, back-haul)

GENERAL DESCRIPTION

The mixed signal front-end (Apollo MxFE) is a highly integrated device with a 16-bit, 16GSPS maximum sample rate, RF digital-to-analog converter (DAC) core, and 12-bit, 8GSPS maximum sample rate, RF analog-to-digital converter (ADC) core. The AD9088 supports eight transmitter channels and eight receiver channels. The AD9088 is well suited for applications requiring both wideband ADCs and DACs to process signal(s) having wide instantaneous bandwidth. The device features a 48 lane, 28.21Gbps JESD204C or 20Gbps JESD204B data transceiver port, an on-chip clock multiplier, and a digital signal processing (DSP) capability targeted at either wideband or multiband, direct to RF applications. The AD9088 also features a bypass mode that allows the full bandwidth capability of the ADC and/or DAC cores to bypass the DSP datapaths. The device also features low latency loopback and frequency hopping modes targeted at phased-array radar systems and electronic warfare applications.

The AD9088 is available in a 24mm × 26mm, 899-ball BGA_ED and can operate over a junction temperature range of −40°C to +110°C.

Table 1. Product Listing with Distinguishing Transmitter and Receiver Features

	Transmitter (Tx)				Receiver (Rx)				
Model	DAC Channel	Maximum DAC Rate (GSPS)	Analog BW[1] (GHz)	Maximum Tx iBW[2] (GHz)	ADC Channel	Maximum ADC Rate (GSPS)	Analog BW[3] (GHz)	Maximum Rx iBW[2] (GHz)	Input Network
AD9088	8	16	16	8	8	8	16	4	Single-Ended

1 The analog bandwidth is the allowed frequency range supported by the DAC output port.

2 The maximum instantaneous bandwidth (iBW) is the maximum instantaneous bandwidth with all digital downconversions (DDCs) and digital upconversions (DUCs) bypassed.

3 The analog bandwidth is the allowed frequency range supported by the ADC input port.

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.935.5565 |

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REVISION HISTORY

2/2026—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

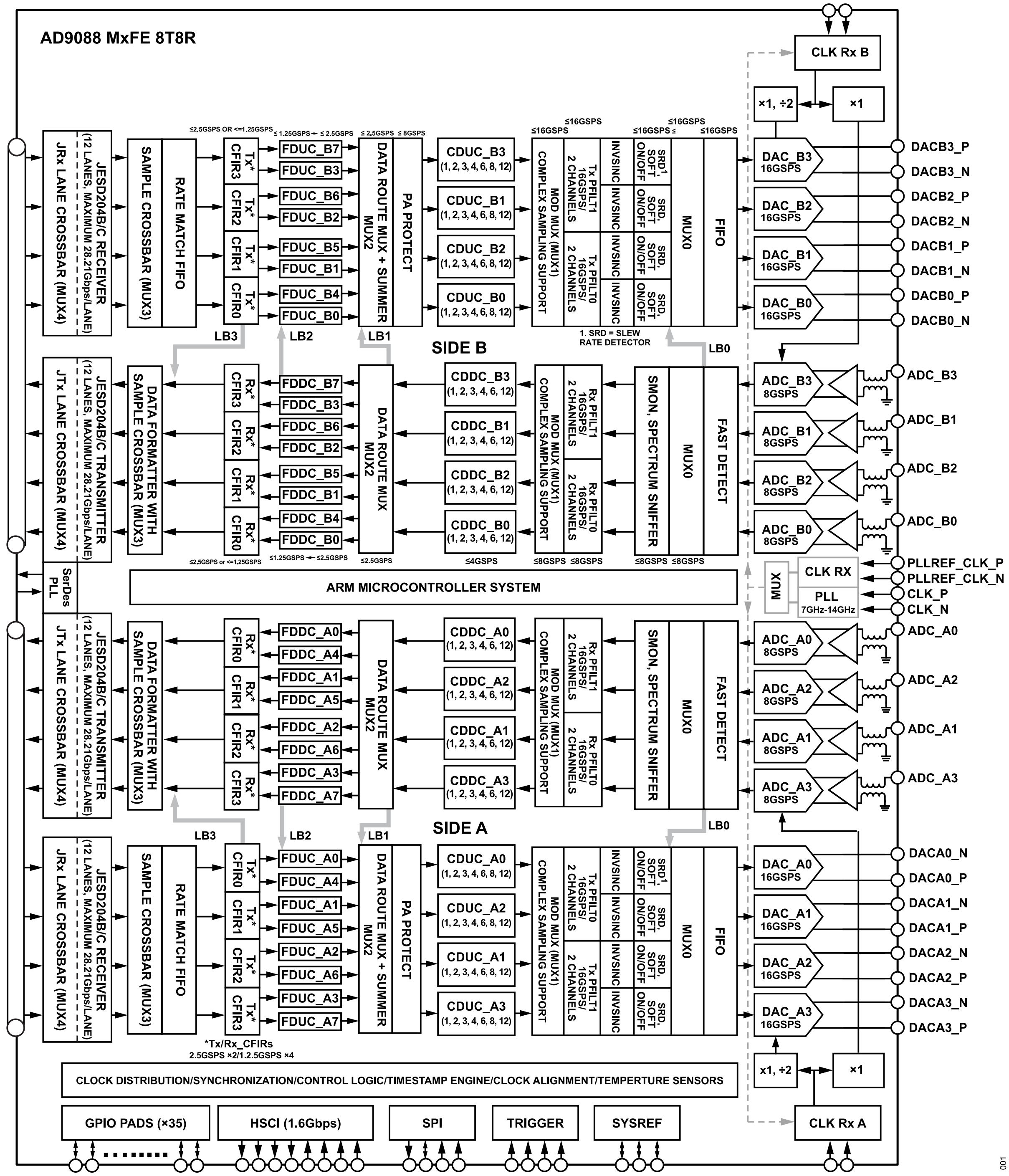

Figure 1. 8T8R, Single-Ended ADC

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RECOMMENDED OPERATING CONDITIONS

Refer to UG-2300 Device User Guide for more information on device initialization.

Table 2. Recommended Operating Conditions

	Functional (Transient)[1]			Performance (Static)[2]			
Parameters	Min	Typ	Max	Min	Typ	Max	Unit
OPERATING JUNCTION TEMPERATURE[3]	−40		+110	−10		+110	°C
ANALOG DOMAIN							
AVDD1P8_DAC_A and AVDD1P8_DAC_B	1.755	1.8	1.845	1.755	1.8	1.845	V
AVDD1P8, AVDD1P8_MCS, and AVDD1P8_PLL	1.755	1.8	1.845	1.755	1.8	1.845	V
AVDD1P0_DAC_DIG_B and AVDD1P0_DAC_DIG_A	0.95	1	1.05	0.975	1	1.025	V
AVDD1P8_ADC_A and AVDD1P8_ADC_B	1.755	1.8	1.845	1.755	1.8	1.845	V
AVDD1P0_ADC_A and AVDD1P0_ADC_B	1		1.05	1.025	1.04	1.05	V
AVDD1P0_MCS, AVDD1P0_CK, and AVDD1P0_PLL_SYN	1		1.05	1.025	1.04	1.05	V
AVDD1P0_ADC_SCLK_A and AVDD1P0_ADC_SCLK_B	1		1.05	1.025	1.04	1.05	V
ANEG1P0_ADC_A, ANEG1P0_ADC_B, ANEG1P0_DAC_A, and ANEG1P0_DAC_B	−0.975	−1	−1.025	−0.975	−1	−1.025	V
AVDD1P0_DAC_A and AVDD1P0_DAC_B	0.95	1	1.05	0.975	1	1.025	V
AVDD1P0_ADCBK_A and AVDD1P0_ADCBK_B	1		1.05	1.025	1.04	1.05	V
DIGITAL DOMAIN POWER							
DVDD1P8	1.71	1.8	1.89	1.71	1.8	1.89	V
DVDD1P0	0.95	1	1.05	0.95	1	1.05	V
DVDD0P8_ADC	0.76	0.8	0.84	0.76	0.8	0.84	V
DVDD0P8	0.76	0.8	0.84	0.76	0.8	0.84	V
SERDES (JESD204B/JESD204C) DOMAIN POWER							
SVDD1P0_TX	0.95	1	1.05	0.975	1	1.025	V
SVDD1P0_RX	0.95	1	1.05	0.975	1	1.025	V
SVDD1P0_PLL and SVDD1P0_PLL_SYN	0.95	1	1.05	0.975	1	1.025	V
SVDD1P8_PLL	1.71	1.8	1.89	1.71	1.8	1.89	V

1 Functional means that the converter remains operational;however, it will not perform at data sheet levels of performance, which may occur because there was a transient on the supply that pulled the supply outside the performance voltage range. Digital datapaths continue to operate as if there is no supply glitch; latency, functionality, and timing are preserved.

2 Performance is a range of voltages that the DAC, ADC, or serialization/deserialization (SERDES) is expected to operate to the full data sheet performance specifications. The data converter must meet specifications with the supply held at a DC value of between the minimum and maximum.

3 Functionality is guaranteed from a T_J of –40°C to +110°C. Performance is guaranteed from a T_J of –10°C to +110°C.

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POWER CONSUMPTION

Typical at nominal supplies. In Table 3, for all minimum and maximum values T_J = −10°C to +110°C, and for all typical values, T_J = 65°C, unless otherwise noted.

Power dissipation varies greatly with device settings, such as the ADC and DAC sample rates, the number of active datapaths (number of virtual converters), interpolation and decimation rates, and the JESD204B and JESD204C operating parameters, such as the lane rate of each lane and the total number of lanes. The power consumption data in Table 4 is measured based on the use cases specified in Table 3.

Table 3. AD9088BBPZ-MX-SE-SW5 Configuration Profile

Parameter	Value	Unit
SAMPLE RATE		
ADC	8	GSPS
DAC	16	GSPS
NUMBER OF ADC AND DAC CHANNELS	8	
TOTAL DECIMATION	8	
TOTAL INTERPOLATION	16	
DATA RATE		
ADC	1	GSPS
DAC	1	GSPS
SERDES SETUP (JTx AND JRx)		
Number of Lanes (L)	8	
Number of Virtual Converters (M)	8	
Lane Rate	16.5	Gbps

See the UG-2300 Device User Guide for further information on the JESD204B and JESD204C mode configurations, and a detailed description of the settings referenced throughout this data sheet.

Table 4. AD9088BBPZ-MX-SE-SW5 Power Consumption

Parameter	Min	Typ	Max	Unit
ANALOG DOMAIN CURRENT				
AVDD1P8_DAC ($I_{AVDD1P8\_DAC\_A}$ + $I_{AVDD1P8\_DAC\_B}$)	0.27	0.35	0.30	A
AVDD1P8_ANALOG ($I_{AVDD1P8\_ADC\_A}$ + $I_{AVDD1P8\_ADC\_B}$ + $I_{AVDD1P8\_MCS}$ + $I_{AVDD1P8}$)	0.66	0.98	1.30	A
AVDD1P8_PLL ($I_{AVDD1P8\_PLL}$)	0.000	0.001	0.002	A
AVDD1P0_ADC ($I_{AVDD1P0\_ADC\_A}$ + $I_{AVDD1P0\_ADC\_B}$)	0.82	0.98	1.12	A
AVDD1P0_ADC_SCLK ($I_{AVDD1P0\_ADC\_SCLK\_A}$ + $I_{AVDD1P0\_ADC\_SCLK\_B}$)	0.24	0.26	0.29	A
AVDD1P0_ADCBK ($I_{AVDD1P0\_ADCBK\_A}$ + $I_{AVDD1P0\_ADCBK\_B}$)	2.75	3.21	3.77	A
AVDD1P0_CK ($I_{AVDD1P0\_CK}$)	0.59	0.64	0.68	A
AVDD1P0_OTHER ($I_{AVDD1P0\_MCS}$ + $I_{AVDD1P0\_PLL\_SYN}$)	0.19	0.23	0.28	A
AVDD1P0_DAC ($I_{IAVDD1P0\_DAC\_A}$ + $I_{AVDD1P0\_DAC\_B}$)	2.69	3.02	3.46	A
ANEG1P0_ADC ($I_{ANEG1P0\_ADC\_A}$ + $I_{ANEG1P0\_ADC\_B}$)	0.07	0.09	0.11	A
ANEG1P0_DAC ($I_{ANEG1P0\_DAC\_A}$ + $I_{ANEG1P0\_DAC\_B}$)	0.38	0.39	0.39	A
AVDD1P0_DAC_DIG ($I_{AVDD1P0\_DAC\_DIG\_A}$ + $I_{AVDD1P0\_DAC\_DIG\_B}$)	1.58	1.77	2.05	A
DIGITAL DOMAIN CURRENT				
DVDD1P8 ($I_{DVDD1P8}$)	0.008	0.011	0.014	A
DVDD1P0 ($I_{DVDD1P0}$)	0.001	0.002	0.004	A
DVDD0P8_ADC ($I_{DVDD0P8\_ADC}$)	2.36	3.20	4.51	A
DVDD0P8 ($I_{DVDD0P8}$)	9.38	10.40	13.23	A

SPECIFICATIONS

Table 4. AD9088BBPZ-MX-SE-SW5 Power Consumption (Continued)

Parameter	Min	Typ	Max	Unit
SERDES (JESD204B/JESD204C) DOMAIN CURRENT				
SVDD1P8_PLL ($I_{SVDD1P8\_PLL}$)	0.04	0.04	0.05	A
SVDD1P0_RX ($I_{SVDD1P0\_RX}$)	0.76	0.93	1.13	A
SVDD1P0_TX ($I_{SVDD1P0\_TX}$)	1.25	1.38	1.53	A
SVDD1P0_PLL ($I_{SVDD1P0\_PLL}$ + $I_{SVDD1P0\_PLL\_SYN}$)	0.11	0.12	0.13	A
TOTAL POWER DISSIPATION	24.6	27.2	32.7	W

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DAC DC SPECIFICATIONS

Nominal supplies with DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. DAC sample rate is 8GSPS with the digital upconverters enabled. In Table 5, for all minimum and maximum values, T_J = −10°C to +110°C, and for all typical values, T_J = 65°C, unless otherwise noted.

Table 5. DAC

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC RESOLUTION		16			Bit
DAC ANALOG OUTPUTS	DAC_Ax_P, DAC_Ax_N, DAC_Bx_P, and DAC_Bx_N				
Full-Scale Output Current Range	Common-mode output voltage (VCM_{OUT}) = 1.8V, AC-coupled only		20		mA
VCM_{OUT}	AC-coupled only		1.8		V
Differential Resistance			50		Ω
Return Loss[1]	L band (1GHz to 2GHz)		26		dB
	S band (2GHz to 4GHz)		22		dB
	C band (4GHz to 8GHz)		16		dB
	X band (8GHz to 12GHz)		16		dB
	Ku band (12GHz to 18GHz)		9		dB

1 Referenced to 50Ω differential impedance.

SINGLE-ENDED ADC DC SPECIFICATIONS

Nominal supplies, unless otherwise noted. ADC sample rate is 8GSPS with the digital downconverters enabled. In Table 6, for all minimum and maximum values, T_J = −10°C to +110°C, and for all typical values, T_J = 65°C, unless otherwise noted.

Table 6. Single-Ended ADC DC Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC RESOLUTION		12			Bit
ADC ACCURACY					
No Missing Codes			Guaranteed		
ADC ANALOG INPUTS	ADC_B0, ADC_B1, ADC_B2, ADC_B3, ADC_A0, ADC_A1, ADC_A2, and ADC_A3				
Full-Scale Input Voltage[1]			550		mV p-p
Input Power			−1.0		dBm
Common-Mode Input Voltage (VCMA_Ax and VCMA_Bx)	Equal to the voltage measured at the VCMA_Ax and VCMA_Bx pins		825		mV
Input Impedance			50		Ω
Return Loss[2]	L band (1GHz to 2GHz)		16		dB
	S band (2GHz to 4GHz)		14		dB
	C band (4GHz to 8GHz)		10		dB
	X band (8GHz to 12GHz)		23		dB
	Ku band (12GHz to 18GHz)[3]		10		dB

1 Measured with a DC signal applied at the device input.

2 Referenced to 50Ω differential impedance.

3 The AD9088 was not fully characterized above 16GHz. Performance may vary.

SPECIFICATIONS

CLOCK INPUT AND PHASE-LOCKED LOOP (PLL) SPECIFICATIONS

Nominal supplies. In Table 7, for all minimum and maximum values, T_J = −10°C to +110°C, and for all typical values, T_J = 65°C, unless otherwise noted.

Table 7. Clock Input and PLL

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUTS (CLK_B_x, CLK_A_x, and CLK_x)					
Differential Input Power		−1	+5		dBm
Common-Mode Voltage	Self biased on-chip, AC-coupled only	0.5	0.65	0.8	V
Differential Input Resistance			50		Ω
Differential Input Return Loss			10		dB
Frequency Range	Direct RF clock	5		8	GHz
PLL REFERENCE CLOCK INPUTS (PLLREF_CLK_x)					
Differential Input Voltage	Self biased on-chip, AC-coupled only	0.35		1.9	V p-p
Differential Input Resistance			100		Ω
Input Reference Frequency Range					
Direct Reference	Reference clock divider = 1	80		307.2	MHz
Divide by 2	Reference clock divider = 2	160		614.4	MHz
Divide by 4	Reference clock divider = 4	320		1228.8	MHz
VOLTAGE-CONTROLLED OSCILATOR (VCO) OUTPUT FREQUENCY RANGE	To reach below the minimum VCO rate, use the on-chip divide by 2	7.1		14.2	GHz

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SAMPLE RATE AND INSTANTANEOUS BANDWIDTH SPECIFICATIONS

Nominal supplies. In Table 8 and Table 9 for all minimum and maximum values, T_J = −10°C to +110°C, and for all typical values, T_J = 65°C, unless otherwise noted.

Table 8. DAC

Parameter	Min	Typ	Max	Unit
DAC SAMPLE RATE[1]				
Minimum			5	GSPS
Maximum	16			GSPS

[1] Pertains to the update rate of the DAC core independent of the datapath and JESD204 mode configuration.

Table 9. ADC

Parameter	Min	Typ	Max	Unit
ADC SAMPLE RATE[1]				
Minimum			5	GSPS
Maximum	8			GSPS

[1] Pertains to the update rate of the ADC core independent of the datapath and JESD204 mode configuration.

Table 10. Instantaneous Bandwidth

Parameter	Min	Typ	Max	Unit
INSTANTANEOUS BANDWIDTH[1]				
8T8R			2.7	GHz
6T6R			3.2	GHz
4T4R			4.0	GHz

[1] The instantaneous bandwidth is limited by either the JESD204B and JESD204C link throughput or the maximum ADC sample rate.

NUMERICALLY CONTROLLED OSCILLATORS (NCOS) FREQUENCY SPECIFICATIONS

Nominal supplies. In Table 11, for all minimum and maximum values, T_J = −10°C to +110°C, and for all typical values, T_J = 65°C, unless otherwise noted.

Table 11. NCO Frequency Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM NCO CLOCK RATE					
Coarse Digital Upconversion (CDUC) NCO	DAC sample rate = 16GSPS			16	GHz
Fine Digital Upconverter (FDUC) NCO				2.5	GHz
Coarse Digital Downconversion (CDDC) NCO	ADC sample rate = 8GSPS			8	GHz
Fine Digital Downconverter (FDDC) NCO				2.5	GHz

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JESD204B AND JESD204C SPEED SPECIFICATIONS

Nominal supplies. In Table 12, Table 13, Table 14, Table 15, and Table 16, for all minimum and maximum values, T_J = −10°C to +110°C, and for all typical values, T_J = 65°C, unless otherwise noted.

Table 12. Serial Interface Rate

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B SERIAL INTERFACE RATE		5.0		20	Gbps
Unit Interval		50		200	ps
JESD204C SERIAL INTERFACE RATE		1.0		28.21	Gbps
Unit Interval		35.45		1000	ps

Table 13. JESD204 Receiver (JRx) Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204 DATA INPUTS	SRXA_xN, SRXA_xP, SRXB_xP, and SRXB_xN, where x = 0 to 11				
Standards Compliance		JESD204B and JESD204C, Subclass1, Subclass 0			
Differential Voltage, R_{VDIFF}			500		mV
Differential Impedance, Z_{RDIFF}	At DC		100		Ω
Termination Voltage, V_{TT}	AC-coupled		0.5		V
SYNCOUTB_Ax_P, SYNCOUTB_Ax_N, SYNCOUTB_Bx_P, AND SYNCOUTB_Bx_N OUTPUTS[1]	Where x = 0 or 1				
Output Differential Voltage, V_{OD}	Driving 100Ω differential load		200	245	mV
Output Offset Voltage, V_{OS}		1100	1200	1300	mV
SYNCOUTB_Ax_P AND SYNCOUTB_Bx_P OUTPUT[1]	CMOS output option	Refer to the CMOS Pin Specifications section			

[1] IEEE 1596.3 standard low voltage differential signaling (LVDS) compatible.

Table 14. JESD204 Transmitter (JTx) Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204 DATA OUTPUTS	STX_AxP, STX_AxN, STX_BxP and STX_BxN, where x = 0 to 11				
Standards Compliance		JESD204B and JESD204C, Subclass 1, Subclass 0			
Differential Output Voltage	Maximum strength		500		mV
Differential Termination Impedance			100		Ω
SYNCINB_Ax_P, SYNCINB_Ax_N, SYNCINB_Bx_P, AND SYNCINB_Bx_N INPUT[1]	Where x = 0 or1				
Logic Compliance			LVDS		
Differential Input Voltage	Internal termination enabled	250			mV
Input Common-Mode Voltage	DC-coupled, Internal termination enabled	1000		1400	mV
Input Resistance (R_{IN}) (Differential)	Internal termination disabled		48		kΩ
	Internal termination enabled		250		Ω
Input Capacitance (Differential)			1		pF
SYNCINB_Ax_P AND SYNCINB_Bx_P INPUT	CMOS input option	Refer to the CMOS Pin Specifications section			

[1] IEEE 1596.3 Standard LVDS compatible.

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Table 15. SYSREF Input Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF_P, SYSREF_N, SYSREF_A_P, SYSREF_A_N, SYSREF_B_P, AND SYSREF_B_N INPUTS					
Logic Compliance			LVDS[1]		
Differential Input Voltage		350			mV
Input Common-Mode Voltage Range	High common mode (input only)	1	1.2	1.4	V
	Low common mode (bidirectional SYSREF)	0.4	0.5	0.7	V
R_{IN} (Differential)					
	SYSREF_N, SYSREF_P, SYSREF_A_P, SYSREF_A_N, SYSREF_B_P, and SYSREF_B_N inputs are on		100		Ω
	SYSREF_N, SYSREF_P, SYSREF_A_P, SYSREF_A_N, SYSREF_B_P, and SYSREF_B_N inputs are off		>30		kΩ
Input Capacitance (Differential)			1		pF
Input Frequency (f_{IN})		1	7.68	78.125	MHz

1 LVDS means low voltage differential signaling.

Table 16. SYSREF Output Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF_P, SYSREF_N, SYSREF_A_P, SYSREF_A_N, SYSREF_B_P, AND SYSREF_B_N OUTPUTS					
Logic Compliance			LVDS[1]		
Differential Output Voltage			550		mV
Output Common-Mode Voltage Range	DC-coupled		500		mV
Output Frequency (f_{OUT})		1	7.68	78.125	MHz

1 LVDS means low voltage differential signaling.

CMOS PIN SPECIFICATIONS

For the minimum and maximum values, T_J = −10°C to +110°C and nominal power supply, unless otherwise noted.

Table 17. CMOS Pin Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUTS		SPI_SDIO, SPI_CLK, SPI_CSB, RESETB, TRIG_x_B, TRIG_x_A, SYNCINB_Ax_P, SYNCINB_Ax_N, SYNCINB_Bx_P, SYNCINB_Bx_N, and GPIO_x				
Logic 1 Voltage	V_{IH}		0.70 × DVDD1P8			V
Logic 0 Voltage	V_{IL}				0.3 × DVDD1P8	V
Input Resistance				>30		kΩ
OUTPUTS		SPI_SDIO, SPI_SDO, GPIO_x, SYNCOUTB_Ax_P, SYNCOUTB_Ax_N, SYNCOUTB_Bx_P, and SYNCOUTB_Bx_N, 4mA load				
Logic 1 Voltage	V_{OH}		DVDD1P8 − 0.45			V
Logic 0 Voltage	V_{OL}				0.45	V

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DAC AC SPECIFICATIONS

Complex IQ data rate frequency (f_{IQ_DATA}) = 1.0GSPS when sample rate = 8GSPS. f_{IQ_DATA} = 4.0GSPS when sample rate = 16GSPS. Shuffle enabled, unless otherwise noted. Vector scale = −7dBFS, unless otherwise noted. Specifications represent the average of all eight DAC channels with the DAC I_{OUTFS} = 20mA, unless otherwise noted. Nominal supplies, unless otherwise noted. T_J = 65°C, unless otherwise noted.

Table 18. DAC AC Specifications

Parameter[1, 2]	Test Conditions/Comments	Min	Typ	Max	Unit
FULL SCALE OUTPUT POWER					
Single-Tone, DAC Frequency (f_{DAC}) = 8GSPS	0dBFS continuous waveform, invsinc disabled				
L Band (1GHz to 2GHz)			−3.2		dBm
S Band (2GHz to 4GHz)			−6.8		dBm
C Band (4GHz to 8GHz)			−29.2		dBm
Single-Tone, f_{DAC} = 16GSPS	0dBFS continuous waveform, invsinc disabled				
L Band (1GHz to 2GHz)			−2.9		dBm
S Band (2GHz to 4GHz)			−4.1		dBm
C Band (4GHz to 8GHz)			−7.1		dBm
X Band (8GHz to 12GHz)			−11.4		dBm
NOISE SPECTRAL DENSITY (NSD)[3]					
No Shuffling, f_{DAC} = 8GSPS	−7dBFS continuous waveform				
L Band (1GHz to 2GHz)			−163		dBFS/Hz
S Band (2GHz to 4GHz)			−161		dBFS/Hz
C Band (4GHz to 8GHz)			−160		dBFS/Hz
No Shuffling, f_{DAC} = 16GSPS	−7dBFS continuous waveform				
L Band (1GHz to 2GHz)			−165		dBFS/Hz
S Band (2GHz to 4GHz)			−162		dBFS/Hz
C Band (4GHz to 8GHz)			−160		dBFS/Hz
X Band (8GHz to 12GHz)			−161		dBFS/Hz
Shuffling, f_{DAC} = 8GSPS	−7dBFS continuous waveform				
L Band (1GHz to 2GHz)			−160		dBFS/Hz
S Band (2GHz to 4GHz)			−160		dBFS/Hz
C Band (4GHz to 8GHz)			−158		dBFS/Hz
Shuffling, f_{DAC} = 16GSPS	−7dBFS continuous waveform				
L Band (1GHz to 2GHz)			−160		dBFS/Hz
S Band (2GHz to 4GHz)			−159		dBFS/Hz
C Band (4GHz to 8GHz)			−158		dBFS/Hz
X Band (8GHz to 12GHz)			−160		dBFS/Hz
SECOND HARMONIC DISTORTION (HD2), f_{DAC} = 8GSPS	−7dBFS continuous waveform, shuffling on				
L Band (1GHz to 2GHz)			−87		dBc
S Band (2GHz to 4GHz)			−84		dBc
C Band (4GHz to 8GHz)			−68		dBc
HD2, f_{DAC} = 16GSPS	−7dBFS continuous waveform, shuffling on				
L Band (1GHz to 2GHz)			−86		dBc
S Band (2GHz to 4GHz)			−89		dBc
C Band (4GHz to 8GHz)			−81		dBc
X Band (8GHz to 12GHz)			−77		dBc
THIRD HARMONIC DISTORTION (HD3), f_{DAC} = 8GSPS	−7dBFS continuous waveform, shuffling on				
L Band (1GHz to 2GHz)			−98		dBc
S Band (2GHz to 4GHz)			−94		dBc
C Band (4GHz to 8GHz)			−64		dBc

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Table 18. DAC AC Specifications (Continued)

Parameter[1, 2]	Test Conditions/Comments	Min	Typ	Max	Unit
HD3, f_{DAC} = 16GSPS	−7dBFS continuous waveform, shuffling on				
L Band (1GHz to 2GHz)			−99		dBc
S Band (2GHz to 4GHz)			−96		dBc
C Band (4GHz to 8GHz)			−95		dBc
X Band (8GHz to 12GHz)			−87		dBc
DOUBLE DATA RATE (DDR) Spur, f_{DAC} = 8GSPS	−7dBFS continuous waveform, shuffling on				
L Band (1GHz to 2GHz)			−66		dBc
S Band (2GHz to 4GHz)			−60		dBc
C Band (4GHz to 8GHz)			−51		dBc
DDR Spur, f_{DAC} = 16GSPS	−7dBFS continuous waveform, shuffling on				
L Band (1GHz to 2GHz)			−79		dBc
S Band (2GHz to 4GHz)			−76		dBc
C Band (4GHz to 8GHz)			−71		dBc
X Band (8GHz to 12GHz)			−70		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR), Excluding HD2, HD3, DDR Spur, f_{DAC}, and $f_{DAC}/2$	f_{DAC} = 8GSPS, −7dBFS continuous waveform, shuffling on				
L Band (1GHz to 2GHz)			−87		dBc
S Band (2GHz to 4GHz)			−82		dBc
C Band (4GHz to 8GHz)			−82		dBc
SFDR, Excluding HD2, HD3, DDR Spur, f_S, and $f_S/2$	f_{DAC} = 16GSPS, −7dBFS continuous waveform, shuffling off				
L Band (1GHz to 2GHz)			−83		dBc
S Band (2GHz to 4GHz)			−81		dBc
C Band (4GHz to 8GHz)			−79		dBc
X Band (8GHz to 12GHz)			−74		dBc
THIRD-ORDER INTERMODULATION DISTORTION (IMD3), f_{DAC} = 8GSPS	Two-tone test, −13dBFS per tone (vector backoff −7dBFS)				
L Band (1GHz to 2GHz)			−90		dBc
S Band (2GHz to 4GHz)			−86		dBc
C Band (4GHz to 8GHz)	f_{OUT} = 7.82GHz, upper edge of C band and the second Nyquist of the DAC; for detailed data, see Figure 22		−54		dBc
IMD3, f_{DAC} = 16GSPS	Two-tone test, −13dBFS per tone (vector backoff −7dBFS)				
L Band (1GHz to 2GHz)			−91		dBc
S Band (2GHz to 4GHz)			−89		dBc
C Band (4GHz to 8GHz)			−80		dBc
X Band (8GHz to 12GHz)			−75		dBc
RESIDUAL SINGLE SIDEBAND PHASE NOISE PER OFFSET FREQUENCY, f_{DAC} = 8GSPS	f_{OUT} = 1.6GHz, 0dBFS continuous waveform				
1kHz			−131		dBc/Hz
100kHz			−149		dBc/Hz
600kHz			−157		dBc/Hz
1.2MHz			−159		dBc/Hz
1.8MHz			−160		dBc/Hz
6MHz			−162		dBc/Hz

SPECIFICATIONS

Table 18. DAC AC Specifications (Continued)

Parameter[1, 2]	Test Conditions/Comments	Min	Typ	Max	Unit
RESIDUAL SINGLE SIDEBAND PHASE NOISE PER OFFSET FREQUENCY, f_{DAC} = 16GSPS	f_{OUT} = 1.6GHz, 0dBFS continuous waveform				
1kHz			−134		dBc/Hz
100kHz			−152		dBc/Hz
600kHz			−158		dBc/Hz
1.2MHz			−160		dBc/Hz
1.8MHz			−161		dBc/Hz
6MHz			−161		dBc/Hz
RF OUTPUT FREQUENCY					
Maximum			16		GHz
Minimum				10	kHz

1 Evaluation set up is de-embedded to DAC output balls up to 20GHz.

2 Performance exhibits variability across the frequency spectrum. For detailed frequency response plots, refer to the Typical Performance Characteristics section.

3 Values are determined with reference to the full scale at 10kHz.

SINGLE-ENDED ADC AC SPECIFICATIONS

8GSPS

Nominal supplies, sample rate = 8GSPS, and f_{IQ_DATA} = 1.0GSPS, unless otherwise noted. T_J = 65°C, unless otherwise noted. Analog input amplitude (A_{IN}) = −7dBFS, unless otherwise noted. Random mode is enabled. The typical values shown for the given L band, S band, C band, and X band correspond to a frequency point near the band edge; for additional details, see the plots in the typical performance characteristics ADC 8GSPS section.

Table 19. 8GSPS

Parameter	Full-Scale Input Voltage = 500mV p-p (Equivalent to −1.0dBm)			Unit
	Min	Typ	Max	
NSD				
At −20dBFS				
Across the Analog Bandwidth of the ADC		−146.4		dBFS/Hz
At −7dBFS				
L Band (1GHz to 2GHz)		−144.9		dBFS/Hz
S Band (2GHz to 4GHz)		−145.1		dBFS/Hz
C Band (4GHz to 8GHz)		−144.5		dBFS/Hz
X Band (8GHz to 12GHz)		−143.8		dBFS/Hz
Ku Band (12GHz to 18GHz)[1]		−141.8		dBFS/Hz
HD2				
L Band (1GHz to 2GHz)		−60		dBFS
S Band (2GHz to 4GHz)		−67		dBFS
C Band (4GHz to 8GHz)		−67		dBFS
X Band (8GHz to 12GHz)		−65		dBFS
Ku Band (12GHz to 18GHz)[1]		−66		dBFS
HD3				
L Band (1GHz to 2GHz)		−78		dBFS
S Band (2GHz to 4GHz)		−78		dBFS
C Band (4GHz to 8GHz)		−79		dBFS
X Band (8GHz to 12GHz)		−78		dBFS
Ku Band (12GHz to 18GHz)[1]		−79		dBFS

SPECIFICATIONS

Table 19. 8GSPS (Continued)

Parameter	Full-Scale Input Voltage = 500mV p-p (Equivalent to −1.0dBm)			
	Min	Typ	Max	Unit
$f_S/2 \pm A_{IN}$ Spur				
L Band (1GHz to 2GHz)		−86		dBFS
S Band (2GHz to 4GHz)		−83		dBFS
C Band (4GHz to 8GHz)		−81		dBFS
X Band (8GHz to 12GHz)		−78		dBFS
Ku Band (12GHz to 18GHz)[1]		−70		dBFS
SFDR, EXCLUDING HD2, HD3, and $f_S/2 \pm A_{IN}$				
L Band (1GHz to 2GHz)		−85		dBFS
S Band (2GHz to 4GHz)		−86		dBFS
C Band (4GHz to 8GHz)		−83		dBFS
X Band (8GHz to 12GHz)		−82		dBFS
Ku Band (12GHz to 18GHz)[1]		−79		dBFS
TWO-TONE IMD3, Input Amplitude 1 (A_{IN1}) = Input Amplitude 2 (A_{IN2}) = −13dBFS				
L Band (1GHz to 2GHz)		−81		dBFS
S Band (2GHz to 4GHz)		−86		dBFS
C Band (4GHz to 8GHz)		−86		dBFS
X Band (8GHz to 12GHz)		−82		dBFS
Ku Band (12GHz to 18GHz)[1]		−78		dBFS

[1] The AD9088 was not fully characterized above 16GHz. Performance may vary.

Others

Table 20. Others

Parameter	Min	Typ	Max	Unit
ANALOG BANDWIDTH				
−3dB Frequency		14.5		GHz
−8dB Frequency		>20		GHz

SPECIFICATIONS

SERIAL PORT INTERFACE (SPI) AND HIGH SPEED CONTROL INTERFACE (HSCI) SPECIFICATIONS

For the minimum and maximum values, T_J = −10°C to +110°C with nominal supply, unless otherwise noted.

Table 21. SPI Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI OPERATION		See Figure 2				
Maximum Serial Clock (SCLK) Rate	f_{SCLK}, $1/t_{SCLK}$		50			MHz
SPI_CLK Clock High	t_{PWH}	SCLK = 50MHz	8			ns
SPI_CLK Clock Low	t_{PWL}	SCLK = 50MHz	8			ns
SPI_SDIO to SPI_CLK Setup Time	t_{DS}		7			ns
SPI_CLK to SPI_SDIO Hold Time	t_{DH}		4			ns
SPI_CSB to SPI_CLK Setup Time	t_S		4			ns
SPI_CLK to SPI_CSB Hold Time	t_H		4			ns

Table 22. HSCI Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
HSCI_DIN_N, HSCI_DIN_P, HSCI_CKIN_P, AND HSCI_CKIN_N INPUTS					
Logic Compliance			LVDS[1]		
Differential Input Voltage			0.43		V p-p
Input Common-Mode Voltage Range	DC-coupled		1.2		V
R_{IN} (Differential)			100		Ω
Clock Duty Cycle			50		%
Data Rate		0.4	1.6	1.6	Gbps
HSCI_DO_P, HSCI_DO_N, HSCI_CKO_P, AND HSCI_CKO_N OUTPUTS					
Logic Compliance			LVDS[1]		
Differential Swing	Driving 100Ω differential load, DC-coupled		0.5		V p-p
Output Common-Mode Voltage Range	DC-coupled		1.19		V
Data Rate		0.4	1.6	1.6	Gbps
Clock Duty Cycle			50		%

[1] LVDS means low voltage differential signaling.

SPI Timing Diagram

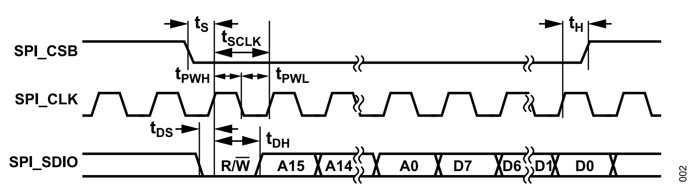

Figure 2. Timing Diagram for 3-Wire Operation

ABSOLUTE MAXIMUM RATINGS

Table 23. Absolute Maximum Ratings

Parameter	Rating
ADC_B0, ADC_B1, ADC_B2, ADC_B3, ADC_A0, ADC_A1, ADC_A2, and ADC_A3[1]	13dBm
AVDD1P8_DAC_A and AVDD1P8_DAC_B	−0.2V to +2.1V
AVDD1P8, AVDD1P8_MCS, AVDD1P8_PLL, AVDD1P8_ADC_A, and AVDD1P8_ADC_B	−0.2V to +2.1V
AVDD1P0_CK, AVDD1P0_MCS, AVDD1P0_ADC_A, AVDD1P0_ADC_B, AVDD1P0_ADC_SCLK_A, AVDD1P0_ADC_SCLK_B, AVDD1P0_ADCBK_A, AVDD1P0_ADCBK_B, AVDD1P0_DAC_A, AVDD1P0_DAC_B, and AVDD1P0_PLL_SYN	−0.2V to +1.1V
ANEG1P0_ADC_A, ANEG1P0_ADC_B, ANEG1P0_DAC_A, and ANEG1P0_DAC_B	−1.05V to +0.2V
DVDD1P8	−0.2V to +2.1V
DVDD1P0	−0.2V to +1.1V
DVDD0P8 and DVDD0P8_ADC	−0.2V to +1.1V
SVDD1P8_PLL	−0.2V to +2.1V
SVDD1P0_RX, SVDD1P0_TX, SVDD1P0_PLL, and SVDD1P0_PLL_SYN	−0.2V to +1.1V
CLK_P, CLK_N, CLK_B_P, CLK_B_N, CLK_A_P, and CLK_A_N	−0.2V to +1.05V
PLLREF_CLK_P and PLLREF_CLK_N	−0.2V to +1.05V
SRXA_xP, SRXA_xN, SRXB_xP, SRXB_xN, STXA_xP, STA_xN, STXB_xP, and STXB_xN	−0.2V to +1.05V
SYSREF_A_N, SYSREF_A_P, SYSREF_B_P, SYSREF_B_N, SYSREF_P, and SYSREF_N	−0.2V to +2.1V
SYNCINB_B0_P, SYNCINB_B0_N, SYNCINB_B1_P, SYNCINB_B1_N, SYNCINB_A0_P, SYNCINB_A0_N, SYNCINB_A1_P, and SYNCINB_A1_N	−0.2V to +2.1V
SYNCOUTB_B0_P, SYNCOUTB_B0_N, SYNCOUTB_B1_P, SYNCOUTB_B1_N, SYNCOUTB_A0_P, SYNCOUTB_A0_N, SYNCOUTB_A1_P, and SYNCOUTB_A1_N	−0.2V to +2.1V
RESETB, SPI_CSB, SPI_CLK, SPI_SDIO, SPI_SDO, GPIO_x, TRIG_x_B, and TRIG_x_A	−0.2V to +2.1V
HSCI_DIN_P, HSCI_DIN_N, HSCI_CKIN_P, HSCI_CKIN_N, HSCI_DO_P, HSCI_DO_N, HSCI_CKO_P, and HSCI_CKO_N	−0.2V to +2.1V
Temperature	
Junction (T_J)[2]	110°C
Storage Range	−65°C to +150°C

1 The absolute maximum input swing allowed at the inputs of the AD9088 is 5.6V p-p differential. Signals operating at this level or more than this level can cause instantaneous permanent damage to the ADC.

2 Do not exceed this temperature for any duration of time when the device is powered. Specified temperature is the average die temperature.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

All ADCs are enabled upon startup. In systems that require a selectable number of ADCs for optimum lifetime performance, all ADCs must remain enabled and clocking. The associated receive digital data path can be disabled for the unused ADCs. All DACs are enabled upon startup for a given variant (see Table 24)

Table 24. SW Variants and DACs Forced On

Variant	DACs Forced On
SW5	A0, A1, A2, A3, B0, B1, B2, B3

In systems that require a selectable number of DACs for optimum lifetime performance, all DACs must remain enabled and clocking. The associated transmit digital data path can be disabled for the unused DACs. Similarly, all transmit SERDES lanes are enabled by default.

In systems where certain ADCs, DACs, and/or transmit SERDES lanes remain disabled for the lifetime of the system, the user can request a special procedure from Analog Devices, Inc., to run during startup that disables those ADCs, DACs, or transmit SERDES lanes to remain permanently disabled. Contact your local Analog Devices sales representative or email ApolloSupport@analog.com for additional information.

REFLOW PROFILE

The AD9088 reflow profile is in accordance with the JEDEC J-STD-020 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum T_J does not exceed the limits shown in Table 23.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure, θ_{JC_TOP} is the junction to case, top thermal resistance, θ_{JC_BOT} is the junction to case, bottom thermal resistance, Ψ_{JT} is the junction to top of the package thermal resistance, and Ψ_{JB} is the junction to the board thermal resistance.

Table 25. Simulated Thermal Resistance[1]

Package Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOT}	Ψ_{JT}	Ψ_{JB}	Unit
BP-899-3							
JEDEC 2s2p Board	0.0	8.41		0.54	0.71	2.2	°C/W
JEDEC 1s0p Board	0.0		0.3				°C/W

1 Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 32W.

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD RATINGS)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDDEC JS-002.

ESD Ratings for AD9088

Table 26. AD9088, 899-Ball BGA_ED

ESD Model	Withstand Threshold (V)	Class
HBM	±200	0B
CDM	±150	C0B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

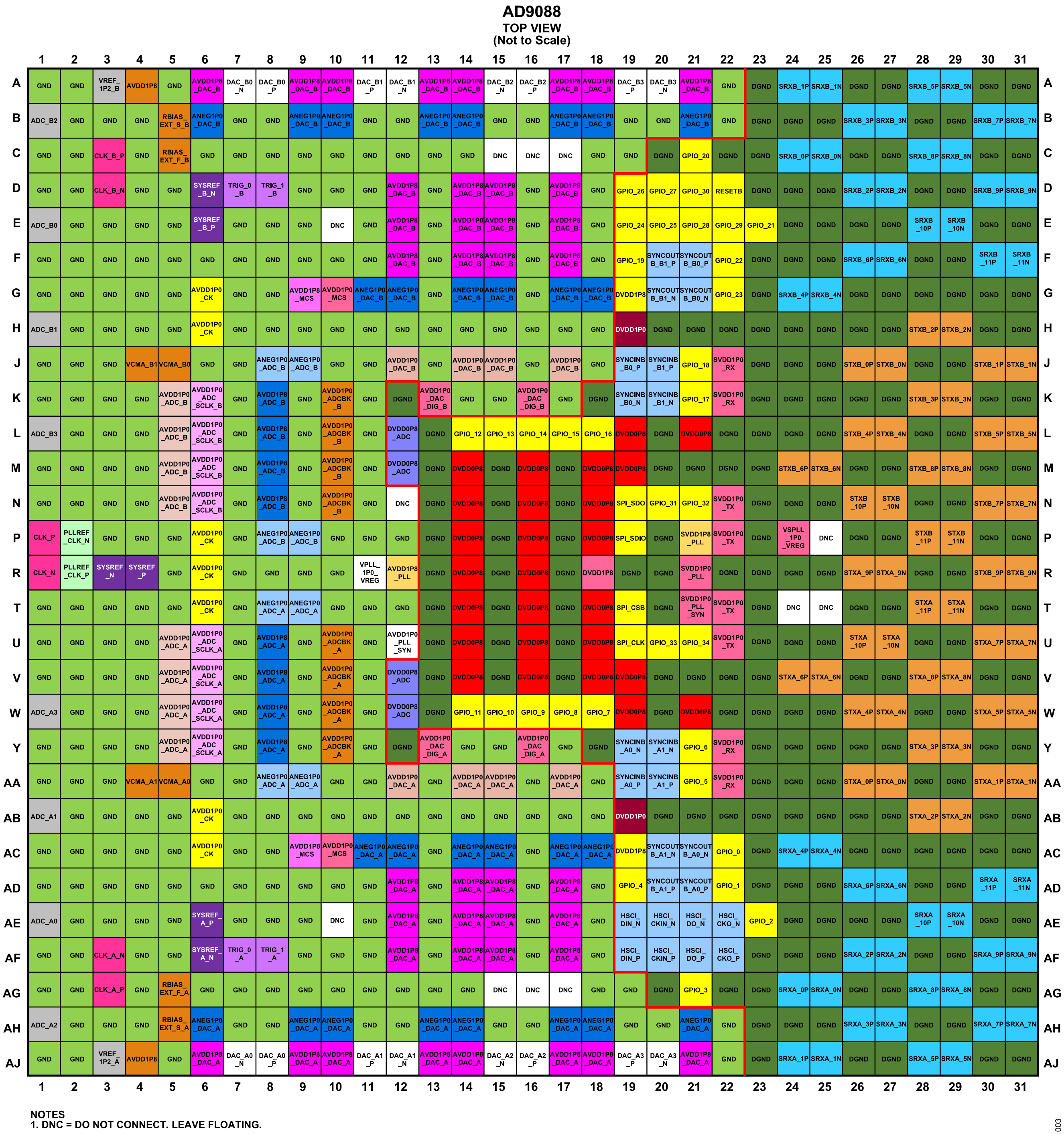

Figure 3. Pin Configuration (8T8R Single-Ended ADC)

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 27. Pin Function Descriptions (8T8R Single-Ended ADC)

Pin No.	Mnemonic	Type	Description
ANALOG POWER SUPPLIES			
A6, A9, A10, A13, A14, A17, A18, A21, D12, D14, D15, D17, E12, E14, E15, E17, F12, F14, F15, F17	AVDD1P8_DAC_B	Input	DAC Analog 1.8V Supply Inputs for Bank B.
AD12, AD14, AD15, AD17, AE12, AE14, AE15, AE17, AF12, AF14, AF15, AF17, AJ6, AJ9, AJ10, AJ13, AJ14, AJ17, AJ18, AJ21	AVDD1P8_DAC_A	Input	DAC Analog 1.8V Supply Inputs for Bank A.
A4, AJ4	AVDD1P8	Input	DAC Analog 1.8V Supply Input.
R12	AVDD1P8_PLL	Input	On-Chip Clock Phase-Locked Loop (PLL) 1.8V Analog Supply Input.
G9, AC9	AVDD1P8_MCS	Input	Analog 1.8V Supply Input for Multichip Synchronization.
K8, L8, M8, N8	AVDD1P8_ADC_B	Input	ADC Analog 1.8V Supply Input for Bank B.
U8, V8, W8, Y8	AVDD1P8_ADC_A	Input	ADC Analog 1.8V Supply Input for Bank A.
U12	AVDD1P0_PLL_SYN	Input	Analog Clock PLL Synthesizer 1.0V Supply Input.
G10, AC10	AVDD1P0_MCS	Input	Analog 1.0V Supply Input for Multichip Synchronization.
G6, H6, P6, R6, T6, AB6, AC6	AVDD1P0_CK	Input	Analog 1.0V Supply Input for Chip Clock.
J12, J14, J15, J17	AVDD1P0_DAC_B	Input	DAC Analog 1.0V Supply Input for Bank B.
AA12, AA14, AA15, AA17	AVDD1P0_DAC_A	Input	DAC Analog 1.0V Supply Input for Bank A.
K5, L5, M5, N5	AVDD1P0_ADC_B	Input	ADC Analog 1.0V Supply Input for Bank B.
U5, V5, W5, Y5	AVDD1P0_ADC_A	Input	ADC Analog 1.0V Supply Input for Bank A.
K6, L6, M6, N6	AVDD1P0_ADC_SCLK_B	Input	ADC Analog Clock 1.0V Supply Input for Bank B.
U6, V6, W6, Y6	AVDD1P0_ADC_SCLK_A	Input	ADC Analog Clock 1.0V Supply Input for Bank A.
K10, L10, M10, N10	AVDD1P0_ADCBK_B	Input	ADC Back-End Analog 1.0V Supply Input for Bank B.
U10, V10, W10, Y10	AVDD1P0_ADCBK_A	Input	ADC Back-End Analog 1.0V Supply Input for Bank A.
B6, B9, B10, B13, B14, B17, B18, B21, G11, G12, G14, G15, G17, G18	ANEG1P0_DAC_B	Input	DAC Analog −1.0V Supply Input for Bank B.
AC11, AC12, AC14, AC15, AC17, AC18, AH6, AH9, AH10, AH13, AH14, AH17, AH18, AH21	ANEG1P0_DAC_A	Input	DAC Analog −1.0V Supply Input for Bank A.
J8, J9, P8, P9	ANEG1P0_ADC_B	Input	ADC Analog −1.0V Supply Input for Bank B.
T8, T9, AA8, AA9	ANEG1P0_ADC_A	Input	ADC Analog −1.0V Supply Input for Bank A.
A3, AJ3	VREF_1P2_B, VREF_1P2_A	Input/output	1.2V Reference for the ADC and DAC Cores for Bank B and Bank A, respectively. Connect these pins to GND with a 0.1µF capacitor when using the on-chip reference. Or, connect these pins to an external 1.2V reference for improved AM noise.
P24	VSPLL_1P0_VREG	Output	1.0V Supply Output for SERDES clock PLL. Decouple this pin to DGND with a 0.1µF capacitor in parallel with a 1µF capacitor.
R11	VPLL_1P0_VREG	Output	1.0V Supply Output for On-Chip Clock PLL. Decouple this pin to GND with a 0.1µF capacitor in parallel with a 1µF capacitor.
DIGITAL POWER SUPPLIES			
G19, R18, AC19	DVDD1P8	Input	Digital 1.8V Supply Input.
H19, AB19	DVDD1P0	Input	Digital 1.0V Supply Input.
L12, M12, V12, W12	DVDD0P8_ADC	Input	ADC Digital 0.8V Supply Input.
L19, L21, M14, M16, M18, M19, N14, N16, N18, P14, P16, P18, R14, R16, T14, T16, T18, U14, U16, U18, V14, V16, V18, V19, W19, W21	DVDD0P8	Input	Main Digital 0.8V Supply Input.
MIXED POWER SUPPLIES			
K13, K16	AVDD1P0_DAC_DIG_B	Input	DAC Digital and Analog 1.0V Supply Input for Bank B.
Y13, Y16	AVDD1P0_DAC_DIG_A	Input	DAC Digital and Analog 1.0V Supply Input for Bank A.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 27. Pin Function Descriptions (8T8R Single-Ended ADC) (Continued)

Pin No.	Mnemonic	Type	Description
SERDES POWER SUPPLIES			
P21	SVDD1P8_PLL	Input	SERDES PLL 1.8V Supply Input.
R21	SVDD1P0_PLL	Input	SERDES PLL 1.0V Supply Input.
T21	SVDD1P0_PLL_SYN	Input	SERDES PLL Synthesizer 1.0V Supply Input.
J22, K22, Y22, AA22	SVDD1P0_RX	Input	JESD204B and JESD204C Receive 1.0V Supply Input.
N22, P22, T22, U22	SVDD1P0_TX	Input	JESD204B and JESD204C Transmit 1.0V Supply Input.
ANALOG GROUND			
A1, A2, A5, A22, B2, B3, B4, B7, B8, B11, B12, B15, B16, B19, B20, B22, C1, C2, C4, C6, C7, C8, C9, C10, C11, C12, C13, C14, C18, C19, D1, D2, D4, D5, D9, D10, D11, D13, D16, D18, E2, E3, E4, E5, E7, E8, E9, E11, E13, E16, E18, F1, F2, F3, F4, F5, F6, F7, F8, F9, F10, F11, F13, F16, F18, G1, G2, G3, G4, G5, G7, G8, G13, G16, H2, H3, H4, H5, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, J1, J2, J3, J6, J7, J10, J11, J13, J16, J18, K1, K2, K3, K4, K7, K9, K11, K14, K15, K17, L2, L3, L4, L7, L9, L11, M1, M2, M3, M4, M7, M9, M11, N1, N2, N3, N4, N7, N9, N11, P3, P4, P5, P7, P10, P11, P12, R5, R7, R8, R9, R10, T1, T2, T3, T4, T5, T7, T10, T11, T12, U1, U2, U3, U4, U7, U9, U11, V1, V2, V3, V4, V7, V9, V11, W2, W3, W4, W7, W9, W11, Y1, Y2, Y3, Y4, Y7, Y9, Y11, Y14, Y15, Y17, AA1, AA2, AA3, AA6, AA7, AA10, AA11, AA13, AA16, AA18, AB2, AB3, AB4, AB5, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AC1, AC2, AC3, AC4, AC5, AC7, AC8, AC13, AC16, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD13, AD16, AD18, AE2, AE3, AE4, AE5, AE7, AE8, AE9, AE11, AE13, AE16, AE18, AF1, AF2, AF4, AF5, AF9, AF10, AF11, AF13, AF16, AF18, AG1, AG2, AG4, AG6, AG7, AG8, AG9, AG10, AG11, AG12, AG13, AG14, AG18, AG19, AH2, AH3, AH4, AH7, AH8, AH11, AH12, AH15, AH16, AH19, AH20, AH22, AJ1, AJ2, AJ5, AJ22	GND	Input/output	Analog Ground References.
DIGITAL GROUND			
A23, A26, A27, A30, A31, B23, B24, B25, B28, B29, C20, C22, C23, C26, C27, C30, C31, D23, D24, D25, D28, D29, E24, E25, E26, E27, E30, E31, F23, F24, F25, F28, F29, G23, G26, G27, G28, G29, G30, G31, H20, H21, H22, H23, H24, H25, H26, H27, H30, H31, J23, J24, J25, J28, J29, K12, K18, K23, K24, K25, K26, K27, K30, K31, L13, L20, L22, L23, L24, L25, L28, L29, M13, M15, M17, M20, M21, M22, M23, M26, M27, M30, M31, N13, N15, N17, N23, N24, N25, N28, N29, P13, P15, P17, P20, P23, P26, P27, P30, P31, R13, R15, R17, R19, R20, R22, R23, R24, R25, R28, R29, T13, T15, T17, T20, T23, T26, T27, T30, T31, U13, U15, U17, U23, U24, U25, U28, U29, V13, V15, V17, V20, V21, V22, V23, V26, V27, V30, V31, W13, W20, W22, W23, W24, W25, W28, W29, Y12, Y18, Y23, Y24, Y25, Y26, Y27, Y30, Y31, AA23, AA24, AA25, AA28,	DGND	Input/output	Digital Ground References.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 27. Pin Function Descriptions (8T8R Single-Ended ADC) (Continued)

Pin No.	Mnemonic	Type	Description
AA29, AB20, AB21, AB22, AB23, AB24, AB25, AB26, AB27, AB30, AB31, AC23, AC26, AC27, AC28, AC29, AC30, AC31, AD23, AD24, AD25, AD28, AD29, AE24, AE25, AE26, AE27, AE30, AE31, AF23, AF24, AF25, AF28, AF29, AG20, AG22, AG23, AG26, AG27, AG30, AG31, AH23, AH24, AH25, AH28, AH29, AJ23, AJ26, AJ27, AJ30, AJ31			
ADC INPUTS			
B1	ADC_B2	Input	ADC_B2 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
E1	ADC_B0	Input	ADC_B0 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
H1	ADC_B1	Input	ADC_B1 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
L1	ADC_B3	Input	ADC_B3 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
W1	ADC_A3	Input	ADC_A3 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
AB1	ADC_A1	Input	ADC_A1 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
AE1	ADC_A0	Input	ADC_A0 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
AH1	ADC_A2	Input	ADC_A2 Single-Ended Input with an Internal 50Ω Resistor. These pins are floating when unused.
DAC OUTPUTS			
A7, A8	DAC_B0_N, DAC_B0_P	Output	DAC_B0 Outputs, 1.8V Referenced. Tie these pins to 1.8V if unused.
A11, A12	DAC_B1_P, DAC_B1_N	Output	DAC_B1 Outputs, 1.8V Referenced. Tie these pins to 1.8V if unused.
A15, A16	DAC_B2_N, DAC_B2_P	Output	DAC_B2 Outputs, 1.8V Referenced. Tie these pins to 1.8V if unused.
A19, A20	DAC_B3_P, DAC_B3_N	Output	DAC_B3 Outputs, 1.8V Referenced. Tie these pins to 1.8V if unused.
AJ7, AJ8	DAC_A0_N, DAC_A0_P	Output	DAC_A0 Outputs, 1.8V Referenced. Tie these pins to 1.8V if unused.
AJ11, AJ12	DAC_A1_P, DAC_A1_N	Output	DAC_A1 Outputs, 1.8V Referenced. Available on SW5 only. Tie these pins to 1.8V if unused.
AJ15, AJ16	DAC_A2_N, DAC_A2_P	Output	DAC_A2 Outputs, 1.8V Referenced. Available on SW5 only. Tie these pins to 1.8V if unused.
AJ19, AJ20	DAC_A3_P, DAC_A3_N	Output	DAC_A3 Outputs, 1.8V Referenced. Tie these pins to 1.8V if unused.
CLOCK INPUTS			
C3, D3	CLK_B_P, CLK_B_N	Input	Differential Direct Clock Inputs for Bank B with an Internal 50Ω Differential Resistor. Float these pins if unused.
P1, R1	CLK_P, CLK_N	Input	Differential Clock Inputs with an Internal 50Ω Differential Resistor. Float these pins if unused.
P2, R2	PLLREF_CLK_N, PLLREF_CLK_P	Input	On-Chip PLL Reference Differential Input with an Internal 100Ω Differential Resistor. Float these pins if unused.
AF3, AG3	CLK_A_N, CLK_A_P	Input	Differential Direct Clock Input for Bank A with an Internal 50Ω Differential Resistor. Float these pins if unused.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 27. Pin Function Descriptions (8T8R Single-Ended ADC) (Continued)

Pin No.	Mnemonic	Type	Description
HSCI PORT INPUTS AND OUTPUTS			
AE19, AF19	HSCI_DIN_N, HSCI_DIN_P	Input	HSCI Data LVDS Input with a Programmable Internal 100Ω Differential Resistor.
AE20, AF20	HSCI_CKIN_N, HSCI_CKIN_P	Input	HSCI Clock LVDS Input with a Programmable Internal 100Ω Differential Resistor.
AE21, AF21	HSCI_DO_N, HSCI_DO_P	Output	HSCI Data LVDS Output.
AE22, AF22	HSCI_CKO_N, HSCI_CKO_P	Output	HSCI Clock LVDS Output.
CMOS INPUTS AND OUTPUTS			
B5	RBIAS_EXT_S_B	Input	DAC Bias Current Setting Pin. Connect this pin to RBIAS_EXT_F_B.
C5	RBIAS_EXT_F_B	Output	DAC Bias Current Setting Pin. Connect this pin to a 464Ω resistor with 0.1% precision.
AG5	RBIAS_EXT_F_A	Output	DAC Bias Current Setting Pin. Connect this pin to a 464Ω resistor with 0.1% precision.
AH5	RBIAS_EXT_S_A	Input	DAC Bias Current Setting Pin. Connect this pin to RBIAS_EXT_F_A.
C21	GPIO_20	Input/output	General-Purpose Input and Output (GPIO).
D7	TRIG_0_B	Input	Trigger Input 0 for Bank B. This pin is floating when unused.
D8	TRIG_1_B	Input	Trigger Input 1 for Bank B. This pin is floating when unused.
D19	GPIO_26	Input/output	GPIO.
D20	GPIO_27	Input/output	GPIO.
D21	GPIO_30	Input/output	GPIO
D22	RESETB	Input	Active Low Reset Input. RESETB places digital logic and SPI registers in a known default state. RESETB must be connected to a digital IC that is capable of issuing a reset signal for the first step in the device initialization process.
E19	GPIO_24	Input/output	GPIO.
E20	GPIO_25	Input/output	GPIO.
E21	GPIO_28	Input/output	GPIO.
E22	GPIO_29	Input/output	GPIO.
E23	GPIO_21	Input/output	GPIO.
F19	GPIO_19	Input/output	GPIO.
F22	GPIO_22	Input/output	GPIO.
G22	GPIO_23	Input/output	GPIO.
J4, J5	VCMA_B1, VCMA_B0	Output	ADC Buffers for VCM_{OUT} for Bank B. Decouple these pins to GND with a 1nF capacitor.
J21	GPIO_18	Input/output	GPIO.
K21	GPIO_17	Input/output	GPIO.
L14	GPIO_12	Input/output	GPIO.
L15	GPIO_13	Input/output	GPIO.
L16	GPIO_14	Input/output	GPIO.
L17	GPIO_15	Input/output	GPIO.
L18	GPIO_16	Input/output	GPIO.
N19	SPI_SDO	Output	Serial Port Data Output.
N20	GPIO_31	Input/output	GPIO.
N21	GPIO_32	Input/output	GPIO.
P19	SPI_SDIO	Input/output	Serial Port Bidirectional Data Input and Output.
T19	SPI_CSB	Input	Serial Port Enable Input. Active low.
U19	SPI_CLK	Input	Serial Port Clock Input.
U20	GPIO_33	Input/output	GPIO.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 27. Pin Function Descriptions (8T8R Single-Ended ADC) (Continued)

Pin No.	Mnemonic	Type	Description
U21	GPIO_34	Input/output	GPIO.
W14	GPIO_11	Input/output	GPIO.
W15	GPIO_10	Input/output	GPIO.
W16	GPIO_9	Input/output	GPIO.
W17	GPIO_8	Input/output	GPIO.
W18	GPIO_7	Input/output	GPIO.
Y21	GPIO_6	Input/output	GPIO.
AA4, AA5	VCMA_A1, VCMA_A0	Output	ADC Buffers for VCM_{OUT} for Bank A. Decouple these pins to GND with a 1nF capacitor
AA21	GPIO_5	Input/output	GPIO.
AC22	GPIO_0	Input/output	GPIO.
AD19	GPIO_4	Input/output	GPIO.
AD22	GPIO_1	Input/output	GPIO.
AE23	GPIO_2	Input/output	GPIO.
AF7	TRIG_0_A	Input	Trigger Input 0 for Bank A.
AF8	TRIG_1_A	Input	Trigger Input 1 for Bank A.
AG21	GPIO_3	Input/output	GPIO.
JESD204B- OR JESD204C-COMPATIBLE SERDES DATA LANES AND CONTROL SIGNALS[1]			
H28, H29	STXB_2P, STXB_2N	Output	JTx Lane Outputs, Data True and Complement.
J26, J27	STXB_0P, STXB_0N	Output	JTx Lane Outputs, Data True and Complement.
J30, J31	STXB_1P, STXB_1N	Output	JTx Lane Outputs, Data True and Complement.
K28, K29	STXB_3P, STXB_3N	Output	JTx Lane Outputs, Data True and Complement.
L26, L27	STXB_4P, STXB_4N	Output	JTx Lane Outputs, Data True and Complement.
L30, L31	STXB_5P, STXB_5N	Output	JTx Lane Outputs, Data True and Complement.
M24, M25	STXB_6P, STXB_6N	Output	JTx Lane Outputs, Data True and Complement.
M28, M29	STXB_8P, STXB_8N	Output	JTx Lane Outputs, Data True and Complement.
N26, N27	STXB_10P, STXB_10N	Output	JTx Lane Outputs, Data True and Complement.
N30, N31	STXB_7P, STXB_7N	Output	JTx Lane Outputs, Data True and Complement.
P28, P29	STXB_11P, STXB_11N	Output	JTx Lane Outputs, Data True and Complement.
R26, R27	STXA_9P, STXA_9N	Output	JTx Lane Outputs, Data True and Complement.
R30, R31	STXB_9P, STXB_9N	Output	JTx Lane Outputs, Data True and Complement.
T28, T29	STXA_11P, STXA_11N	Output	JTx Lane Outputs, Data True and Complement.
U26, U27	STXA_10P, STXA_10N	Output	JTx Lane Outputs, Data True and Complement.
U30, U31	STXA_7P, STXA_7N	Output	JTx Lane Outputs, Data True and Complement.
V24, V25	STXA_6P, STXA_6N	Output	JTx Lane Outputs, Data True and Complement.
V28, V29	STXA_8P, STXA_8N	Output	JTx Lane Outputs, Data True and Complement.
W26, W27	STXA_4P, STXA_4N	Output	JTx Lane Outputs, Data True and Complement.
W30, W31	STXA_5P, STXA_5N	Output	JTx Lane Outputs, Data True and Complement.
Y28, Y29	STXA_3P, STXA_3N	Output	JTx Lane Outputs, Data True and Complement.
AA26, AA27	STXA_0P, STXA_0N	Output	JTx Lane Outputs, Data True and Complement.
AA30, AA31	STXA_1P, STXA_1N	Output	JTx Lane Outputs, Data True and Complement.
AB28, AB29	STXA_2P, STXA_2N	Output	JTx Lane Outputs, Data True and Complement.
D6, E6	SYSREF_B_N, SYSREF_B_P	Input	SYSREF_P and SYSREF_N Inputs for CLK_B_P and CLK_B_N .
R3, R4	SYSREF_N, SYSREF_P	Input	SYSREF_P and SYSREF_N Inputs for CLK_P and CLK_N .
AE6, AF6	SYSREF_A_P, SYSREF_A_N	Input	SYSREF_P and SYSREF_N Inputs for CLK_A_P and CLK_A_N .

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 27. Pin Function Descriptions (8T8R Single-Ended ADC) (Continued)

Pin No.	Mnemonic	Type	Description
F20, G20	SYNCOUTB_B1_P, SYNCOUTB_B1_N	Input/output	Dual-Use Pins. Configure these two pins as differential JRx Link B1 synchronization output ports for the JESD204B interface or as two single-ended GPIO pins. These pins can provide differential 100Ω output impedance in LVDS mode. These pins are floating when unused.
F21, G21	SYNCOUTB_B0_P, SYNCOUTB_B0_N	Input/output	Dual-Use Pin. Configure these two pins as differential JRx Link B0 synchronization output ports for the JESD204B interface or as two single-ended GPIO pins. These pins can provide differential 100Ω output impedance in LVDS mode. These pins are floating when unused.
J19, K19	SYNCINB_B0_P, SYNCINB_B0_N	Input/output	Dual-Use Pin. Configure these two pins as differential JTx Link B0 synchronization input ports for the JESD204B interface or as two single-ended GPIO pins. These pins can provide differential 100Ω input impedance in LVDS mode. These pins are floating when unused.
J20, K20	SYNCINB_B1_P, SYNCINB_B1_N	Input/output	Dual-Use Pin. Configure these two pins as differential JTx Link B1 synchronization input ports for the JESD204B interface or as two Single-ended GPIO pins. These pins can provide differential 100Ω input impedance in LVDS mode. These pins are floating when unused.
Y19, AA19	SYNCINB_A0_N, SYNCINB_A0_P	Input/output	Dual-Use Pin. Configure these two pins as differential JTx Link A0 synchronization input ports for the JESD204B interface or as two single-ended GPIO pins. These pins can provide differential 100Ω input impedance in LVDS mode. These pins are floating when unused.
Y20, AA20	SYNCINB_A1_N, SYNCINB_A1_P	Input/output	Dual-Use Pin. Configure these two pins as differential JTx Link A1 synchronization input ports for the JESD204B interface or as two single-ended GPIO pins. These pins can provide differential 100 Ω input impedance in LVDS mode. These pins are floating when unused.
AC20, AD20	SYNCOUTB_A1_N, SYNCOUTB_A1_P	Input/output	Dual-Use Pin. Configure these two pins as differential JRx Link A1 synchronization output ports for the JESD204B interface or as two single-ended GPIO pins. These pins can provide differential 100Ω output impedance in LVDS mode. These pins are floating when unused.
AC21, AD21	SYNCOUTB_A0_N, SYNCOUTB_A0_P	Input/output	Dual-Use Pin: Configure these two pins as differential JRx Link A0 synchronization output ports for the JESD204B interface or as two single-ended GPIO pins. These pins can provide differential 100Ω output impedance in LVDS mode. These pins are floating when unused.
A24, A25	SRXB_1P, SRXB_1N	Input	JRx Lane Inputs, Data True and Complement.
A28, A29	SRXB_5P, SRXB_5N	Input	JRx Lane Inputs, Data True and Complement.
B26, B27	SRXB_3P, SRXB_3N	Input	JRx Lane Inputs, Data True and Complement.
B30, B31	SRXB_7P, SRXB_7N	Input	JRx Lane Inputs, Data True and Complement.
C24, C25	SRXB_0P, SRXB_0N	Input	JRx Lane Inputs, Data True and Complement.
C28, C29	SRXB_8P, SRXB_8N	Input	JRx Lane Inputs, Data True and Complement.
D26, D27	SRXB_2P, SRXB_2N	Input	JRx Lane Inputs, Data True and Complement.
D30, D31	SRXB_9P, SRXB_9N	Input	JRx Lane Inputs, Data True and Complement.
E28, E29	SRXB_10P, SRXB_10N	Input	JRx Lane Inputs, Data True and Complement.
F26, F27	SRXB_6P, SRXB_6N	Input	JRx Lane Inputs, Data True and Complement.
F30, F31	SRXB_11P, SRXB_11N	Input	JRx Lane Inputs, Data True and Complement.
G24, G25	SRXB_4P, SRXB_4N	Input	JRx Lane Inputs, Data True and Complement.
AC24, AC25	SRXA_4P, SRXA_4N	Input	JRx Lane Inputs, Data True and Complement.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 27. Pin Function Descriptions (8T8R Single-Ended ADC) (Continued)

Pin No.	Mnemonic	Type	Description
AD26, AD27	SRXA_6P, SRXA_6N	Input	JRx Lane Inputs, Data True and Complement.
AD30, AD31	SRXA_11P, SRXA_11N	Input	JRx Lane Inputs, Data True and Complement.
AE28, AE29	SRXA_10P, SRXA_10N	Input	JRx Lane Inputs, Data True and Complement.
AF26, AF27	SRXA_2P, SRXA_2N	Input	JRx Lane Inputs, Data True and Complement.
AF30, AF31	SRXA_9P, SRXA_9N	Input	JRx Lane Inputs, Data True and Complement.
AG24, AG25	SRXA_0P, SRXA_0N	Input	JRx Lane Inputs, Data True and Complement.
AG28, AG29	SRXA_8P, SRXA_8N	Input	JRx Lane Inputs, Data True and Complement.
AH26, AH27	SRXA_3P, SRXA_3N	Input	JRx Lane Inputs, Data True and Complement.
AH30, AH31	SRXA_7P, SRXA_7N	Input	JRx Lane Inputs, Data True and Complement.
AJ24, AJ25	SRXA_1P, SRXA_1N	Input	JRx Lane Inputs, Data True and Complement.
AJ28, AJ29	SRXA_5P, SRXA_5N	Input	JRx Lane Inputs, Data True and Complement.
DO NOT CONNECTS			
C15, C16, C17, E10, N12, P25, T24, T25, AE10, AG15, AG16, AG17	DNC	DNC	Do Not Connect. Leave floating.

[1] STXA_xP, STXA_xN, STXB_xP, STXB_xN, SRXA_xP, SRXA_xN, SRXB_xP, and SRXB_xN include 100Ω internal termination resistors.

TYPICAL PERFORMANCE CHARACTERISTICS

DAC

8GSPS

The data curves represent the average performance across all outputs. Vector scale = 0dBFS, unless otherwise noted. All data is measured on a laboratory evaluation board. Nominal supplies, sample rate = 8GSPS, f_{IQ_DATA} = 1.0GSPS, and JESD N' = 16 bit, with T_J = 65°C, unless otherwise noted.

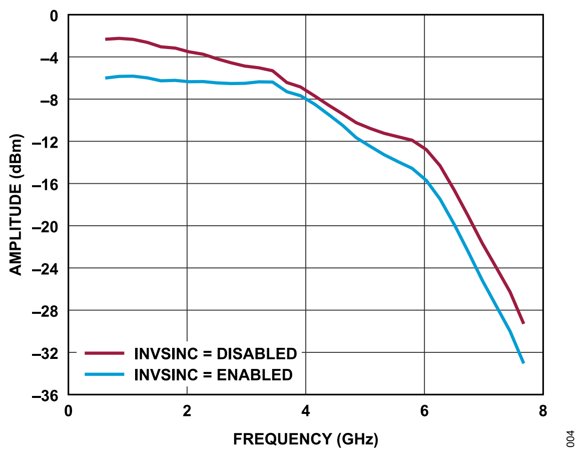

Figure 4. DAC Fundamental Amplitude vs. Fundamental Output Frequency, Across Inverse Sinc (InvSinc) Settings

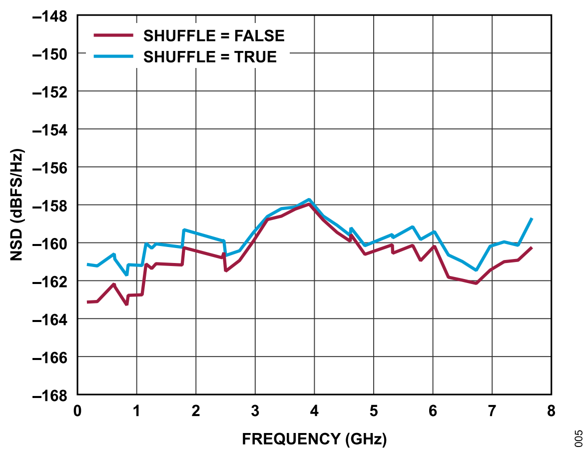

Figure 5. NSD (Measured at 500MHz Offset Above f_{OUT}) vs. Fundamental Output Frequency, Vector Amplitude Backoff = 0dBFS Across Shuffle Settings

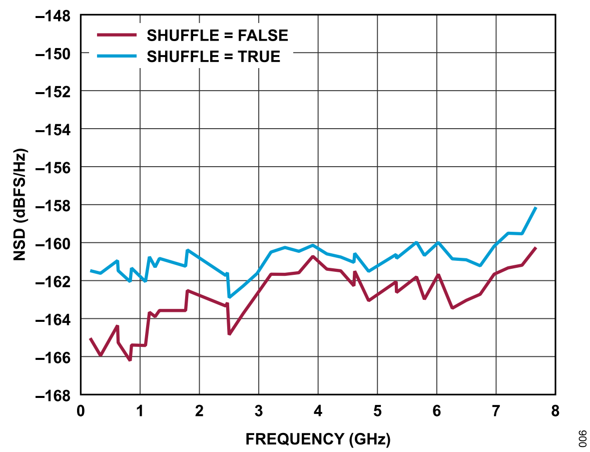

Figure 6. NSD (Measured at 500MHz Offset Above f_{OUT}) vs. Fundamental Output Frequency, Vector Amplitude Backoff = −7dBFS Across Shuffle Settings

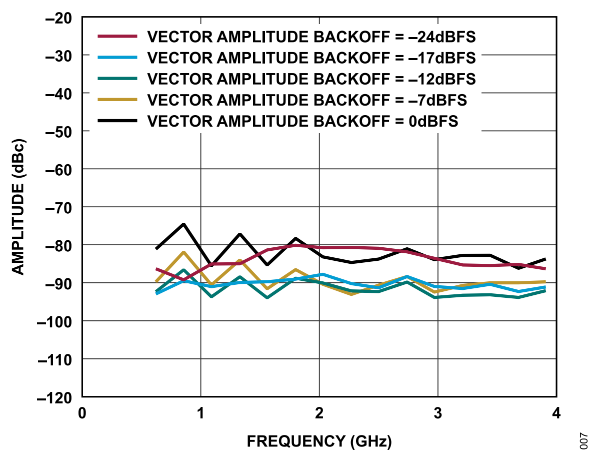

Figure 7. Second Harmonic Amplitude Referenced to the First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

TYPICAL PERFORMANCE CHARACTERISTICS

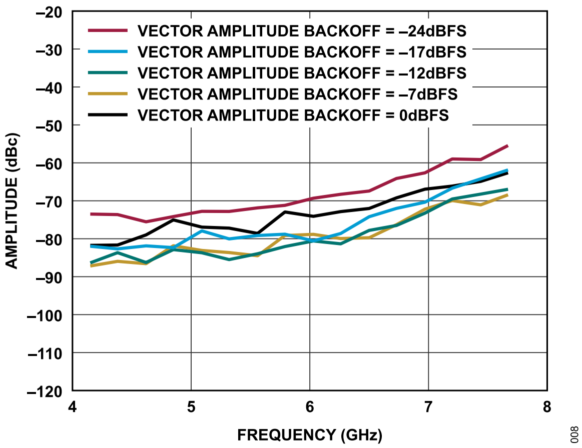

Figure 8. Second Harmonic Amplitude Referenced to the Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

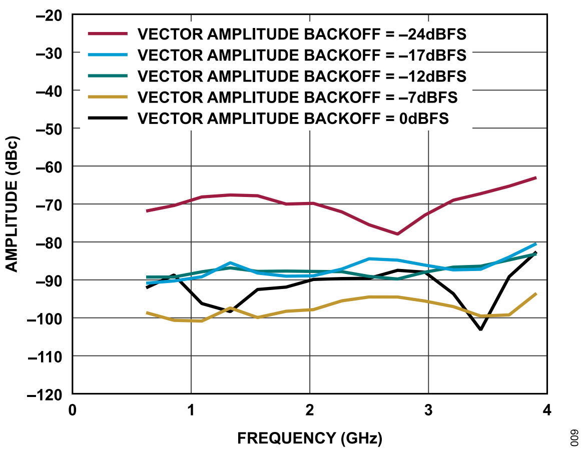

Figure 9. Third Harmonic Amplitude Referenced to the First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

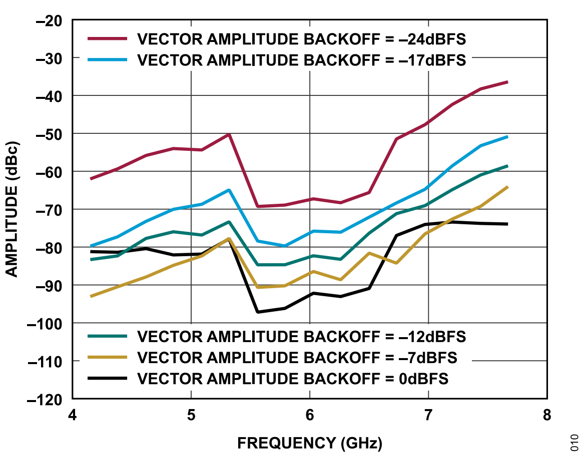

Figure 10. Third Harmonic Amplitude Referenced to the Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

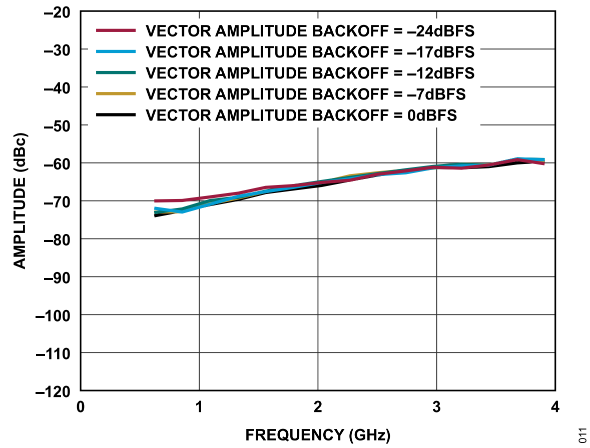

Figure 11. DDR Spur Amplitude Referenced to the First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

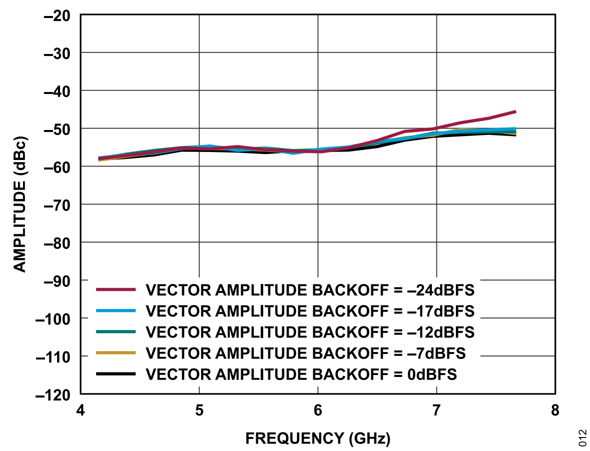

Figure 12. DDR Spur Amplitude Referenced to the Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

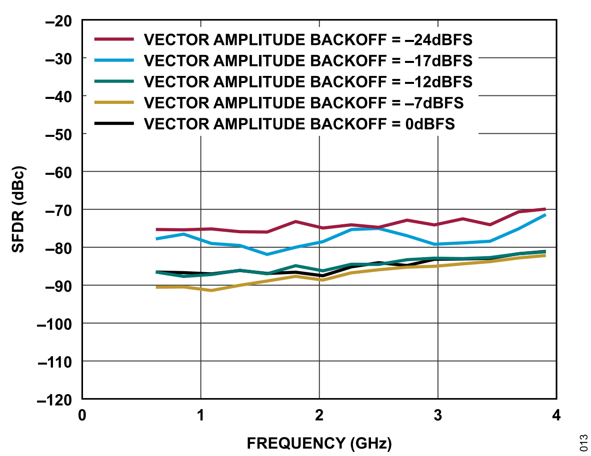

Figure 13. SFDR (Excluding Second and Third Harmonics and DDR Spur) Referenced to First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

TYPICAL PERFORMANCE CHARACTERISTICS

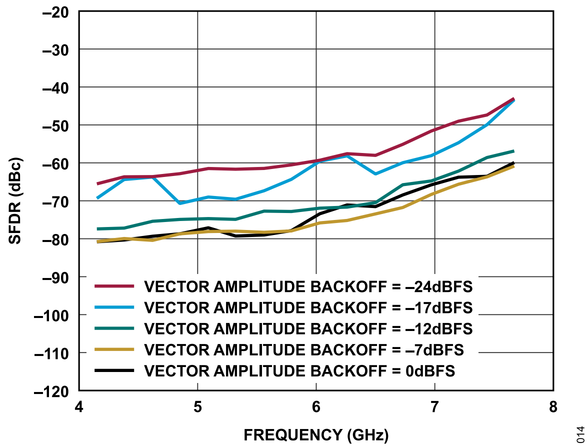

Figure 14. SFDR (Excluding Second and Third Harmonics and DDR Spur) Referenced to Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

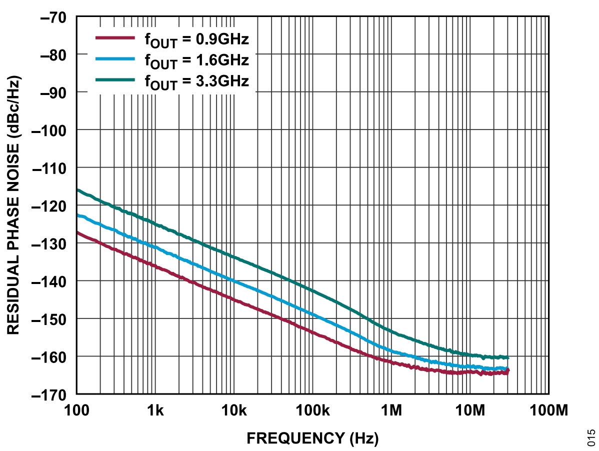

Figure 15. Residual Single Sideband Phase Noise vs. Frequency Offset When Using an Off-Chip Clock Source at Multiple Fundamental Output Frequencies (f_{OUT}), Excludes Phase Noise Contributions from the Off-Chip Clock Source

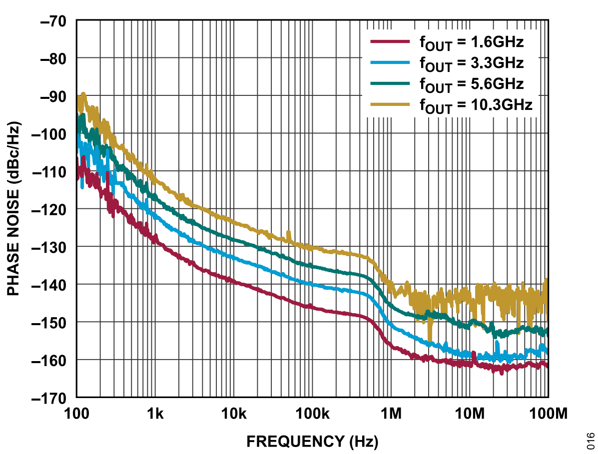

Figure 16. Single Sideband Phase Noise vs. Frequency Offset When Using an Off-Chip Clock Source at Multiple Fundamental Output Frequencies (f_{OUT}), Includes Phase Noise Contributions from the Off-Chip Clock Source

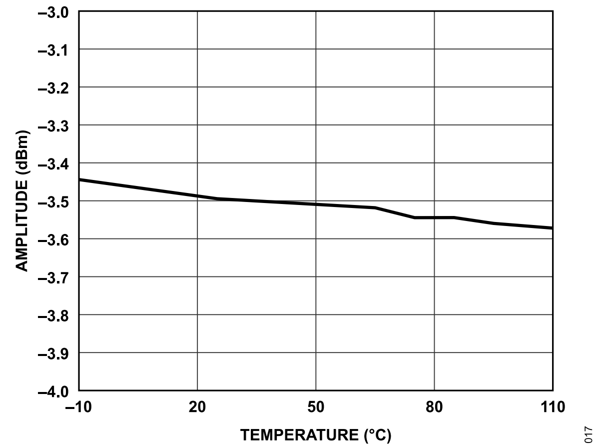

Figure 17. DAC Fundamental Amplitude vs. Junction Temperature when f_{OUT} = 1.9GHz, Vector Amplitude Backoff = 0dBFS

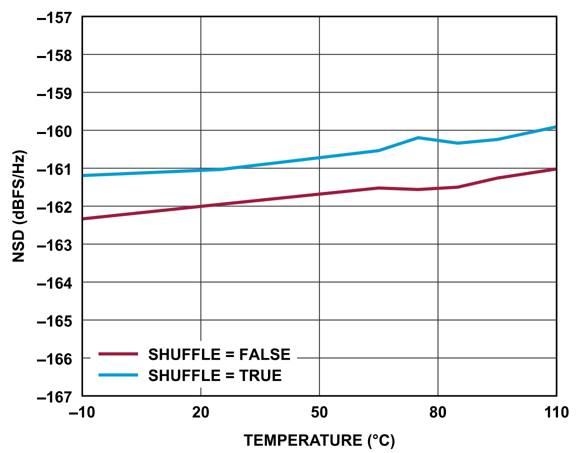

Figure 18. NSD (Measured at 500MHz Above f_{OUT}) vs. Junction Temperature when f_{OUT} = 1.9GHz, Vector Amplitude Backoff = 0dBFS

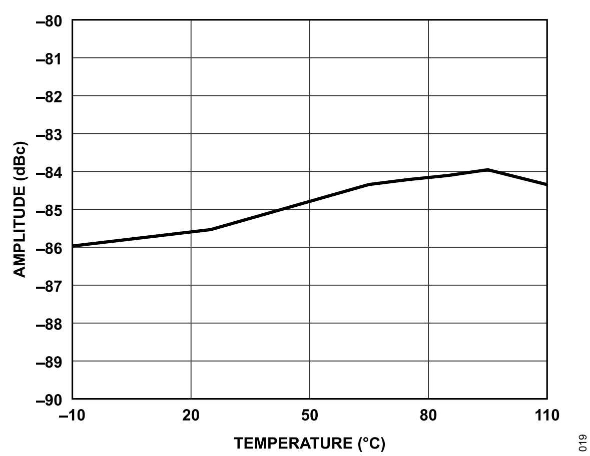

Figure 19. Second Harmonics Amplitude Referenced to the First Nyquist Zone vs. Junction Temperature when f_{OUT} = 1.9GHz

TYPICAL PERFORMANCE CHARACTERISTICS

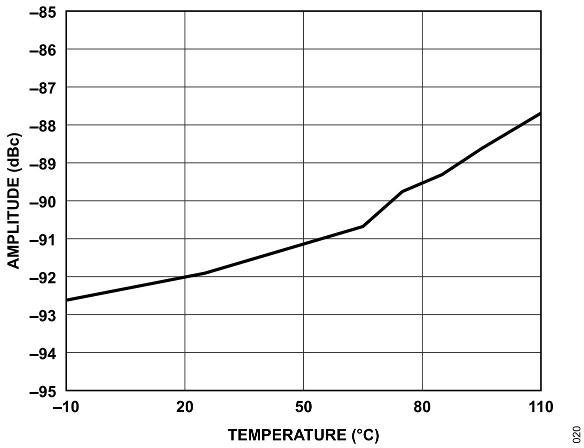

Figure 20. Third Harmonics Amplitude Referenced to the First Nyquist Zone vs. Junction Temperature when f_{OUT} = 1.9GHz

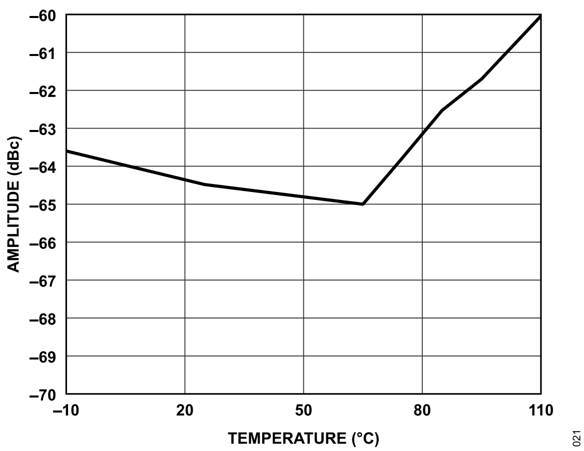

Figure 21. DDR Spur Amplitude Referenced to the First Nyquist Zone vs. Junction Temperature when f_{OUT} = 1.9GHz

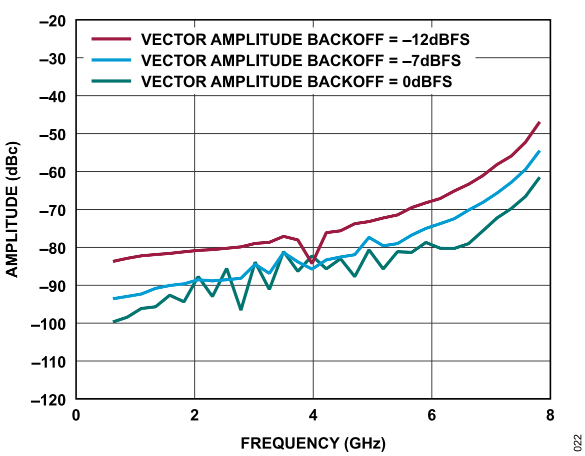

Figure 22. IMD3 Amplitude vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

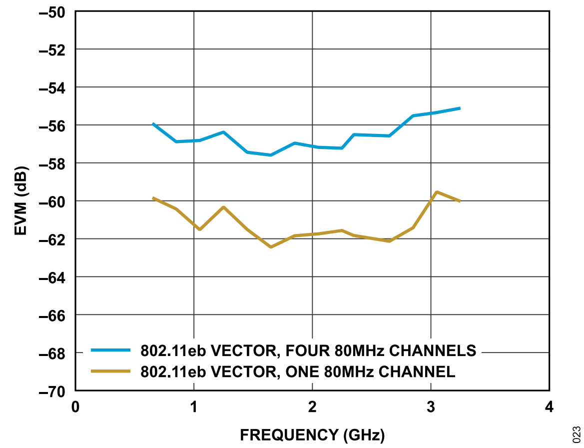

Figure 23. Error Vector Magnitude (EVM) vs. Carrier Frequency (Note That the 802.11eb Signal Vector Used for This Test Is a Common Test Signal Used to Benchmark EVM Performance; the Carrier Frequency and Channel Count During Testing Do Not Adhere to the 802.11be Specification as Published by IEEE, Whereas the Channel Bandwidth and Encoding Do)

TYPICAL PERFORMANCE CHARACTERISTICS

16GSPS

The data curves represent the average performance across all outputs. Vector scale = 0dBFS, unless otherwise noted. All data is measured on a laboratory evaluation board. Nominal supplies, sample rate = 16GSPS, f_{IQ_DATA} = 4.0GSPS, and JESD N' = 16 bit, with T_J = 65°C, unless otherwise noted.

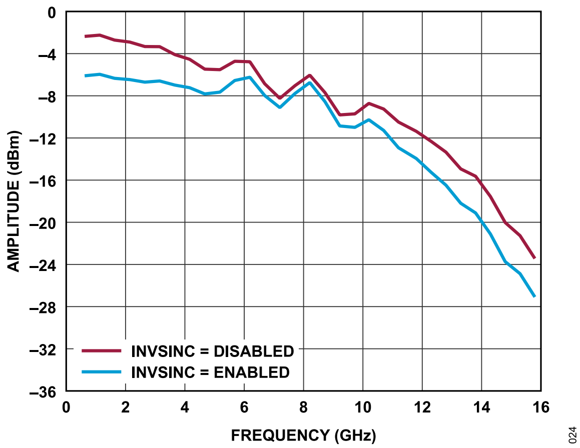

Figure 24. DAC Fundamental Amplitude vs. Fundamental Output Frequency, Across Inverse Sinc (InvSinc) Settings

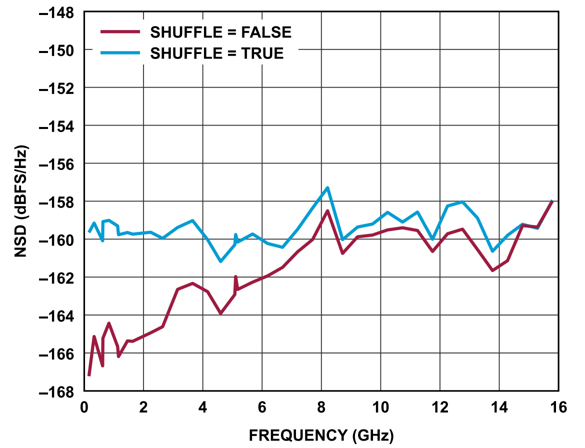

Figure 26. NSD (Measured at 500MHz Offset Above f_{OUT}) vs. Fundamental Output Frequency, Vector Amplitude Backoff = −7dBFS Across Shuffle Settings

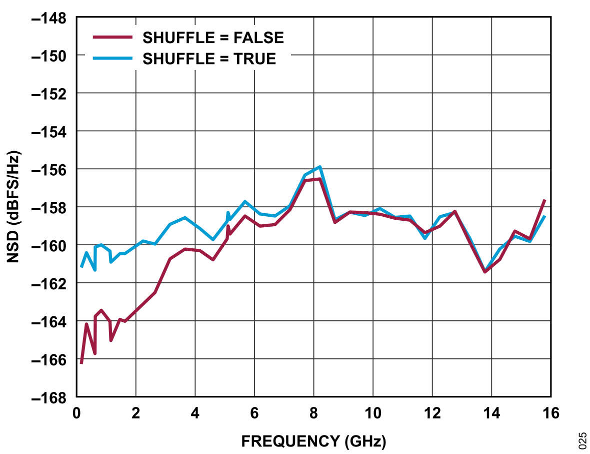

Figure 25. NSD (Measured at 500MHz Offset Above f_{OUT}) vs. Fundamental Output Frequency, Vector Amplitude Backoff = 0dBFS Across Shuffle Settings

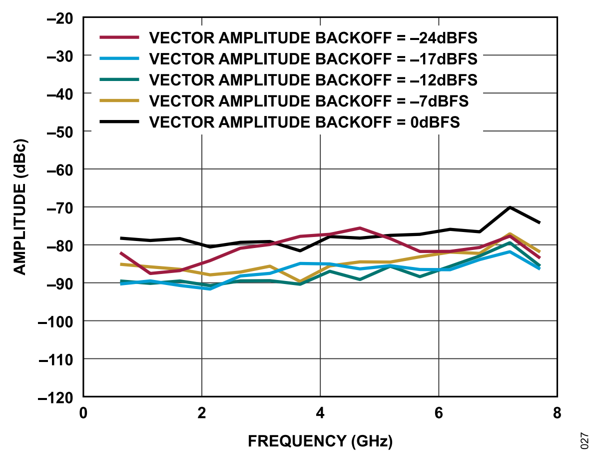

Figure 27. Second Harmonics Amplitude Referenced to the First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

TYPICAL PERFORMANCE CHARACTERISTICS

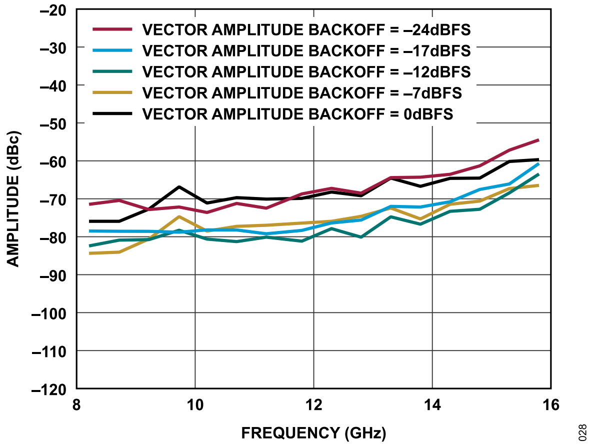

Figure 28. Second Harmonics Amplitude Referenced to the Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

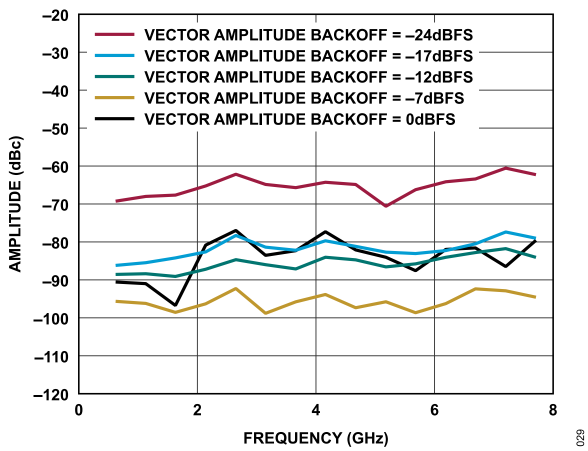

Figure 29. Third Harmonics Amplitude Referenced to the First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

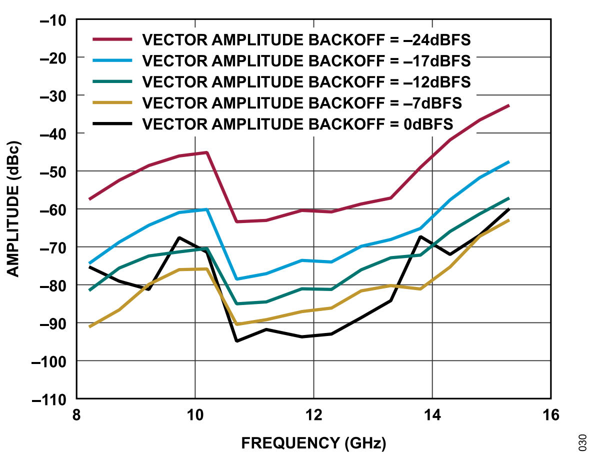

Figure 30. Third Harmonics Amplitude Referenced to the Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

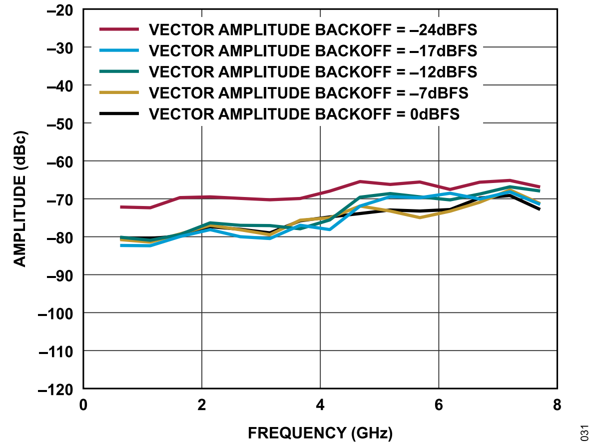

Figure 31. DDR Spur Amplitude Referenced to First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

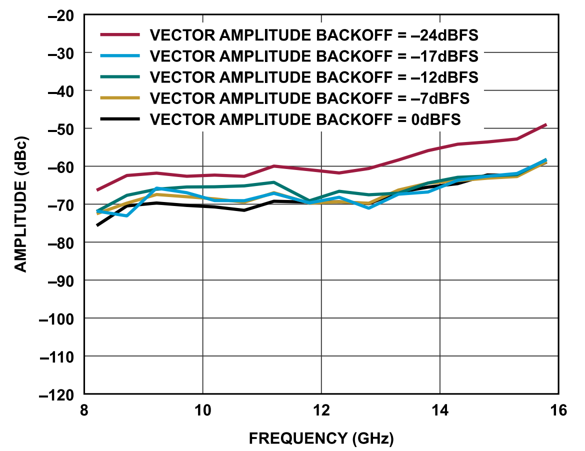

Figure 32. DDR Spur Amplitude Referenced to Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

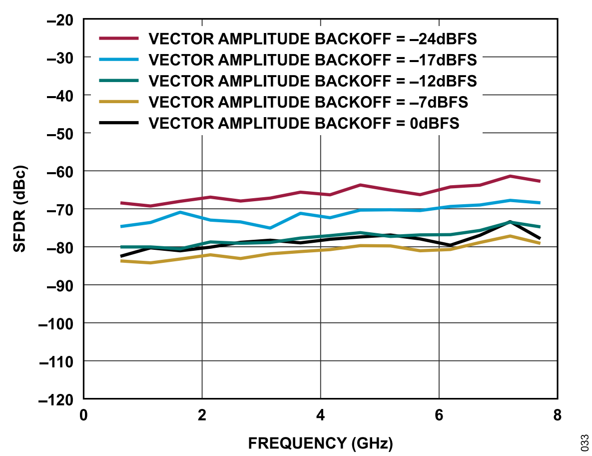

Figure 33. SFDR (Excluding Second and Third Harmonics and DDR Spur) Referenced to First Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

TYPICAL PERFORMANCE CHARACTERISTICS

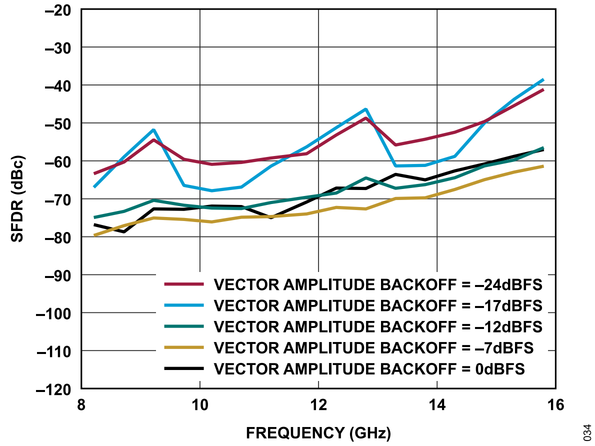

Figure 34. SFDR (Excluding Second and Third Harmonics and DDR Spur) Referenced to Second Nyquist Zone vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

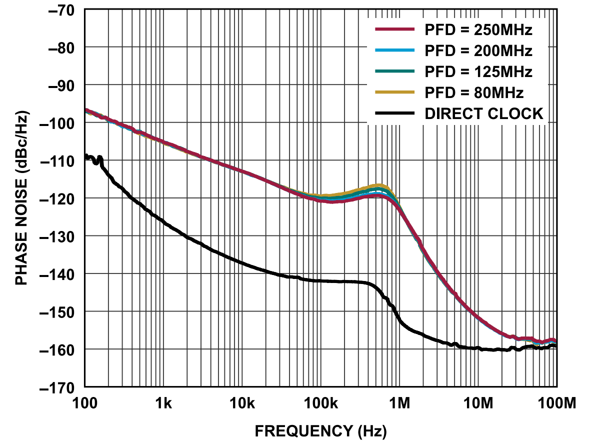

Figure 37. Single Sideband Phase Noise vs. Frequency Offset when Using the On-Chip PLL at Multiple Phase-Frequency Detector (PFD) Frequencies, f_{OUT} = 3.2GHz

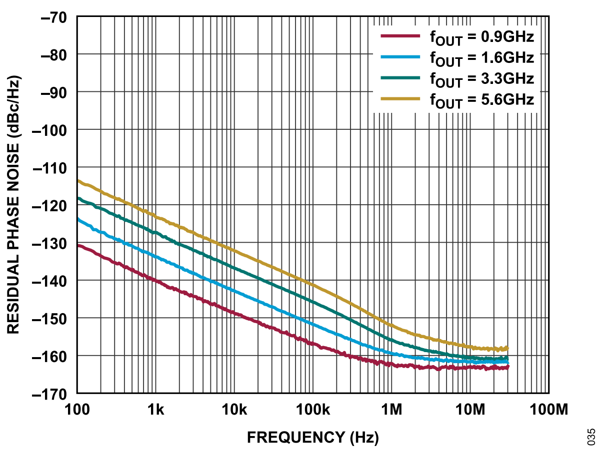

Figure 35. Residual Single Sideband Phase Noise vs. Frequency Offset when Using an Off-Chip Clock Source at Multiple Fundamental Output Frequencies (f_{OUT}), Excludes Phase Noise Contributions from the Off-Chip Clock Source

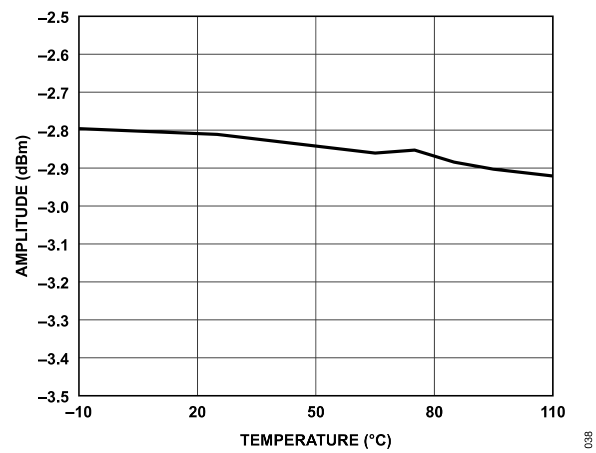

Figure 38. DAC Fundamental Amplitude vs. Junction Temperature when f_{OUT} = 1.9GHz

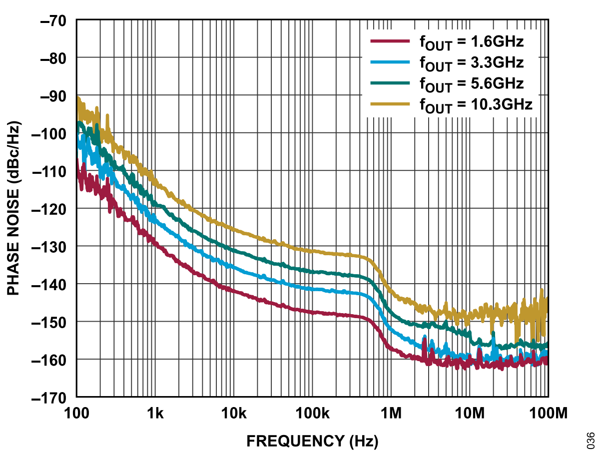

Figure 36. Single Sideband Phase Noise vs. Frequency Offset when Using an Off-Chip Clock Source at Multiple Fundamental Output Frequencies (f_{OUT}), Includes Phase Noise Contributions from the Off-Chip Clock Source

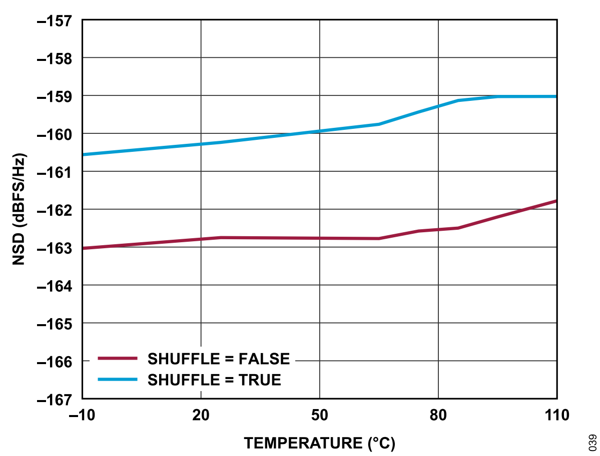

Figure 39. NSD (Measured at 500MHz Above f_{OUT}) vs. Junction Temperature, f_{OUT} = 1.9GHz, Vector Amplitude Backoff = 0dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

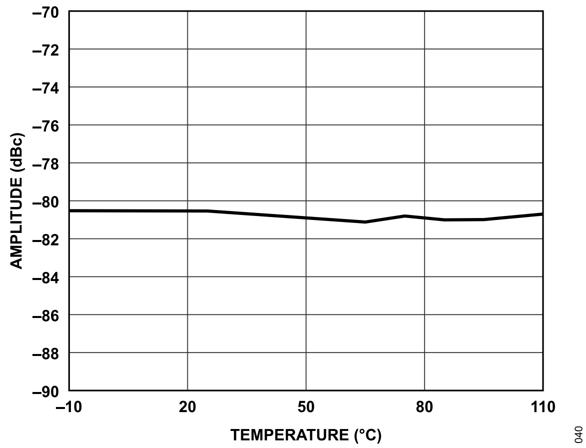

Figure 40. Second Harmonics Amplitude Referenced to the First Nyquist Zone vs. Junction Temperature when f_{OUT} = 1.9GHz

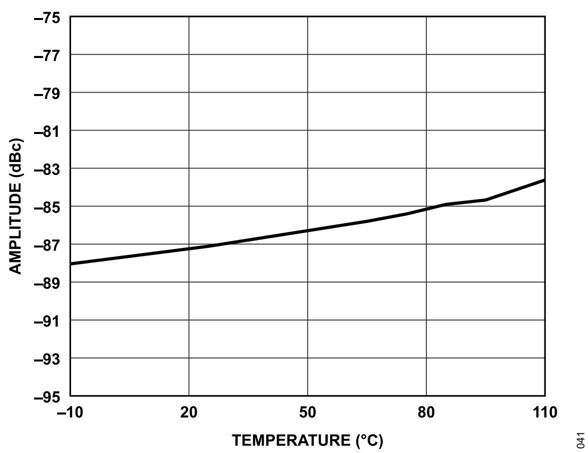

Figure 41. Third Harmonics Amplitude Referenced to the First Nyquist Zone vs. Junction Temperature when f_{OUT} = 1.9GHz

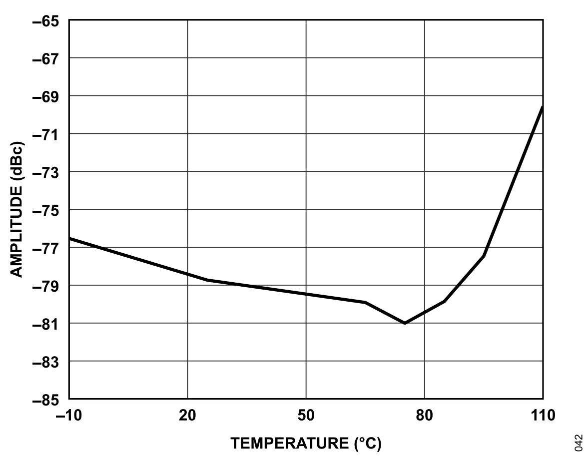

Figure 42. DDR Spur Amplitude Referenced to the First Nyquist Zone vs. Junction Temperature when f_{OUT} = 1.9GHz

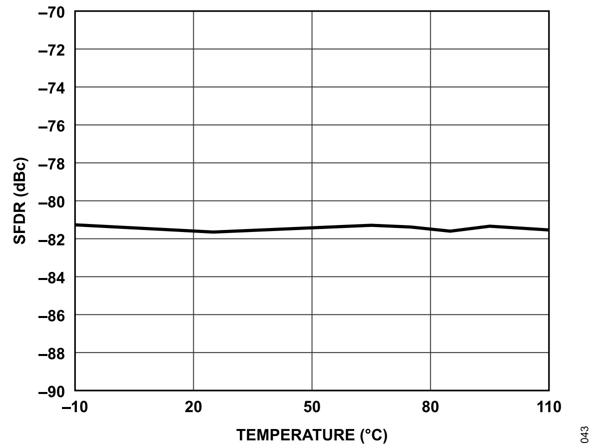

Figure 43. SFDR (Excluding Second and Third Harmonics and DDR Spur) Referenced to the First Nyquist Zone vs. Junction Temperature when f_{OUT} = 1.9GHz

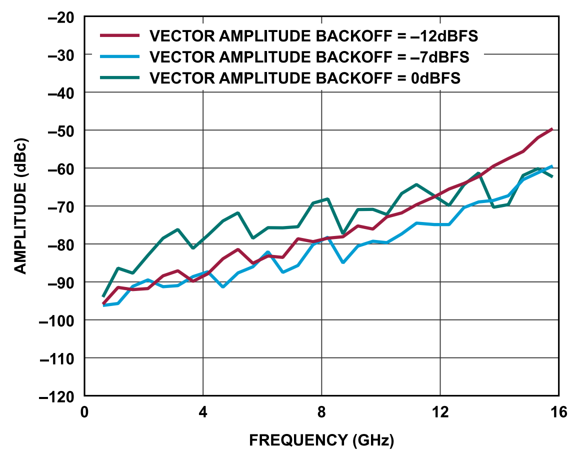

Figure 44. IMD3 Amplitude vs. Fundamental Output Frequency, Multiple Vector Amplitude Backoffs

TYPICAL PERFORMANCE CHARACTERISTICS

Sample Rate Sweep

Shuffle enabled, unless otherwise noted. Vector scale = 0dBFS, unless otherwise noted. Specifications represent the average of all eight DAC channels with the DAC I_{OUTFS} = 20mA, unless otherwise noted. Nominal supplies, unless otherwise noted. T_J = 65°C, unless otherwise noted.

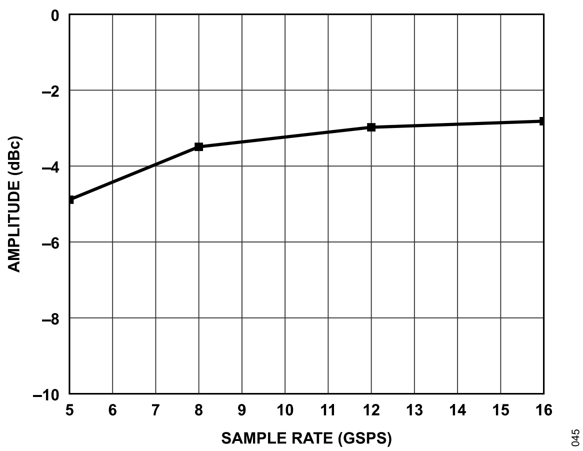

Figure 45. DAC Fundamental Amplitude vs. DAC Sample Rate, f_{OUT} = 1.9GHz

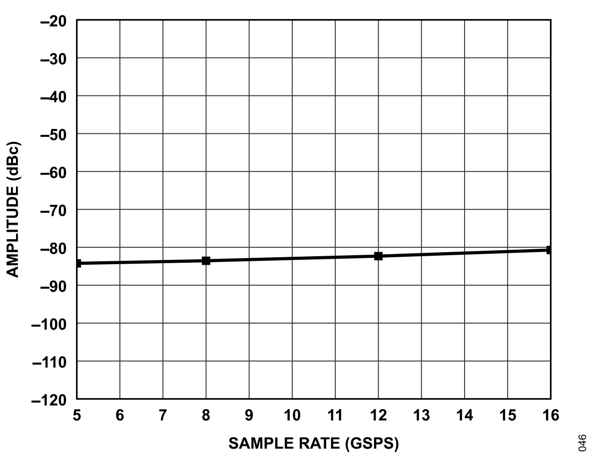

Figure 46. Second Harmonic Amplitude Referenced to First Nyquist Zone vs. DAC Sample Rate, f_{OUT} = 1.9GHz

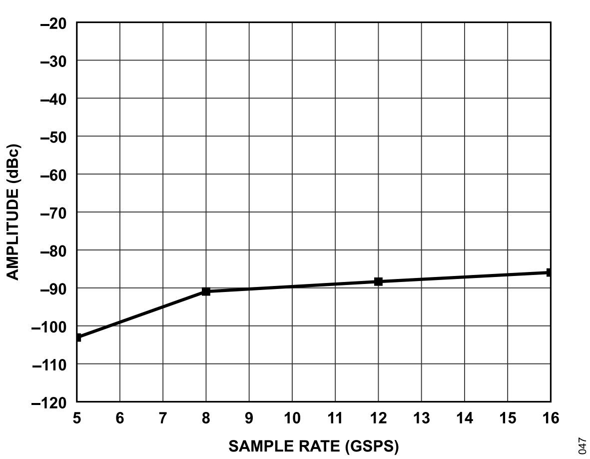

Figure 47. Third Harmonic Amplitude Referenced to First Nyquist Zone vs. DAC Sample Rate, f_{OUT} = 1.9GHz

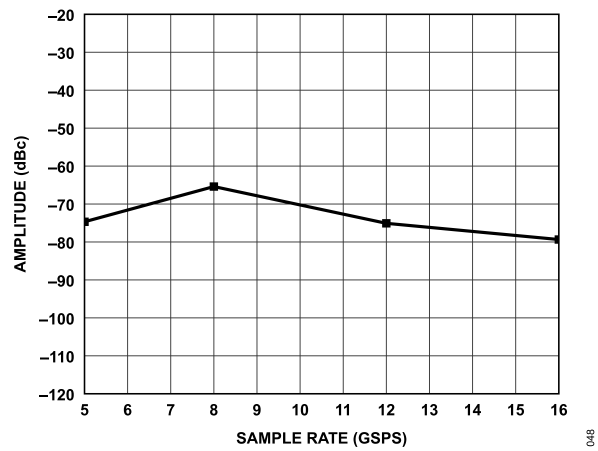

Figure 48. DDR Spur Amplitude Referenced to First Nyquist Zone vs. DAC Sample Rate, f_{OUT} = 1.9GHz

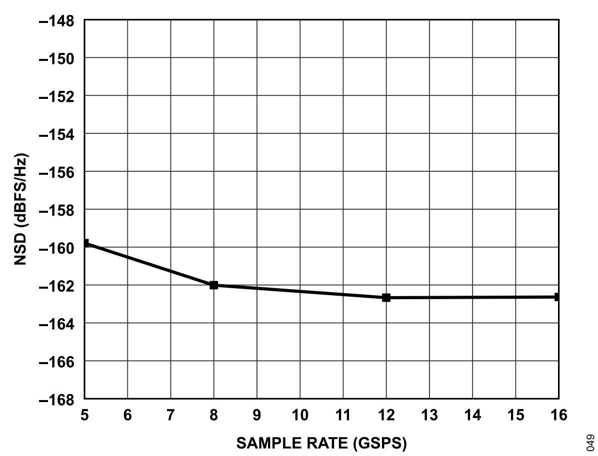

Figure 49. NSD Referenced to First Nyquist Zone vs. DAC Sample Rate, f_{OUT} = 1.9GHz

TYPICAL PERFORMANCE CHARACTERISTICS

ADC

8GSPS

Nominal supplies, sample rate = 8GSPS, and f_{IQ_DATA} = 1.0GSPS, unless otherwised noted. T_J = 65°C, unless otherwise noted. Analog input amplitude (A_{IN}) = −7dBFS and JESD N' = 16 bit, unless otherwise noted. The random mode of the ADC is enabled.

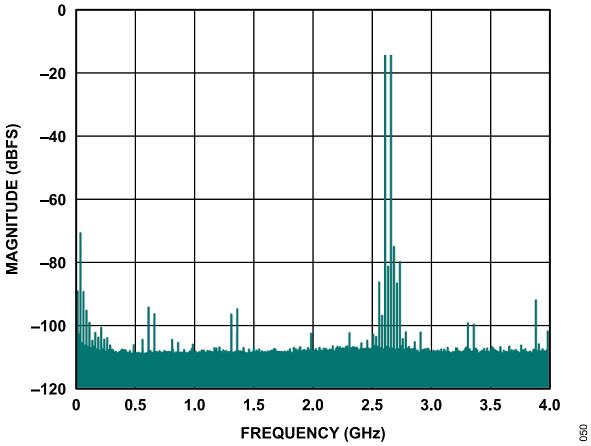

Figure 50. Two-Tone Fast Fourier Transform (FFT) at f_{IN} = 2.625GHz, CDDC and FDDC Bypassed

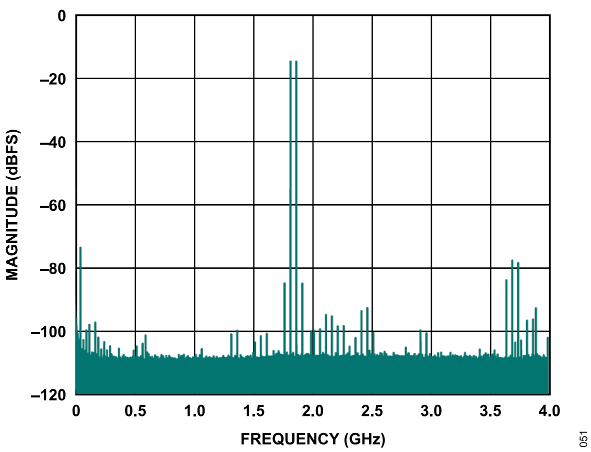

Figure 51. Two-Tone FFT at f_{IN} = 6.125GHz, CDDC and FDDC Bypassed

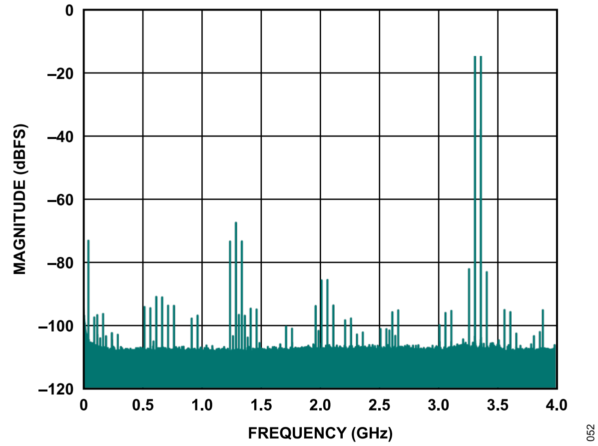

Figure 52. Two-Tone FFT at f_{IN} = 12.625GHz, CDDC and FDDC Bypassed

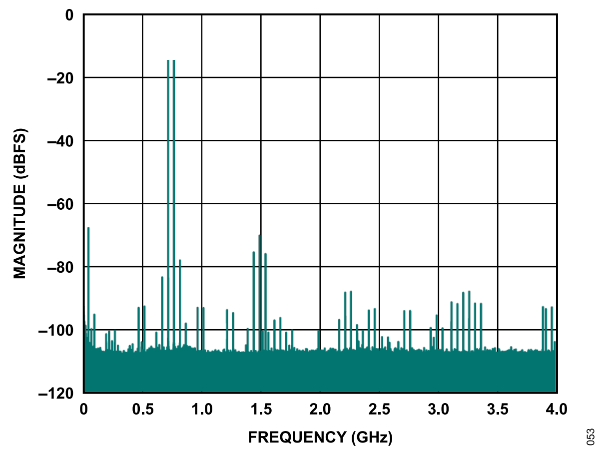

Figure 53. Two-Tone FFT at f_{IN} = 16.725GHz, CDDC and FDDC Bypassed

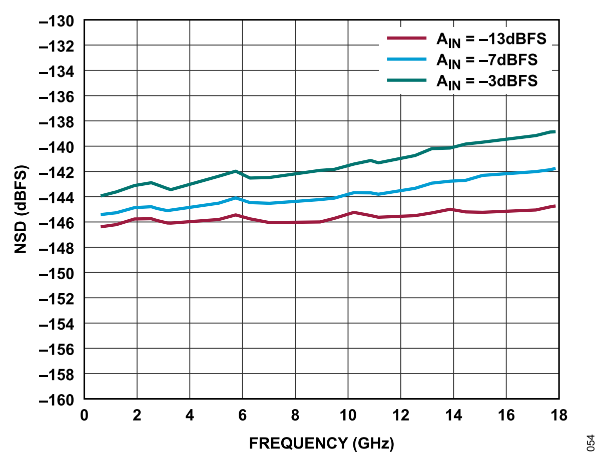

Figure 54. Single-Tone NSD vs. Frequency for Various A_{IN} Values

TYPICAL PERFORMANCE CHARACTERISTICS

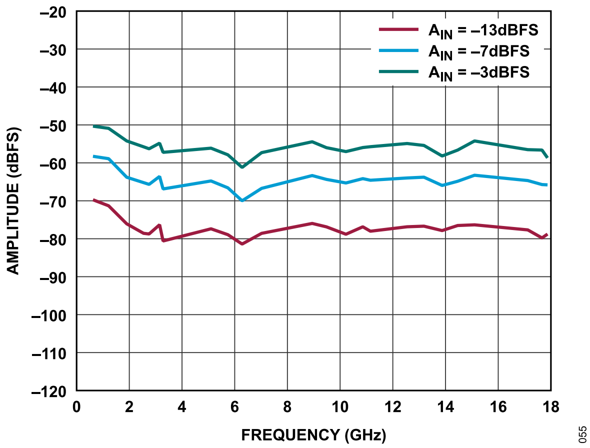

Figure 55. Single-Tone Second Harmonic Amplitude vs. Frequency for Various A_{IN} Values

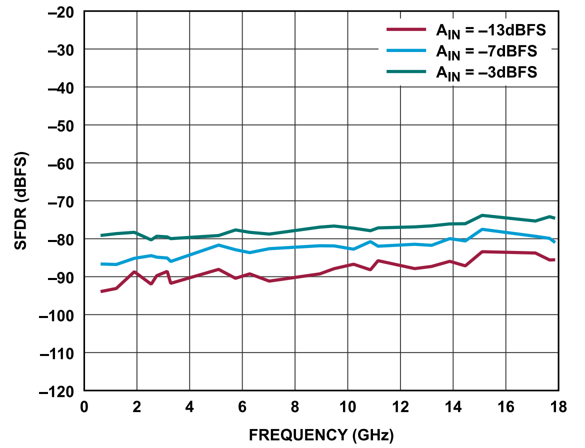

Figure 58. Single-Tone SFDR (Excluding Second and Third Harmonics and $f_S/2 - A_{IN}$) vs. Frequency for Various A_{IN} Values

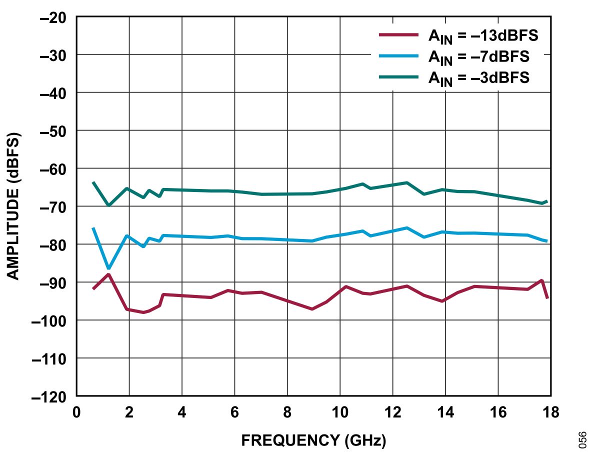

Figure 56. Single-Tone Third Harmonic Amplitude vs. Frequency for Various A_{IN} Values

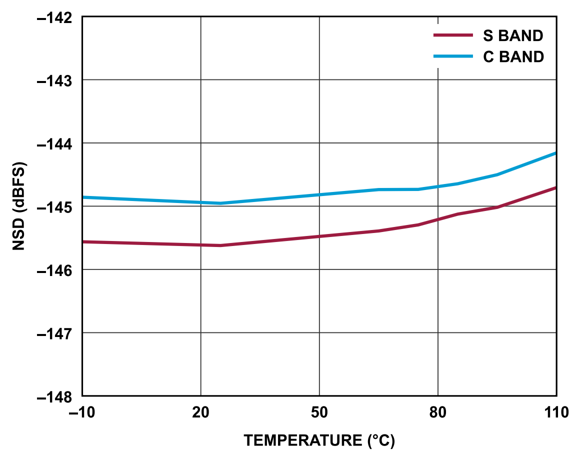

Figure 59. Single-Tone NSD vs. Junction Temperature Across Multiple IEEE Frequency Bands

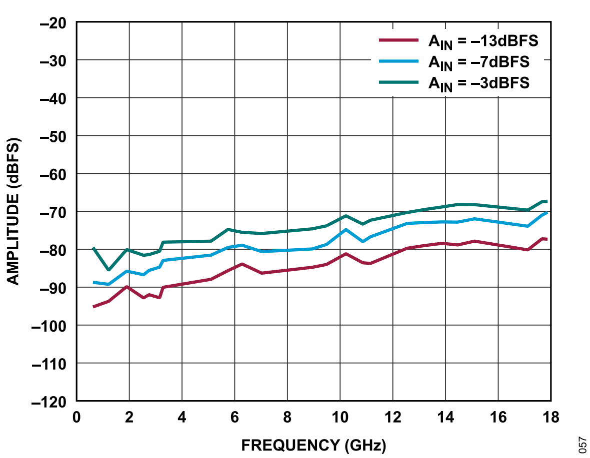

Figure 57. Single-Tone $f_S/2 - A_{IN}$ Spur Amplitude vs. Frequency for Various A_{IN} Values

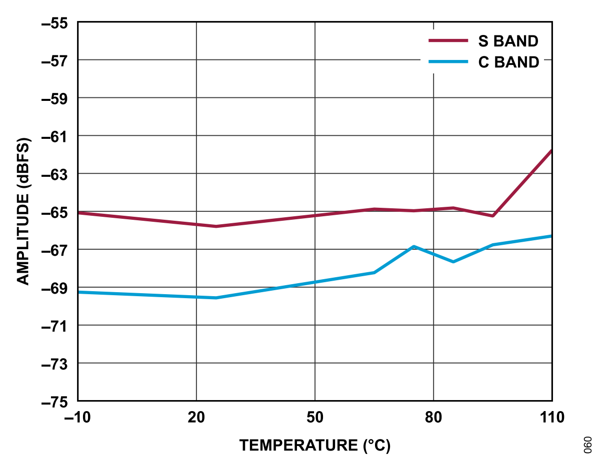

Figure 60. Single-Tone Second Harmonic Amplitude vs. Junction Temperature Across Multiple IEEE Frequency Bands

TYPICAL PERFORMANCE CHARACTERISTICS

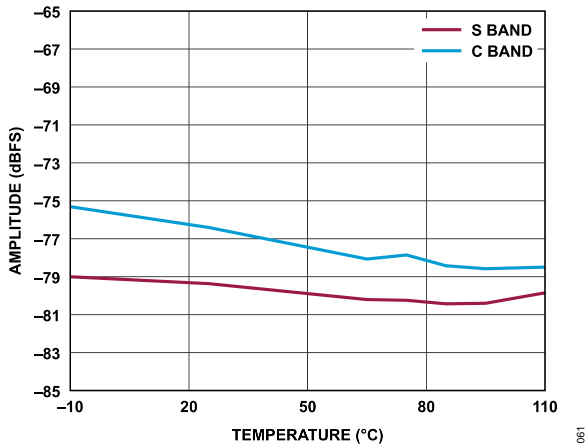

Figure 61. Single-Tone Third Harmonic Amplitude vs. Junction Temperature Across Multiple IEEE Frequency Bands

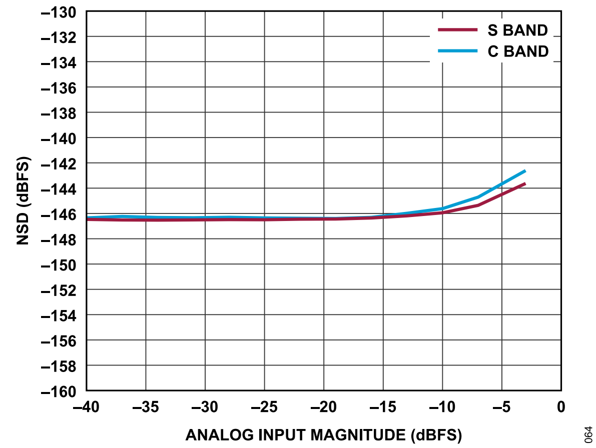

Figure 64. Single-Tone NSD vs. Analog Input Magnitude Across Multiple IEEE Frequency Bands

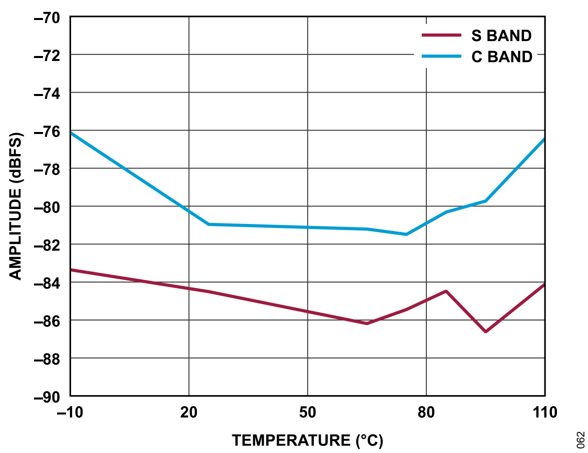

Figure 62. Single-Tone $f_S/2 - A_{IN}$ Spur Amplitude vs. Junction Temperature Across Multiple IEEE Frequency Bands

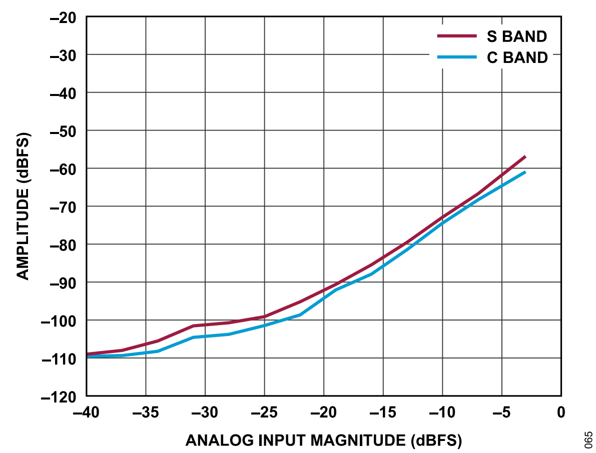

Figure 65. Single-Tone Second Harmonic Amplitude vs. Analog Input Magnitude Across Multiple IEEE Frequency Bands

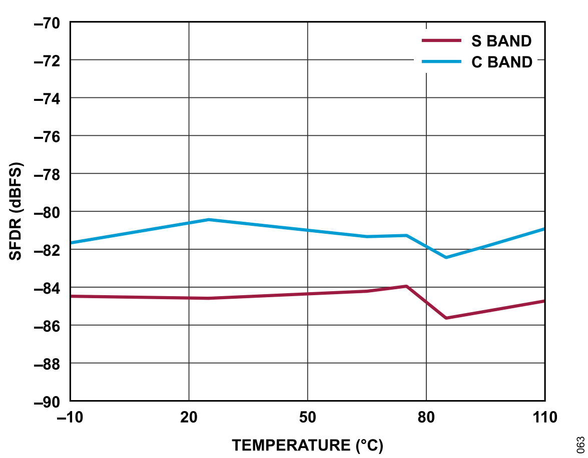

Figure 63. Single-Tone SFDR (Excluding Second and Third Harmonics and $f_S/2 - A_{IN}$) vs. Junction Temperature Across Multiple IEEE Frequency Bands

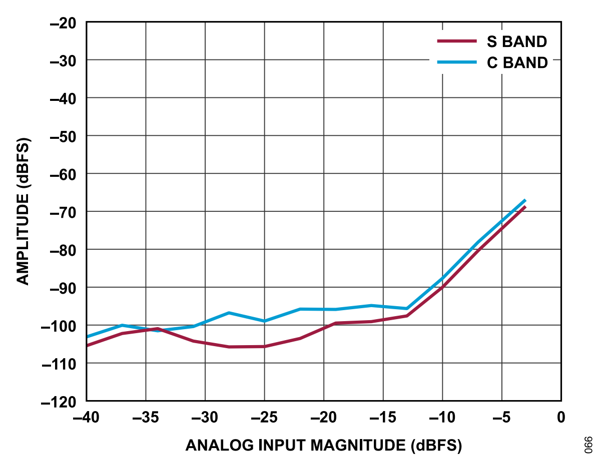

Figure 66. Single-Tone Third Harmonic Amplitude vs. Analog Input Magnitude Across Multiple IEEE Frequency Bands

TYPICAL PERFORMANCE CHARACTERISTICS

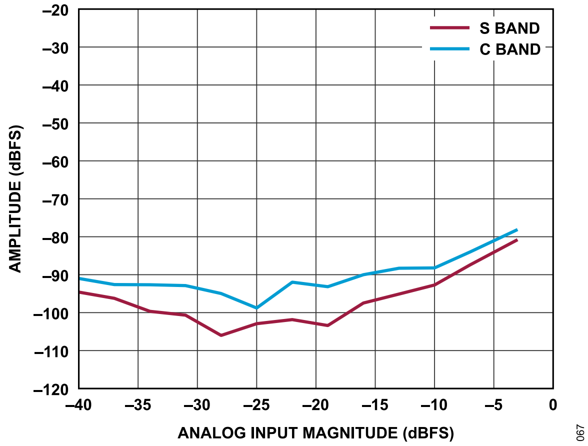

Figure 67. Single-Tone $f_S/2 - A_{IN}$ Spur Amplitude vs. Analog Input Magnitude Across Multiple IEEE Frequency Bands

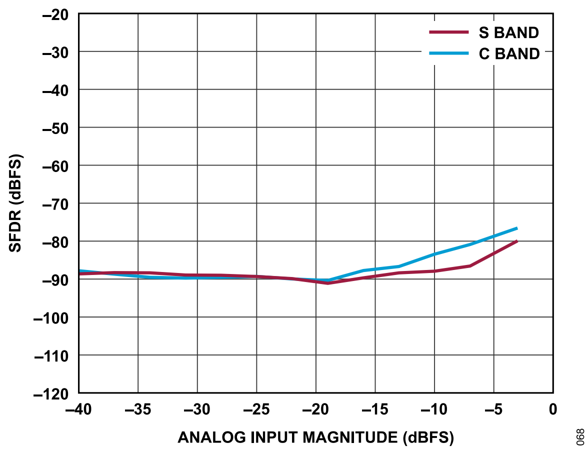

Figure 68. Single-Tone SFDR (Excluding Second and Third Harmonics and $f_S/2 - A_{IN}$) vs. Analog Input Magnitude Across Multiple IEEE Frequency Bands

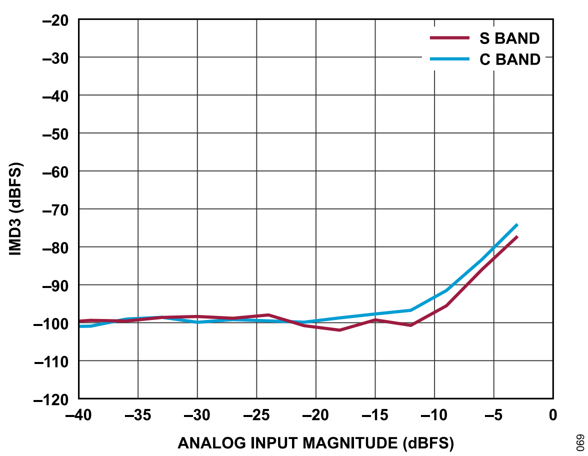

Figure 69. Two-Tone IMD3 vs. Analog Input Magnitude Across Multiple IEEE Frequency Bands

TYPICAL PERFORMANCE CHARACTERISTICS

Sample Rate Sweep

Nominal supplies and T_J = 65°C, unless otherwise noted. A_{IN} = −7dBFS, unless otherwise noted.

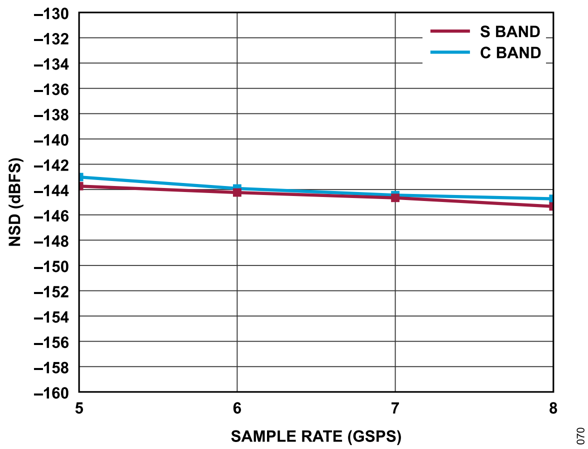

Figure 70. Single-Tone NSD vs. ADC Sample Rate Across Multiple IEEE Frequency Bands

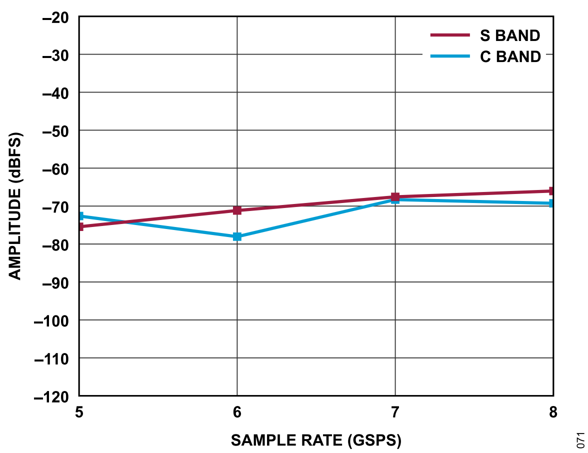

Figure 71. Single-Tone Second Harmonic Amplitude vs. ADC Sample Rate Across Multiple IEEE Frequency Bands

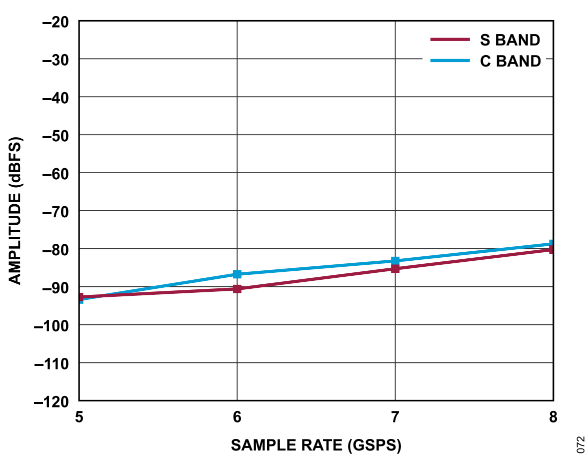

Figure 72. Single-Tone Third Harmonic Amplitude vs. ADC Sample Rate Across Multiple IEEE Frequency Bands

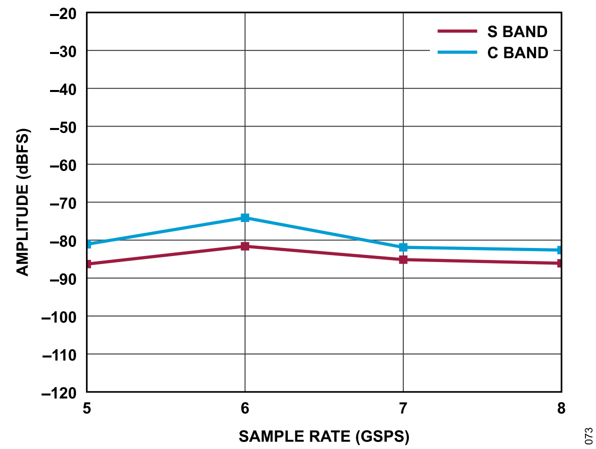

Figure 73. Single-Tone $f_S/2 - A_{IN}$ Spur Amplitude vs. ADC Sample Rate Across Multiple IEEE Frequency Bands

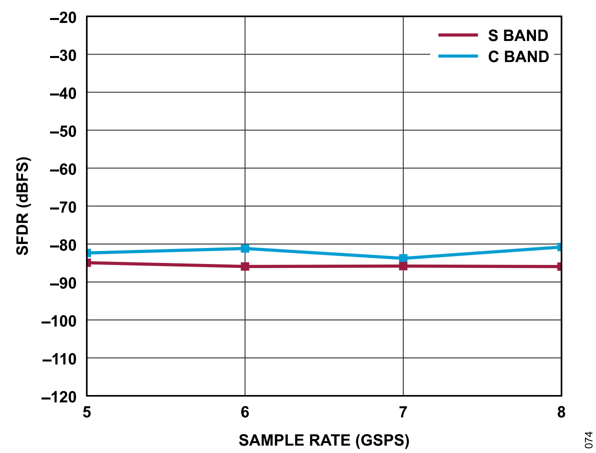

Figure 74. Single-Tone SFDR (Excluding Second and Third Harmonics and $f_S/2 - A_{IN}$ Spur) vs. ADC Sample Rate Across Multiple IEEE Frequency Bands

TYPICAL PERFORMANCE CHARACTERISTICS

POWER CONSUMPTION ACROSS TEMPERATURE

Nominal supplies. DAC sample rate = 16GSPS and ADC sample rate = 8GSPS with a f_{IQ_DATA} = 1.0GSPS. T_J = 65°C, unless otherwise noted.

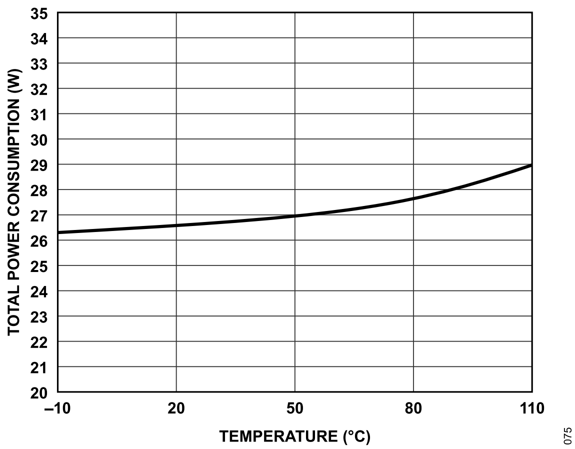

Figure 75. Total Power Consumption vs. Junction Temperature

THEORY OF OPERATION

The AD9088 is a highly integrated RF, mixed signal front-end (MxFE) that features eight, 16-bit, 16GSPS DAC cores and eight, 12-bit, 8GSPS ADC cores (8T8R). Both ADC and DAC cores are differential broadband cores featuring an on-chip buffer input and output with a 50Ω termination.

Each AD9088 ADC port features an integrated, on-chip balun for single-ended ADC input.

These high-speed data converter cores feature superior dynamic range performance, such as:

- Single-ended ADC AC performance at 8GSPS
  - Full-scale input voltage: 500mV p-p (−1.0dBm)
  - NSD: −146.4dBFS/Hz at −20dBFS
  - HD2 and HD3: −60dBFS and −78dBFS at −7dBFS for the L band, respectively
  - HD2 and HD3: −65dBFS and −78dBFS at −7dBFS for the X band, respectively
- DAC AC performance at 16GSPS
  - Full-scale output power: −2.9dBm and −11.4dBm for the L band and X band, respectively
  - NSD (shuffling disabled): −165dBFS/Hz and −161dBFS/Hz at −7dBFS for the L band and X band, respectively
- DAC AC performance at 8GSPS
  - Full-scale output power: −3.2dBm and −6.8dBm for the L band and S band, respectively
  - NSD (shuffling disabled): −163dBFS/Hz and −160dBFS/Hz at −7dBFS for the L band and C band, respectively

Due to the wide analog bandwidth and multiband capabilities of the AD9088, the DAC AC performance is characterized in both the first and second Nyquist zones. These characterizations are based on the following formulas:

$$HD_{N\_REAL} = (\mathrm{N} \times f_{OUT}) \bmod \mathrm{f}_{DAC}$$

$$HD_{N\_FOLDED} = (f_{DAC} - \mathrm{N} \times \mathrm{f}_{OUT}) \bmod \mathrm{f}_{DAC}$$

$$HD_{N,\ FIRST\ NYQUIST} = \left(\mathrm{x} \in \mathrm{HD}_{N\_REAL}, HD_{N\_FOLDED}: 0 < \mathrm{x} < \frac{f_{DAC}}{2}\right)$$

$$HD_{N,\ SECOND\ NYQUIST} = \left(\mathrm{x} \in \mathrm{HD}_{N\_REAL}, \mathrm{HD}_{N\_FOLDED}: \frac{f_{DAC}}{2} < \mathrm{x} < \mathrm{f}_{DAC}\right)$$

where:
HD_{N_REAL} is the frequency location of the real Nth-order harmonics of the DAC.
N is the integer.
HD_{N_FOLDED} is the frequency location of the folded Nth-order harmonics of the DAC.$HD_{N,\ FIRST\ NYQUIST}$ is the frequency location of the real Nth-order harmonics referenced to the first Nyquist zone.
x is the number as specified in the formula.
$HD_{N,\ SECOND\ NYQUIST}$ is the frequency location of the real Nth-order harmonics referenced to the second Nyquist zone.

The transmit and receive digital datapaths are highly configurable and support a wide range of single-band and multiband applications with varying RF bandwidth requirements. The AD9088 features advanced multichip synchronization capabilities to ensure sample accurate pipeline delays between ADCs and DACs on the same chip as well as between multiple chips. The AD9088 transmit and receive datapaths consist of eight main datapaths in support of wideband signals and 16 channelizers in support of narrower band signals. For multiband applications with wide separation between RF bands, the channelizers can be used to process the individual RF bands to reduce the overall complex data rate required to support narrow noncontiguous bands. Both the main and channelizer datapath stages offer flexible interpolating and decimation factors to allow a more manageable data interface rate aligned to the actual signal bandwidth requirements. The NCO of each stage can be independently tuned for the flexibility of frequency placement.

These versatile digital features are available to support a wide range of configurations during operation:

- Supports real or complex digital data (8-, 12-, or 16-bit)
- Configurable DDC and DUC
  - 16 fine complex DUCs and 8 coarse complex DUCs
  - 16 fine complex DDCs and 8 coarse complex DDCs
  - Option to bypass fine and coarse DUC and DDC
  - DUC and DDC alias rejection
  - >85dB for interpolation filters and >100dB for decimation filters
  - Coarse interpolation ratios available: 1×, 2×, 3×, 4×, 6×, 8×, or 12×
  - Coarse decimation ratios available: 1×, 2×, 3×, 4×, 6×, or 12×
  - Fine interpolation and decimation ratios available: 1×, 2×, 4×, 8×,16×, 32×, or 64×
  - Rate change programmable from 1× to 2×
- 48-bit fine tuning word and 32-bit course tuning word
- Programmable finite impulse response (FIR) filter for transmit and receive
  - Full converter rate, 32-tap programmable finite impulse response (PFIR) filter
  - Supports real, half complex, and complex modes
- 2.5GSPS maximum data rate, 16-tap complex FIR filter
  - Supports 128 taps in zero sparse mode
- Dynamic configuration through SPI, HSCI, or GPIO
- Course numerically controlled oscillator (CNCO) and fine numerically controlled oscillator (FNCO) fast frequency hopping
- Complex finite impulse response (CFIR) and programmable FIR (PFILT) profiles hopping
- CDDC decimation and CDUC interpolation are reconfigurable at run time (dynamic reconfiguration), 1× to 12×
- CDDC, CDUC, FDDC, and FDUC reconfigured between multiple decimation and interpolation ratios on the fly

THEORY OF OPERATION

- Interface
  - SPI: maximum SCLK rate of 50MHz
  - HSCI: maximum rate of 1.6Gbps in DDR mode
  - JESD204B and JESD204C: 16Gbps and 28.21Gbps
  - 24 lanes for receive and 24 lanes for transmit
- Receive automatic gain control (AGC) support
- Fast detect with low latency for fast AGC
- Signal monitor for slow AGC
- Power amplifier downstream protection circuitry
- Additional digital features are listed in the UG-2300 Device User Guide.

APPLICATIONS INFORMATION

Refer to the UG-2300 Devices User Guide for more information on the device initialization and additional applications information.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
BP-899-3	BGA_ED	899-Ball Ball Grid Array, Thermally Enhanced

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
AD9088BBPZ-MX-SE-SW5	−40°C to +110°C	899-Ball BGA_ED, AD9088 MxFE with Single-Ended ADC Inputs, CDDC, CDUC, FDDC, FDUC, Fast Frequency Hopping NCOs, PFILT, CFIR, Dynamic Reconfiguration, Loopbacks, FFT Sniffer, and Eight DACs and ADCs	BP-899-3

[1] Z = RoHS Compliant Part.

[2] See the Recommended Operating Conditions section for the specified operating T_J.