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APPLICATION NOTE

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# Stability and Transient Analysis of the Miller-Compensated Linear Regulators on the ADP3178

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Analog Devices' power management group has been in the desktop computer VRM controller market since the mid-90s. The ADP3158 programmable synchronous buck converter was positioned to fit into designs conforming to Intel's VRM 8.4 specifications. Designers typically used the ADP3158's buck converter for the CPU core switching supply and its two integrated fixed linear regulators to generate additional system voltages. In one major application, the ADP3158 linear regulators were used for generating a 2.5 V, 4.3 A DDR VDDQ supply and the 1.5 V, 1.5 A GTL supply. In order to generate the 1.5 V supply, designers used the 1.8 V linear regulator, driving its inverting input with the output of the 2.5 V regulator through an $R_f/R_{in}$ ratio of 3/7:

$$1.8\left(10/7\right)-2.5\left(3/7\right)=1.5\ V$$

This approach added a minor tolerance error and noise component to the resultant 1.5 V supply. Additional compensation was added to control loop disturbances initially thought to be sympathetic to the frequency of the switching supply. Unfortunately, these techniques did not optimize performance of both the loop stability and overall transient response. Design using the ADP3178 resolves these issues. The on-board references of the ADP3178 are now based on a 1.0 V reference versus the 1.8 V and 2.5 V references on the ADP3158.

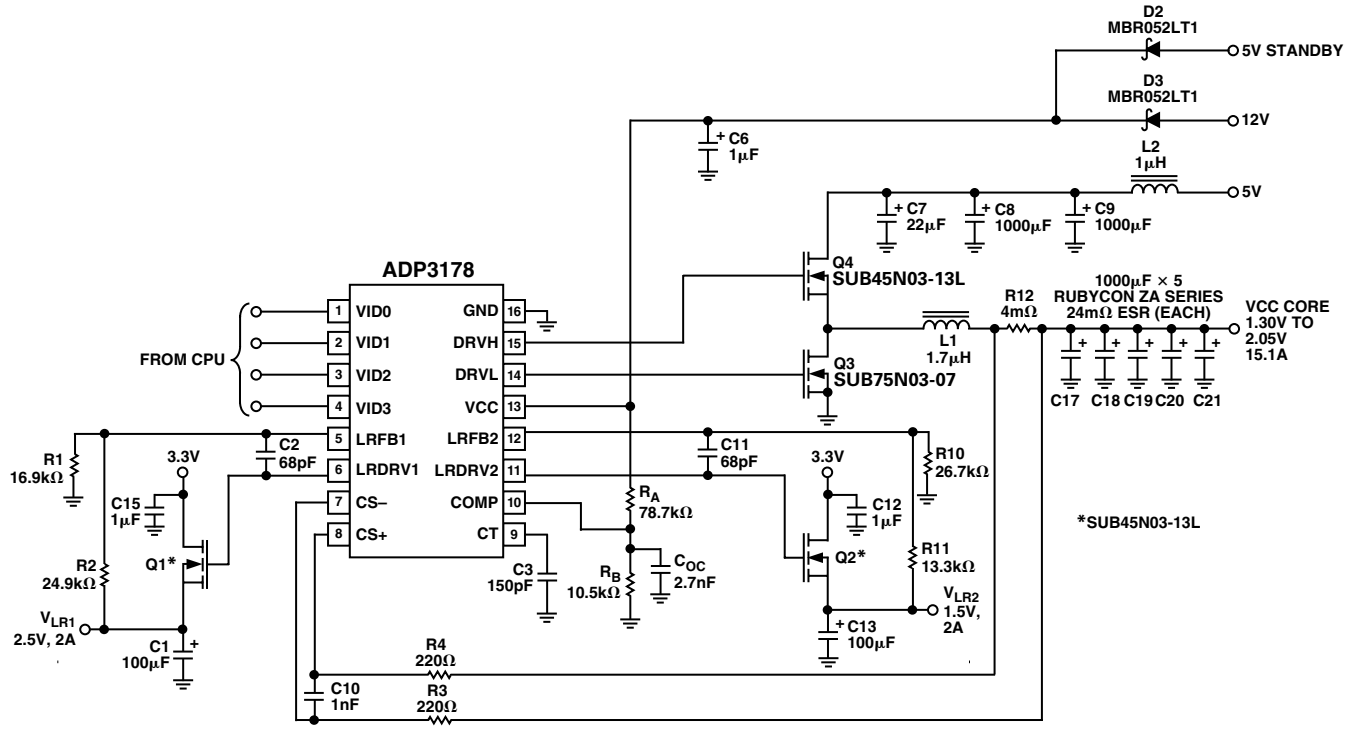


*Figure 1. Complete Implementation of the ADP3178*

Figure 1 shows a complete implementation of the ADP3178. Whereas the ADP3158 linear regulators use a fixed 10 kΩ resistor, the ADP3178 uses voltage dividers in the feedback. Equations 32 and 33 of the ADP3178 data sheet provide the calculations for these resistor sizes. Figure 1 shows standard 1% resistors that approximate a 10 kΩ equivalent for both 2.5 V and 1.5 V supplies. The output voltage can be easily set from 1.0 V to within $V_{ds}$ (for the required load current) from the supply tied to the drain of the external N-channel MOSFET. In addition, the lower on-board reference voltages on the ADP3178 versus the ADP3158 allow for better noise immunity for sub 1.8 V output voltage requirements.

Miller compensation is used for the ADP3178 design. The open-loop gain, $A_V$, of the linear regulator amplifiers on the ADP3178 from simulation is approximately 450 V/V (see Figure 2). Taking advantage of this gain, a relatively small compensation capacitor can be placed in the feedback of the linear regulator amplifier from LRFB to LRDRV. This capacitor, along with the parallel combination of the resistive voltage divider used to set the output voltage, sets the dominant pole for the linear regulator loop via the equation:

$$P_d = 1 / \left(2 \times \pi \times \left(\left(C_m \times A_V\right) + C_g\right) \times R_f\right)$$

where $C_m$ is the Miller compensation capacitor, $A_V$ is the open-loop gain of the linear regulator amplifier, $C_g$ is the MOSFET gate capacitance (2.7 nF for the SUB45N03-13L), and $R_f$ is $R_1 \| R_2$ (the resistors used in the voltage divider).

The dominant pole location should be set to roll off the open-loop gain of the amplifier to 0 dB at approximately the same point as the second pole comes into the picture. The output impedance of the MOSFET and the load capacitance set the second pole. The MOSFET shown in the ADP3178 data sheet is the SUB45N03-13L. The method for selecting a MOSFET for a particular application should be driven by power dissipation requirements. It should also have a logic level $V_{th}$ for easier drive. In addition, selection of a MOSFET with lower $Q_g$ (gate charge) will improve the transient response and slew rate. Ideally, one would use a drain supply voltage sufficiently above the required output voltage to give headroom on $V_{ds}$ for a required output current while keeping the power dissipation to a minimum. The 4.3 A requirement on the 2.5 V DDR VDDQ supply would give a maximum power dissipation figure of $0.8 \times 4.3 = 3.44$ W given a 3.3 V supply. That figure can be dropped to 2.15 W if a 3 V drain supply is available. After selecting a MOSFET and package capable of handling the power, one should check the transconductance, $g_m$. For example, the SUB45N03-13L has a $g_m$ of 15 Siemens for a 1 A load current.

Because the output capacitance of the MOSFET is very small compared to the load capacitance, the second pole for this Miller configuration can be simplified to:

$$P_2 = 1 / \left(2 \times \pi \times \left(R_O \times R_{ESR}\right) \times C_L\right)$$

Where $C_L$ is the load capacitance and $R_O = 1/g_m$. Load capacitance in this paper is meant to describe the physical capacitor placed between the source of the MOSFET and analog ground.

Some authors refer to the sum of the capacitances driven by the MOSFET's source as the bypass capacitance, $C_{BP}$. This value is typically smaller than that of the load capacitance. For example, if the linear regulator drives the supply voltage for five other devices, each of which locally bypasses VDD to VGND through the typical 0.1 μF ceramic capacitor (ESR is negligible for these capacitors), this bypass capacitance would be only 0.5 μF versus, say, a 10 μF load capacitance. The pole contributed by the bypass capacitance for this compensation approach is usually well beyond the "zone of concern."

For example, if the load capacitor is a 10 μF MLCC (with an ESR of around 10 mΩ) and the SUB45N03-13L is used, the second pole lands at 208 kHz. The pole contributed by 0.5 μF of bypass capacitance is around 32 MHz, as:

$$P_3 = 1 / \left(2 \times \pi \times R_{ESR} \times C_{BP}\right)$$

Given a constant gain-bandwidth product for this voltage feedback circuit, a dominant pole location near $P_2/A_V = 208$ kHz/450 = 462 Hz is needed in order to cross through unity gain at 208 kHz. Figure 2 illustrates the frequency response. Using a value of 10 kΩ for $R_f$, $C_m$ would be about 71 pF, per the equation for $P_d$ above. 68 pF is the closest standard value, as seen in Figure 1. Given that the ADP3178 requires a feedback voltage of 1.0 V, the 10 kΩ equivalent feedback resistance for generating 2.5 V would be $R_1$ = 25 kΩ (replacing the 10 kΩ resistor in Figure 1) and $R_2$ = 16.7 kΩ (tied from LRFB to ground). The Thevenin value of 10 kΩ is a convenient value and can be changed (which also changes $C_m$). However, it should not be made too large due to the input bias current of the linear regulator.

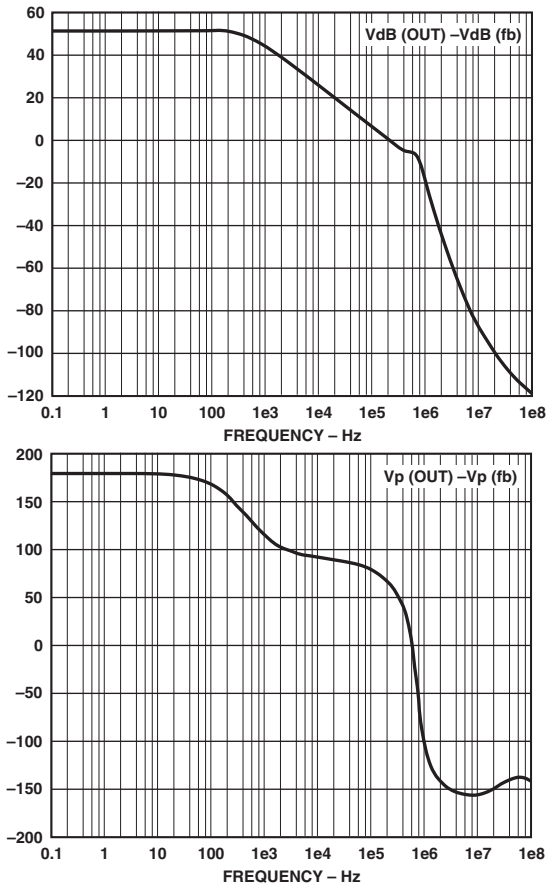


*Figure 2. AC Gain/Phase Plot*

The equivalent model for the load capacitance is difficult to determine exactly because it depends on the ESR of the capacitance as well as the layout. For example, if instead of a 10 μF MLCC for the load capacitor, a bulk capacitor of 100 μF and 0.5 Ω ESR were used, the second pole of this system would be at 2.8 kHz. The zero, also a function of the bulk capacitor's ESR, is at 3.2 kHz via:

$$Z = 1 / \left(2 \times \pi \times C_L \times R_{ESR}\right)$$

Since both of these transitions occur close together and well before (nearly two decades) the 208 kHz critical point, they act to "cancel" one another. Thus the bulk capacitor will not have a significant effect on the loop response of the linear regulator at crossover. Also, if several high frequency capacitors are connected in parallel (along a bus on the linear regulator's output, for example), the ESR of these capacitors located away from the linear regulator's output will be higher due to board parasitics. This will only push the zero closer to the second pole. So, fortunately for the ADP3178 design, these "distant" capacitors will maintain their preferable local bypass effect, but will not affect stability. However, because of this uncertainty in the load characteristics, it is still important to verify the operation in the actual application. If the output shows instability under any load conditions, $C_m$ should be increased.

The linear regulator cannot instantaneously respond to a transient condition. There is some fixed delay time before the MOSFET can handle the increased load current. During this time, the load capacitor has to handle the full transient load. The ESL (equivalent series inductance) of the load capacitor and its layout, while usually quite small, can have an impact where design specifications call out a high $\delta i/\delta t$. To keep the ESL low, place the MOSFET and the load capacitor as close as possible to the linear regulator. In addition, one should consider using a plane for the linear regulator output and its return path.

The next question to ask when selecting the load capacitor is: "Is the ESR low enough for a transient load step?" If the specification allows for a 100 mV droop for a 1 A current step, then the ESR should obviously be less than 100 mΩ. The second consideration is the total charge and allowable droop. After the ESR step, the capacitor has to supply the load current until the linear regulator can catch up.

The larger the dip in the output voltage, the greater the differential voltage seen on the inputs of the linear regulator amplifier; thus a greater MOSFET drive current. So the linear regulator responds faster in circuits with larger ESR values; the ESR droop period decreases as the ESR increases. Optimal transient performance would mandate a minimum ESR, which in many alternate designs would compromise stability. This is a primary advantage of the ADP3178. As discussed earlier, the ADP3178 does not rely on load capacitor ESR for stability (the pole and zero created by the ESR tend to cancel one another).

The dip in output voltage can be translated to the output of the amplifier via $A_V$, where the output drive current is governed by the amplifier's small signal output impedance (measurements show it on the ADP3178 to be typically around 100 kΩ with a range of 75 kΩ to 150 kΩ). For a 10 μF MLCC load capacitor, as discussed previously, the unity gain crossover point was calculated as 208 kHz. The closed-loop response of this system must, therefore, be greater than 1/208 kHz or 4.8 μs. The simulations in Figure 3 are consistent.

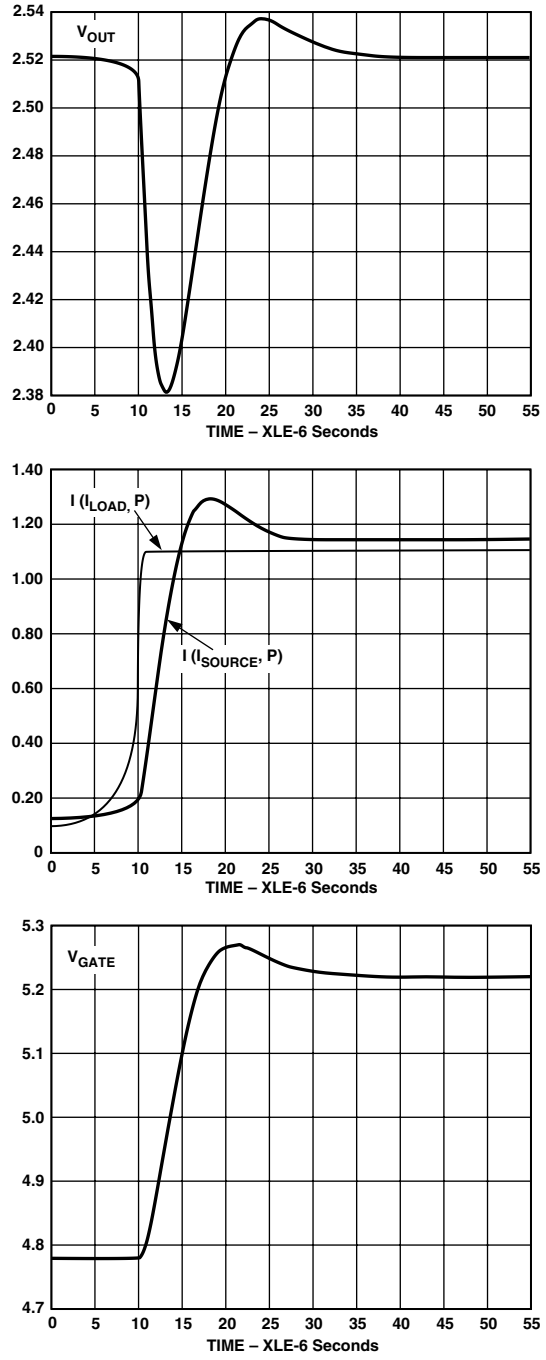


*Figure 3. Transient Response with 10 µF MLCC Output Capacitor*

Another way to examine this closed loop is from a voltage standpoint (see Figure 3). The load capacitor "sees" a voltage dip as a result of the current step—in this case 1 A. This voltage dip is governed by:

$$\delta V_{OUT} / \delta t = I_{STEP} / C_L$$

For this example, the $V_{OUT}$ graph of Figure 3 shows a slope of about –100 mV/µs. The linear regulator amplifier will respond to an attenuated version of this at its input—40 mV/µs for an output voltage of 2.5 V and reference voltage of 1 V as on the ADP3178. The amplifier's negative feedback attempts to force its inputs equal by driving its output more positive. The response of the system takes advantage of the "pull-apart" drive on the MOSFET—i.e., the amplifier is driving the gate higher, while the load capacitor discharge is pulling the source lower. $V_{gs}$ thus increases relatively quickly, as does the MOSFET drain current managed by $g_m = I_d/V_{gs}$.

Of interest is the fact that the ADP3178's output drive current is about four times greater than that of the ADP3158 (it is limited to about 2 mA), but will likely have an advantage only for MOSFETs with very high gate capacitance or very small transconductances. Therein lies another factor beyond power dissipation for MOSFET selection. It is clear from the $V_{GATE}$ graph in Figure 3, estimating $\delta V_{GATE}/\delta t$ to be about 60 mV/µs, that the amplifier's drive current is nonlimiting, as:

$$I_{DRIVE} = C_{GATE} \times \left(\delta V_{GATE} / \delta t\right)$$

and for this example, with the SUB45N03-13L, the average $I_{DRIVE}$ is about 160 µA. This is well within the specifications for the ADP3178.

$V_{OUT}$ will continue to drop, as the graph in Figure 3 shows, until the MOSFET is charging the load capacitor at the same rate as the load capacitor is discharging to drive the load. After this point, the capacitor will be charging while the MOSFET supplies a growing percentage of the total load current. If critically damped, the system will reach equilibrium when the MOSFET drain current exceeds 1 A and the residual current is available to charge the load capacitor back to the programmed output voltage as a function of the load capacitance, its ESR, and the output resistance of the MOSFET. For this example, the system overshoots, and, as expected, the voltage on the load capacitor lags behind the MOSFET "charging" current.

In conclusion, the ADP3178 provides two versatile linear regulators capable of excellent transient response. It operates without the need for large load capacitors or MOSFETs while avoiding stability concerns via Miller compensation.

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