TMC2241

65V 2ARMS Smart Integrated Stepper Driver with S/D and SPI

General Description

The TMC2241 is a smart, high-voltage stepper driver IC with step and direction control and serial communication interfaces. It combines the industry's most advanced stepper motor driver based on the 256 microsteps, built-in indexer and two fully integrated 65V, 3.0AMAX H-bridges, plus non-dissipative integrated current sensing (ICS).

ADI-Trinamic's sophisticated StealthChop2 chopper ensures absolutely noiseless operation combined with maximum efficiency and best motor torque.

High integration, high energy efficiency, and a small form factor enable miniaturized and scalable systems for cost-effective solutions. The complete solution reduces the learning curve to a minimum, while giving best-in-class performance. The H-bridge field-effect transistors (FETs) have very low impedance, resulting in high driving efficiency and minimal heat generated. The typical total R_{ON} (high side + low side) is 0.31Ω.

The maximum RMS current per H-bridge is $2A_{RMS}$ with V_S = 24V and $1.7A_{RMS}$ with V_S = 48V supply at room temperature, assuming a four-layer PCB.

The permissible continuous current is thermally limited. It depends on the operation duty cycle, and on the thermal characteristics of the application (PCB ground planes, heatsink, and ventilation).

The maximum full-scale current per H-bridge is 3A (peak). This current is defined as the maximum current setting of the embedded current drive regulation circuit.

The internal overcurrent protection (OCP) adapts to the motor current range to protect the IC and motor, and limits peak current to 5A in the highest setting.

The non-dissipative ICS eliminates the bulky external power resistors, resulting in a dramatic space and power saving compared with mainstream applications based on external sense resistors, while providing the same overall accuracy.

The TMC2241 features extensive diagnostics and protections such as short protection/OCP, thermal shutdown, and undervoltage lockout (UVLO).

During thermal shutdown and UVLO events, the driver is disabled. Furthermore, the TMC2241 provides functions to measure the driver temperature, estimate the motor temperature, and measure one external analog input.

The TMC2241 is available in a small TQFN38 5mm x 7mm package with exposed pad.

Applications

- Textile, Sewing Machines, Knitting Machines
- Lab and Factory Automation
- ID Printers/Card Printers
- Liquid Handling, Medical Applications
- Office Automation and Paper Handling
- POS, Massage Chairs
- ATM, Cash Recycler, Bill Validators, Cash Machines
- CCTV, Security
- Pumps and Valve Control
- Heliostat and Antenna Positioning
- Stage Lighting

Benefits and Features

- Voltage Range: 4.5V to 65V DC
- Low R_{ON} (HS + LS): 0.31Ω Typical (T_A = 25°C)
- Current Ratings per H-Bridge (Typical at 25°C):
  - $2A_{RMS}$ (2.8A Sine Peak) at V_S = 24V
  - $1.7A_{RMS}$ (2.4A Sine Peak) at V_S = 48V
- Fully Integrated Lossless Current Sensing
- Step/Direction (S/D) Interface with MicroPlyer Step Interpolation
- SPI and Single-Wire UART
- Encoder Interface
- Highest Resolution of 256 Microsteps per Full Step
- Flexible Wave Table and Phase Shift to Match Motor
- StealthChop2 Silent Motor Operation
- SpreadCycle Highly Dynamic Motor Control Chopper
- Jerk-Free Combination of StealthChop2 and SpreadCycle
- StallGuard2 and StallGuard4 Sensorless Motor Load Detection
- CoolStep Current Control for Energy Savings up to 75%
- Passive Braking and Freewheeling Mode
- Motor Phase Temperature Estimation
- Chip Temperature Measurement
- General Purpose Analog Input
- Full Protection and Diagnostics
- Overvoltage Protection Output
- Compact 5mm x 7mm TQFN38 Package

19-102045; Rev 0; 11/25

TMC2241

65V 2ARMS Smart Integrated Stepper Driver with S/D and SPI

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Package Information

TQFN38 5mm x 7mm	
Package Code	T3857+1C
Outline Number	21-0172
Land Pattern Number	90-0076
Thermal Resistance, Single Layer Board:	
Junction to Ambient (θ_{JA})	38°C/W
Junction to Case (θ_{JC})	1°C/W
Thermal Resistance, Four Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

Absolute Maximum Ratings

V_S to GND ..... -0.3V to 70V

V_{DD1V8} to GND ..... -0.3V to Min. (2.2, V_S + 0.3)V

AGND to GND ..... -0.3V to +0.3V

OUT1A, OUT2A, OUT1B, OUT2B .....-0.3V to V_S + 0.3V

V_{CP} to GND .....V_S - 0.3V to Min. (74, V_S + 6)V

CPO to GND .....V_S - 0.3V to V_{CP} + 0.3V

CPI to GND .....-0.3V to V_S + 0.3V

SLEEPN to GND .....-0.3V to V_S + 0.3V

I_{REF}, AIN to GND .....-0.3V to Min. (2.2, V_{DD1V8} + 0.3)V

V_{CC_IO} to GND.....-0.3V to 6V

Logic Input/Output Voltage to GND..... -0.3V to V_{CC_IO} + 0.3V

OV to GND.....-0.3V to 6V

Operating Temperature Range..... -40°C to 125°C

Junction Temperature.....+165°C

Storage Temperature Range..... -65°C to +150°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_S = 4.5V to 65V, V_{CC_IO} = 2.2V to 5.5V = R_{REF} from 12kΩ to 24kΩ. Typical values assume T_A = 25ºC and V_S = 48V. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_S		4.5		65	V
Sleep Mode Current Consumption	IVS	V(SLEEPN) = 0		4	25	µA
Quiescent Current Consumption	IVS	V(SLEEPN) = 1, V(DRV_ENN) = 1		3.5	6	mA
1.8V Regulator Output Voltage	VVDD	V_S = 4.5V		1.8		V

(V_S = 4.5V to 65V, V_{CC_IO} = 2.2V to 5.5V = R_{REF} from 12kΩ to 24kΩ. Typical values assume T_A = 25ºC and V_S = 48V. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Current Limit	IV18LIM		20			mA
Charge Pump Voltage	V_{CP}			V_S + 2.7		V
Logic I/O Supply Voltage Range	V_{CC_IO}		2.2		5.5	V
Sleep Mode Current Consumption	IVCC_IO	V(SLEEPN) = 0		5	10	µA
Quiescent Current Consumption	IVCC_IO	V(SLEEPN) = 1		35	60	µA
LOGIC LEVEL INPUTS-OUTPUTS						
Input Voltage Level - High	V_{IH}		0.7 × V_{CC_IO}			V
Input Voltage Level - Low	V_{IL}				0.3 × V_{CC_IO}	V
Input Hysteresis	V_{HYS}			0.15 × V_{CC_IO}		V
Internal Pullup/Pulldown Resistance	R_{PULL}	To GND or to V_{CC_IO}	60	100	140	kΩ
Input Leakage	InLeak	Inputs without pullup/pulldown resistance	-1		+1	µA
Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.4	V
Push-Pull Output LogicHigh Voltage	V_{OH}	I_{LOAD} = 5mA	V_{CC_IO} – 0.4V			
Open-Drain Output Logic High Leakage Current	I_{OH}	V(PIN) = 5.5V	-1		+1	µA
SLEEPN Voltage Level High	$V_{IHSLEEPN}$		0.9			V
SLEEPN Voltage Level Low	$V_{ILSLEEPN}$				0.6	V
SLEEPN Pulldown Input Resistance	$R_{PDSLEEPN}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output ON-Resistance Low Side	R_{ONLS}	Full-scale bits = 10		0.15	0.3	Ω
		Full-scale bits = 01		0.21	0.4	
Output ON-Resistance Low Side	R_{ONLS}	Full-scale bits = 00		0.37	0.75	Ω
Output ON-Resistance High Side	R_{ONLS}			0.16	0.3	Ω
Output Leakage	I_{LEAK}		-10		+10	µA
Output Slew Rate	SR	Slew-rate bits = 00		100		V/µs
		Slew-rate bits = 01		200		
		Slew-rate bits = 10		400		
		Slew-rate bits = 11		800		
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	OCP	Full-scale bits = 10	5.0			A
		Full-scale bits = 01	3.33			

(V_S = 4.5V to 65V, V_{CC_IO} = 2.2V to 5.5V = R_{REF} from 12kΩ to 24kΩ. Typical values assume T_A = 25ºC and V_S = 48V. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Full-scale bits = 00	1.67			
Overcurrent Protection Blanking Time	TOCP		0.9	1.5	2.3	µs
UVLO Threshold on V_S	UVLO	V_S falling	3.75	3.9	4.05	V
UVLO Threshold on V_S Hysteris	UVLOHYS			0.12		V
UVLO Threshold on V_{CC_IO}	UVLO	V_{CC_IO} falling	0.9	1.5	1.95	
V_{CC_IO} UVLO Hysteresis	UVLOVCCH			100		mV
Thermal Protection Threshold Temperature	TSD			165		°C
Thermal Protection Temperature Hysteresis				20		°C
CURRENT REGULATION						
I_{REF} Pin Resistor Range	R_{REF}		12		60	kΩ
I_{REF} Output Voltage	V_{REF}		0.882	0.9	0.918	V
Full-Scale Current Constant	KIFS	IFS = 1A		11.75		A × kΩ
		IFS = 2A		24		
		IFS = 3A		36		
Regulation Accuracy	DITRIP1	Output current from 7% to 100% FS, R_{REF} = 12kΩ	-7		+7	%
Phase-to-Phase Current Regulation Mismatch	I_{MATCH}	Output currents from 7% to 100% FS, R_{REF} = 12kΩ One Sigma		0.7		%
FUNCTIONAL TIMINGS						
SLEEP Time	t_{SLEEP}	SLEEPN = 0 to OUT_ three state			50	µs
Wake-Up Time from Sleep	T_{WAKE}	SLEEPN = 1 to normal operation			2.5	ms
Enable Time	T_{EN}	Time from DRV_ENN pin falling edge to driver on			1.5	µs
Disable Time	T_{EN}	Time from DRV_ENN pin rising edge to driver off			6	µs
CLOCK						
Internal Clock Frequency	f_{CLKOSC}		11.9	12.5	13.2	MHz
External Clock Frequency	f_{CLK}		8	16	20	MHz
External Clock Duty Cycle	t_{CLKL}		40		60	%
External Clock Detection in Cycles			4		8	
External Clock Timeout Detection in Cycles of Internal fCLKOSC			12		16	
External Clock Detection Lower Frequency Threshold	f_{CLKLO}		4			MHz

(V_S = 4.5V to 65V, V_{CC_IO} = 2.2V to 5.5V = R_{REF} from 12kΩ to 24kΩ. Typical values assume T_A = 25ºC and V_S = 48V. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMINGS						
SCK Valid Before or After Change of CSN	t_{CC}		t_{SCK}			ns
CSN High Time	t_{CSH}		4 × t_{SCK}			ns
SCK Low Time	t_{CL}		20			ns
SCK High Time	t_{CH}		20			ns
SCK Frequency	f_{SCK}	V_{CC_IO} = 3V			8	MHz
		V_{CC_IO} = 2.2V			5	
SDI Setup Time Before SCK Rising Edge	t_{DU}		10			ns
SDI Hold Time After SCK Rising Edge	t_{DH}		10			ns
Data Out Valid Time After SCK Falling Edge	t_{DO}	V_{CC_IO} = 3V		33	50	ns
		V_{CC_IO} = 2.2V		50	80	ns
SDI, SCK, and CSN Filter Delay Time	t_{FILT}	Rising and falling edge		10		ns
STEP/DIR TIMINGS						
Step Frequency	f_{STEP}	Dedge = 1			f_{CLK}/4	
		Dedge = 0			f_{CLK}/8	
Fullstep Frequency	f_{FS}				f_{CLK}/512	
STEP High Time	t_{SH}		t_{CLK} + 20			ns
STEP Low Time	t_{SL}		t_{CLK} + 20			ns
DIR/STEP to CLK Setup Time	t_{SU}		10			ns
DIR/STEP to CLK Hold Time	t_{SH}		10			ns
DIR to STEP Setup Time	t_{SU}		20			ns
ENCODER TIMING						
Encoder Counting Frequency	f_{CNT}			< 2/3 f_{CLK}	f_{CLK}	
A/B/N Input Low Time	t_{ABNL}		3 x t_{CLK} + 20			ns
A/B/N Input High Time	t_{ABNH}		3 x t_{CLK} + 20			ns
A/B/N Spike Filtering Time	$t_{FILTABN}$	Rising and falling edge		3 x CLK		
ADC/ANALOG INPUT/TEMPERATURE						
ADC Resolution		12 bit + sign		13		Bit
Analog Input Voltage Range	V_{AIN}		0		1.25	V
Analog Input Leakage	$I_{AIN,IEAK}$		-1		+1	uA
Analog Input Frequency	f_{AIN}	Assuming undersampling at AIN is accepted, the AIN input frequency must be lower than the given max. value for a			70	kHz

(V_S = 4.5V to 65V, V_{CC_IO} = 2.2V to 5.5V = R_{REF} from 12kΩ to 24kΩ. Typical values assume T_A = 25ºC and V_S = 48V. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		meaningful ADC conversion for a single ADC channel.				
Driver Temperature Accuracy	T_{DRIVER}			±10		°C
Supply Voltage Measurement Accuracy		V_M = 4.5V	-7		+7	%
		V_M >= 12V	-4		+4	
ADC Sample Rate	$f_{SAMPLE, ADC}$			$\frac{fCLK}{2048}$		

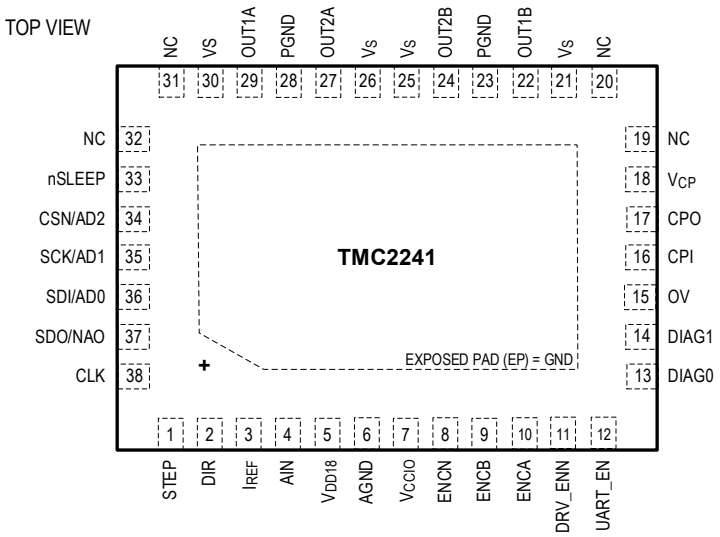
Pin Descriptions

PIN	NAME	FUNCTION	REF SUPPLY	Type
6	AGND	Analog Ground. Connect to ground plane.		GND
23, 28	PGND	Power Ground. Connect to ground plane.		GND
21, 25, 26, 30	V_S	Motor Supply Voltage. Provide filtering capacity near pin with shortest loop to GND plane/exposed pad.		Supply
5	V_{DD1V8}	Output of Internal 1.8V Regulator. Attach 2.2µF or larger ceramic capacitor to AGND near to pin for best performance.		Supply
18	V_{CP}	Charge Pump Voltage. Tie to V_S using 1.0µF capacitor. Connect positive end of capacitor close to V_S pin to avoid inductive peaks.		Analog Output
7	V_{CC_IO}	Digital IO supply voltage provided from external source to define circuit IO level. Required for proper voltage level settings on output pins.		Supply
17	CPO	Charge Pump Capacitor Output		Analog Output
16	CPI	Charge Pump Capacitor Input. Tie to CPO using the VS-rated 22nF capacitor.		Analog Output
38	CLK	CLK Input. Tie to GND using short wire for internal clock or supply external clock. Internal clock-fail over circuit protects against loss of external clock signal.	VCC_IO	Digital Input
1	STEP	Step Input	VCC_IO	Digital Input
2	DIR	Direction input	VCC_IO	Digital Input
34	CSN/AD2	SPI chip select input (negative active) (UART_EN = 0) or Address input 2 (+4) in UART mode (UART_EN = 1).	VCC_IO	Digital Input (Pullup)
35	SCK/AD1	SPI serial clock input (UART_EN = 0) or address input 1 (+2) in UART mode (UART_EN = 1).	VCC_IO	Digital Input (Pullup)
36	SDI/AD0	SPI data input (UART_EN = 0) or address input 0 (+1) in UART mode (UART_EN = 1).	VCC_IO	Digital Input (Pullup)
37	SDO/NAO	SPI data output (three-state) (UART_EN = 0) or next address output (NAO) in UART mode (UART_EN = 1).	VCC_IO	Digital Output
3	I_{REF}	Analog Reference Current for Current Scaling. Provide external resistor to GND.	VDD_18	Analog Input

12	UART_EN	Interface selection pin. When tied low, the SPI interface is enabled. When tied high, the UART interface is enabled. Integrated pull-down resistor.	VCC_IO	Digital Input (Pulldown)
9	ENCB	Encoder B-channel input.	VCC_IO	Digital Input (Pullup)
10	ENCA	Encoder A-channel input.	VCC_IO	Digital Input (Pullup)
8	ENCN	Encoder N-channel input.	VCC_IO	Digital Input (Pullup)
11	DRV_ENN	Enable Input. The power stage is switched off (all motor outputs floating) when this pin is driven to a high level.	VCC_IO	Digital Input (Pullup)
13	DIAG0	Diagnostics output DIAG0. Interrupt or STEP output from internal motion controller for external driver. Use external pullup resistor in open drain mode. In system reset state this pin is actively pulled low to indicate reset condition to external controller.	VCC_IO	Digital Output
14	DIAG1/SW	Diagnostics Output DIAG1. Position compare or DIR output from internal motion controller for external driver. Use external pullup resistor in open-drain mode. Single-wire I/O in UART mode.	VCC_IO	Digital IO
33	nSLEEP	Low active power down input/reset input. Apply a continuous low level to bring the device to sleep mode. SLEEPN has an internal pulldown. If not used, connect to V_S or V_{CC_IO} (this is a high voltage pin). Once the IC returns from sleep mode/reset, it must be reconfigured before being used again. Register content is not stored during sleep mode. While reconfiguring the IC, it is advised to still hold the bridge drivers disabled with DRV_ENN. Do not use while at high motor velocity!	VS	Analog Input (Pulldown)
24	OUT2B	Motor Coil B Output 2	VS	Analog Output
22	OUT1B	Motor Coil B Output 1	VS	Analog Output
27	OUT2A	Motor Coil A Output 2	VS	Analog Output
29	OUT1A	Motor Coil A Output 1	VS	Analog Output
EP	GND	Exposed Die Pad. Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to the GND plane. Serves as the GND pin for power stage and internal circuitry.		GND
19, 20, 31, 32	N.C.	No Internal Connection. Leave this pin open or tie it to GND for improved cooling.		N.C.
15	OV	Overvoltage Indicator Output (Open-Drain) with Programmable Threshold Voltage. Attach external MOSFET with load resistor to limit supply voltage. External pullup resistor required. Updated by ADC with $f_{CLK}/2048$.	VCC_IO	Digital Output (Open-Drain)
4	AIN	General-purpose analog input measured with internal ADC with $f_{CLK}/2048$. Input range 0 to 1.25V. Value available through SPI/UART.	VDD_18	Analog Input

Pin Configurations

TMC2241 TQFN Pin Configuration



TQFN38
(5mm x 7mm)

Functional Diagrams

TMC2241

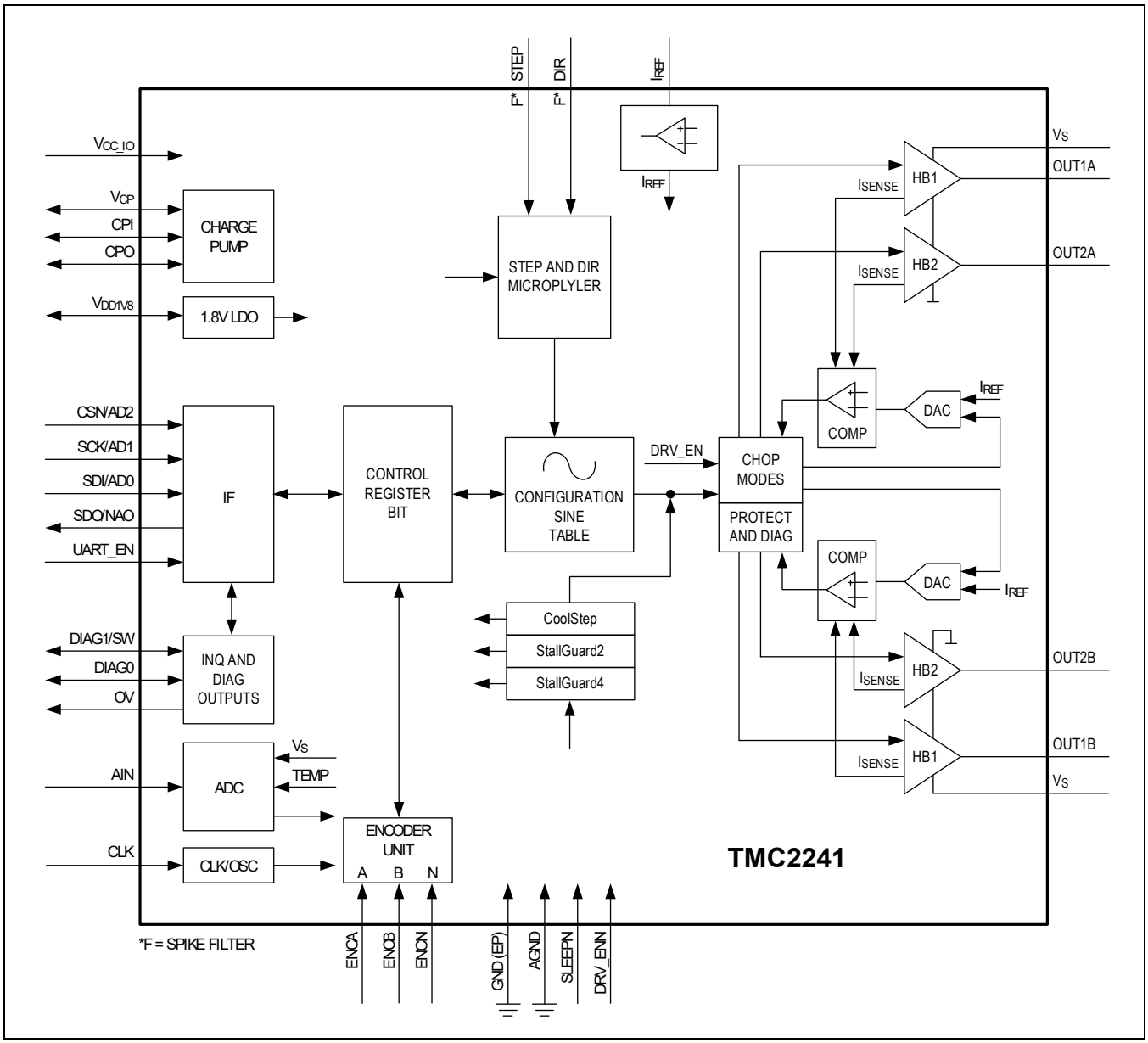


Figure 1. Block Diagram

Detailed Description

Principles of Operation

SPI Stepper Motor Driver

The TMC2241 is an intelligent stepper motor driver chip. This smart power conversion component directly drives a two-phase stepper motor and interfaces to a CPU for configuration, control, and diagnostic feedback. All current control functions to drive a stepper motor are fully integrated. The TMC2241 offers numerous unique functions, which support operating the motor within the application.

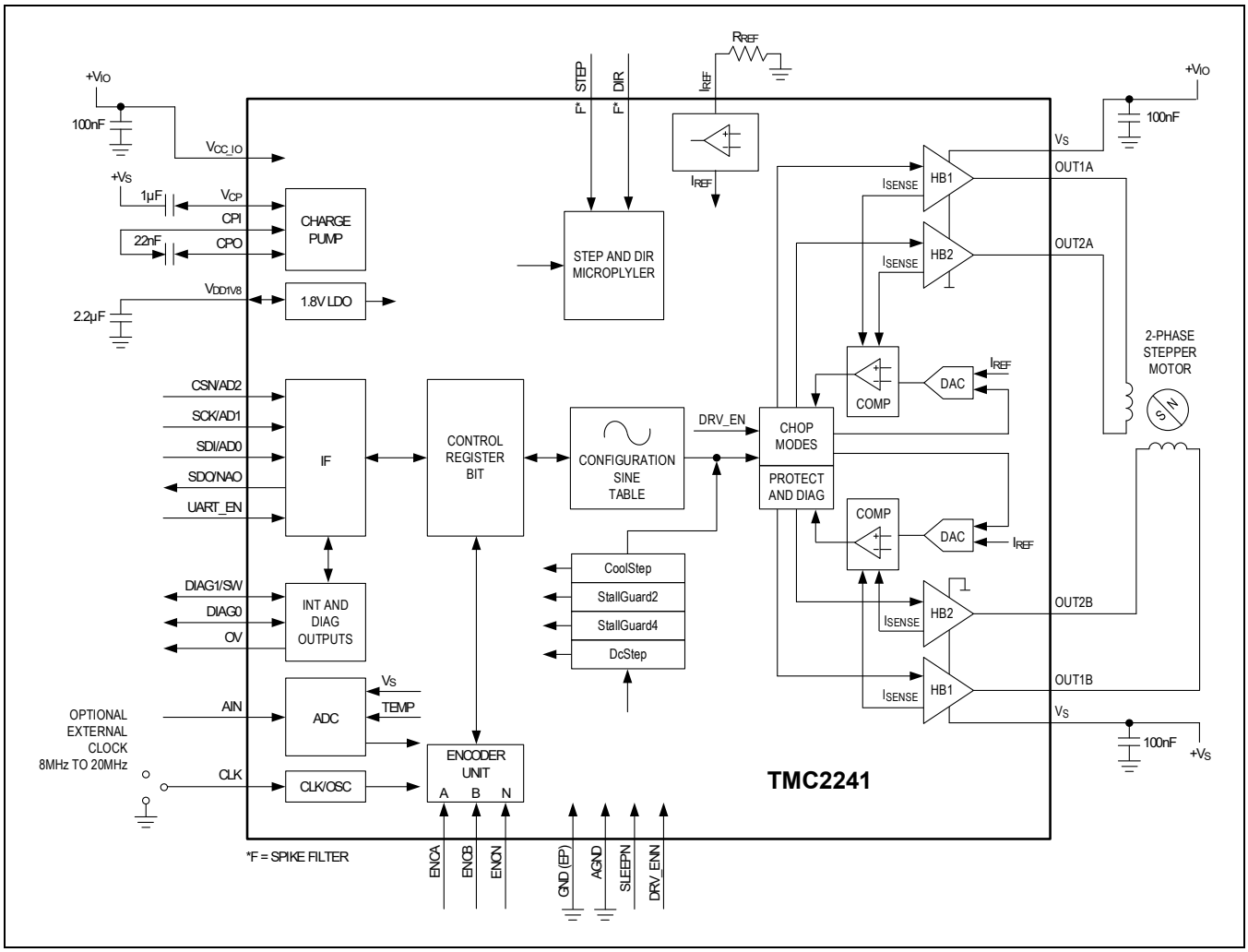


Figure 2. Block Diagram with Typical External Components

Key Concepts

The TMC2241 implements advanced features exclusive to ADI-Trinamic products. These features contribute toward greater precision, greater energy efficiency, higher reliability, smoother motion, and cooler operation in many stepper motor applications.

StealthChop2	No-noise, high-precision chopper algorithm for inaudible motion and inaudible standstill of the motor. Allows faster motor acceleration and deceleration than StealthChop and extends StealthChop to low standstill motor currents.
SpreadCycle	High-precision cycle-by-cycle current control for highest dynamic movements.
StallGuard2	Sensorless stall detection and mechanical load measurement for SpreadCycle.

StallGuard4	Sensorless stall detection and mechanical load measurement for StealthChop.
CoolStep	Uses StallGuard measurement to adapt the motor current for best efficiency and lowest heat-up of the motor and driver.
MicroPlyer	Microstep interpolator to run at full 256 microstepping with low resolution step input.

In addition to these performance enhancements, the ADI-Trinamic motor drivers offer safeguards to detect and protect against shorted outputs, output open-circuit, overtemperature, and undervoltage conditions for enhancing safety and recovery from equipment malfunctions.

Control Interfaces

The TMC2241 supports both the SPI and UART-based single-wire interface with cyclic redundancy check (CRC). The actual interface combination is selected through the UART_EN pin, which can be hardwired to GND or V_{CC_IO}, depending on the desired interface selection.

The SPI is a bit-serial interface synchronous to a bus clock. For every bit sent from the bus controller to the bus peripheral, another bit is sent simultaneously from the peripheral back to the controller. Communication between an SPI controller (example, an MCU) and the peripheral always consists of sending one 40-bit command word and receiving one 40-bit status word.

The single-wire interface allows a bidirectional single-wire interfacing. It can be driven by any standard UART. No baud rate configuration is required.

Automatic Standstill Power Down

An automatic current reduction drastically reduces application power dissipation and cooling requirements. A reduction to half of the run current reduces standstill power dissipation to roughly 25%. Standstill current, delay time, and decay parameters can be configured through the serial control interfaces.

Automatic freewheeling and passive motor braking are provided as an option for standstill. Passive braking reduces motor standstill power consumption to zero, while still providing effective dampening and braking!

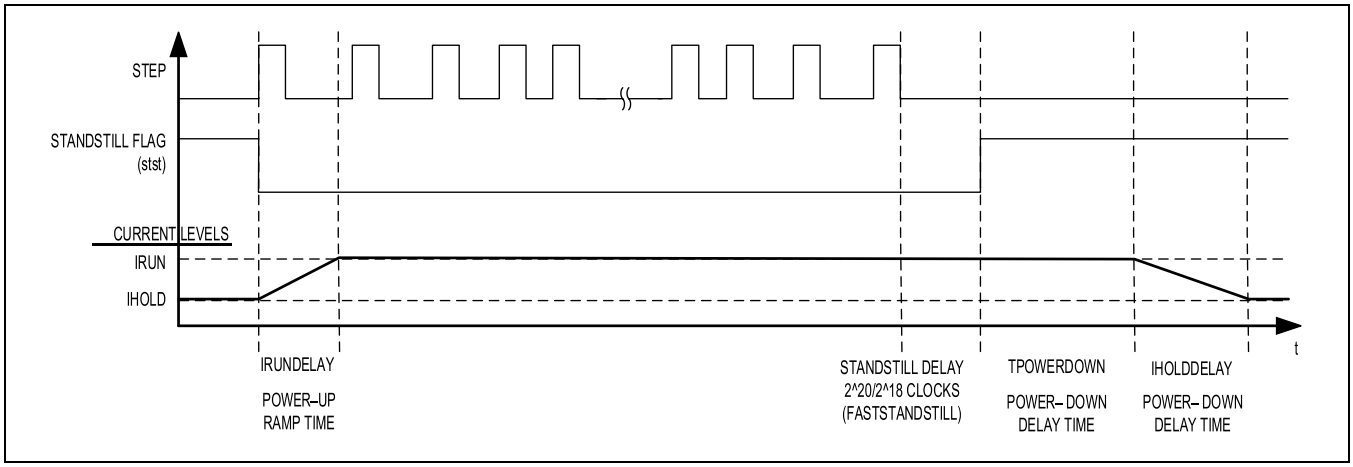


Figure 3. Automatic Motor Current Control at Standstill and Ramp-Up

StealthChop2 and SpreadCycle Driver

StealthChop2 is a voltage chopper-based principle. It guarantees the motor is absolutely quiet in standstill and in slow motion, except for the noise generated by ball bearings.

Unlike other voltage mode choppers, StealthChop2 does not require any configuration. It automatically learns the best settings during the first motion after power-up and further optimizes the settings in subsequent motions.

An initial homing sequence is sufficient for learning. Optionally, initial learning parameters can be loaded to the register set. StealthChop2 allows high motor dynamics by reacting at once to a change of motor velocity.

For highest velocity applications, SpreadCycle is an alternative option to StealthChop2. StealthChop2 and SpreadCycle may even be used in a combined configuration for the best of both worlds: StealthChop2 for no-noise standstill, silent, and smooth performance, SpreadCycle at higher velocity for high dynamics and highest peak velocity at low vibration.

SpreadCycle is an advanced cycle-by-cycle chopper mode. It offers smooth operation and good resonance dampening over a wide range of speed and load. The SpreadCycle chopper scheme automatically integrates and tunes fast decay cycles to guarantee smooth zero-crossing performance.

Benefits

- Significantly improved microstepping with low-cost motors.
- Motor runs smooth and quiet.
- Absolutely no standby noise.
- Reduced mechanical resonance improves torque output.

StallGuard2/StallGuard4 – Mechanical Load Sensing

StallGuard2 and StallGuard4 provide an accurate measurement of the load on the motor. These can be used for stall detection as well as for other uses at loads below those that stall the motor, such as CoolStep load-adaptive current reduction.

This gives more information on the drive, allowing functions like sensorless homing and diagnostics of the drive mechanics. While StallGuard2 combines with SpreadCycle chopper, StallGuard4 uses a different principle to combine with StealthChop2.

CoolStep – Load Adaptive Current Control

CoolStep drives the motor at the optimum current. It uses the StallGuard2 or StallGuard4 load measurement information to adjust the motor current to the minimum amount required in the actual load situation.

CoolStep results in energy savings and keeps the components cool. Because it drives the motor with the optimum current, CoolStep increases the motor efficiency compared to standard operations with approximately 50% torque reserve.

Benefits

- Highest energy efficiency, power consumption decreased by up to 75%.
- Motor generates less heat.
- Improved mechanical precision.
- Less or no cooling.
- Improved reliability.
- Use of smaller motor is possible, less torque reserve required.
- Less motor noise due to less energy exciting motor resonances.

Encoder Interface

The TMC2241 provides an encoder interface for external incremental encoders. The encoder can be used for consistency checks on-the-fly between the encoder position and external ramp generator position. A programmable prescaler allows the adaptation of the encoder resolution to the motor resolution. A 32-bit encoder counter is provided.

Serial Peripheral Interface (SPI)

SPI Datagram Structure

The TMC2241 uses 40-bit SPI datagrams for communication with a microcontroller. Microcontrollers equipped with hardware SPI are typically able to communicate using integer multiples of 8 bits. The TMC2241 can cascade ICs with multiples of 5 bytes in a single chain. It is possible to cascade third-party peripherals with a single byte. For this, dummy bytes must be inserted to achieve a multiple of 5 bytes. The CSN line of the device must stay active (= low) for the complete duration of the datagram transmission.

Each datagram sent to the device is composed of an address byte followed by four data bytes. This allows direct 32-bit data word communication with the register set. Each register is accessed through 32 data bits even if it uses less than 32 data bits.

For simplification, each register is specified by a one byte address:

- For a read access, the most significant bit of the address byte is 0.
- For a write access, the most significant bit of the address byte is 1.

All registers are readable, most of them are read write, some read only, and some write 1 to clear (example, GSTAT registers).

Table 1. SPI Datagram Structure

MSB (TRANSMITTED FIRST)		40-BIT				LSB (TRANSMITTED LAST)			
39 ... 0									
Write: 8-bit address Read: 8-bit SPI status		Read/write 32-bit data							
39 ... 32		31 ... 0							
Write to RW + 7-bit address Read from 8-bit SPI status		8-bit data		8-bit data		8-bit data		8-bit data	
39/38 ... 32		31 ... 24		23 ... 16		15 ... 8		7 ... 0	
W	38...32	31...28	27...24	23...20	19...16	15...12	11...8	7...4	3...0

Selecting Write/Read (WRITE_notREAD)

The read and write selection is controlled by the MSB of the address byte (bit-39 of the SPI datagram). This bit is 0 for read access and 1 for write access. So, the bit named W is a WRITE_notREAD control bit. The active high write bit is the MSB of the address byte. So, 0x80 must be added to the address for a write access. The SPI always delivers data back to the controller, independent of the W bit. The data transferred back is the data read from the address transmitted with the previous datagram, if the previous access is a read access. If the previous access is a write access, the data read back mirrors the previously received write data. So, the difference between a read and a write access is that the read access does not transfer data to the addressed register but it transfers the address only and its 32 data bits are dummies, and further, the following read or write access delivers back the data read from the address transmitted in the preceding read cycle.

A read access request datagram uses dummy write data. Read data is transferred back to the controller with the subsequent read or write access. Hence, multiple registers can be read in a pipelined fashion.

Whenever data is read from or written to the TMC2241, the MSBs delivered back contain the SPI status. The SPI_STATUS is a number of eight selected status bits.

Example:

For a read access to the register (XACTUAL) with the address 0x21, the address byte must be set to 0x21 in the access preceding the read access. For a write access to the register (VACTUAL), the address byte must be set to 0x80 + 0x22 = 0xA2. For read access, the data bit might have any value (-). So, it can be set to 0.

Table 2. SPI Read/Write Example Flow

ACTION	DATA SENT TO TMC2241	DATA RECEIVED FROM TMC2241
Read TSTEP	0x1200000000	0xST and unused data*
Read TSTEP	0x1200000000	0xST and TSTEP
Write *X_ENC* = 0x00ABCDEF	0xB900ABCDEF	0xST and TSTEP

* ST is a placeholder for the status bits SPI_STATUS.

SPI Status Bits Transferred with Each Datagram Read Back

New status information is latched at the end of each access and is available with the next SPI transfer.

Table 3. SPI_STATUS – Status Flags Transmitted with Each SPI Access in Bits 39 to 32

BIT	NAME	COMMENT
7:4	Don't care	Not used in TMC2241.
3	Standstill	DRV_STATUS[31] – 1: Signals motor standstill.
2	sg2	DRV_STATUS[24] – 1: Signals StallGuard flag active.
1	Driver_error	GSTAT[1] – 1: Signals driver driver error (clear by resetting bit in GSTAT).
0	Reset_flag	GSTAT[0] – 1: Signals that a reset occurred (clear by resetting bit in GSTAT).

Data Alignment

All data are right aligned. Some registers represent unsigned (positive) values, some represent integer values (signed) as two's complement numbers, and single bits or groups of bits are represented as single bits, respectively, as integer groups.

SPI Signals

The SPI bus on the TMC2241 has four signals:

- SCK – bus clock input
- SDI – serial data input
- SDO – serial data output
- CSN – chip select input (active low)

The SPI peripheral is enabled for an SPI transaction by a low on-the-chip select input CSN. Bit transfer is synchronous to the bus clock SCK, with the peripheral latching the data from SDI on the rising edge of SCK and driving data to SDO following the falling edge. The most significant bit is sent first. A minimum of 40 SCK clock cycles is required for a bus transaction with the TMC2241.

If more than 40 clocks are driven, the additional bits shifted into SDI are shifted out on SDO after a 40-clock delay through an internal shift register. This can be used for daisy chaining multiple chips.

The CSN must be low during the whole bus transaction. When CSN goes high, the contents of the internal shift register are latched into the internal control register and recognized as a command from the SPI controller to the SPI peripheral. If more than 40 bits are sent, only the last 40 bits received before the rising edge of CSN are recognized as the command.

SPI Timing

The SPI maximum frequency is at 8MHz. SCK is independent from the clock frequency of the system, while the only parameter depending on the clock frequency is the minimum CSN high time. All SPI inputs are internally filtered to avoid triggering on pulses shorter than 10ns. *Figure 4* shows the timing parameters of an SPI bus transaction. The **Electrical Characteristics** table gives the timing values.

The SPI uses SPI MODE 3.

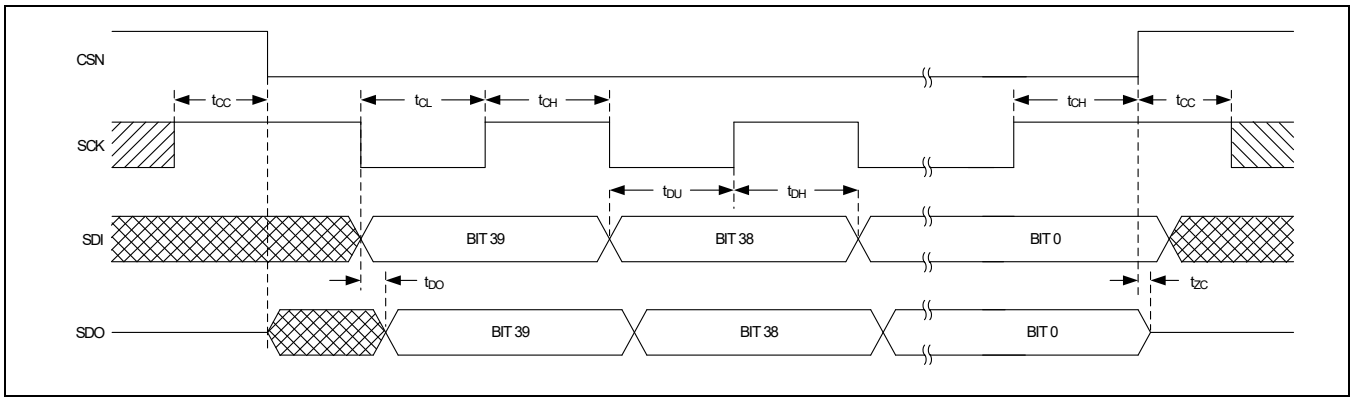


Figure 4. SPI Timing Diagram

UART Single-Wire Interface

The UART single-wire interface allows control of the TMC2241 with any microcontroller UART. It shares transmit and receive line like an RS485-based interface. Data transmission is secured using a cyclic redundancy check, so that increased interface distances (example, over cables between two PCBs) can be bridged without danger of wrong or missed commands even during electromagnetic disturbance. The automatic baud rate detection makes this interface easy to use.

Datagram Structure

Write Access

Table 4. UART Write Access Datagram Structure

EACH BYTE IS LSB…MSB, HIGHEST BYTE TRANSMITTED FIRST																		
0 … 63																		
Sync + Reserved								8-bit node address			RW + 7-bit register address			32-bit data			CRC		
0…7								8…15			16…23			24…55			56…63		
1	0	1	0	Reserved (don't cares but included in CRC)				NODEADDR			Register address		1	Data bytes 3, 2, 1, 0 (high to low byte)			CRC		
0	1	2	3	4	5	6	7	8	…	15	16	…	23	24	…	55	56	…	63

A sync nibble precedes each transmission to and from the TMC2241 and is embedded into the first transmitted byte, followed by an addressing byte. Each transmission allows a synchronization of the internal baud rate divider to the UART host clock. The actual baud rate is adapted and variations of the internal clock frequency are compensated. Thus, the baud rate can be freely chosen within the valid range. Each transmitted byte starts with a start bit (logic 0, low level on DIAG1/SW) and ends with a stop bit (logic 1, high level on DIAG1/SW). The bit time is calculated by measuring the time from the beginning of start bit (1 to 0 transition) to the end of the sync frame (1 to 0 transition from bit-2 to bit-3). All data is transmitted byte wise. The 32-bit data words are transmitted with the highest byte first.

A minimum baud rate of 9000 bauds is permissible, assuming 20MHz clock (worst case for low baud rate). Maximum baud rate is $f_{CLK}/16$ due to the required stability of the baud clock.

The initial peripheral address NODEADDR is selected by CSN_AD2, SCK_AD1, and SDI_AD0 in the range 0 to 7.

The peripheral address is determined by the sum of the register NODEADDR and the pin selection given above. This means that a high level on SDI (with CSN low and SCK low) increments the NODEADDR setting by one.

Bit 7 of the register address identifies a Read (0) or a Write (1) access. Example: Address 0x10 is changed to 0x90 for a write access.

The communication resets if there is a pause of longer than 63-bit times between the start bits of two successive bytes. This timing is based on the last correctly received datagram. In this case, the transmission must be restarted after a failure recovery time of minimum 12-bit times of the bus idle time. This scheme allows the UART host to reset communication in case of transmission errors. Any pulse on an idle data line below 16 clock cycles is treated as a glitch and leads to a timeout of 12-bit times, for which the data line must be idle. Other errors like wrong CRC are also treated the same way. This allows a safe resynchronization of the transmission after any error conditions. Consider that, due to this mechanism, an abrupt reduction of the baud rate to less than 15% of the previous value is not possible.

Each accepted write datagram is acknowledged by the receiver by incrementing an internal cyclic datagram counter (8-bit). Reading out the datagram counter allows the UART host to check the success of an initialization sequence or single write accesses. Read accesses do not modify the counter.

Read Access

Table 5. UART Read Access Request Datagram Structure

EACH BYTE IS LSB…MSB, HIGHEST BYTE TRANSMITTED FIRST																	
Sync + Reserved								8-bit node address			RW + 7-bit register address			CRC			
0...7								8…15			16…23			24…31			
1	0	1	0	Reserved (don't cares but included in CRC)				NODEADDR			Register address		0	CRC			
0	1	2	3	4	5	6	7	8	…	15	16	…	23	24	…	31	

The read access request datagram structure is identical to the write access datagram structure, but uses a lower number of user bits. Its function is to address the UART node and transmit the desired register address for the read access. The TMC2241 responds with the same baud rate as the UART host uses for the read request. To ensure a clean bus transition from the host to the node, the TMC2241 does not immediately send the reply to a read access, but it uses a programmable delay time, after which the first reply byte is sent following a read request.

This delay can be set in multiples of 8-bit times using the SENDDELAY time setting (default = 8-bit times) according to the needs of the UART host. In a multinode system, set SENDDELAY to a minimum of two for all nodes. Otherwise, a non-addressed node might detect a transmission error upon read access to a different node.

Table 6. UART Read Access Reply Datagram Structure

EACH BYTE IS LSB…MSB, HIGHEST BYTE TRANSMITTED FIRST																			
0 63																			
Sync + Reserved								8-bit node address			RW + 7-bit register address			32-bit data			CRC		
0…7								8…15			16…23			24…55			56…63		
1	0	1	0	Reserved (0)				0xFF			Register address		0	Data bytes 3, 2, 1, 0 (high to low byte)			CRC		
0	1	2	3	4	5	6	7	8	…	15	16	…	23	24	…	55	56	…	63

The read response is sent to the UART host using address code %11111111. The transmitter is switched inactive 4-bit times after the last bit is sent.

The address %11111111 is reserved for read accesses going to the UART host. A node cannot use this address.

CRC Calculation

An 8-bit CRC polynomial is used for checking both the read and write access. It allows detection of up to eight single-bit errors. The CRC8-ATM polynomial with an initial value of zero is applied LSB to MSB, including the sync and addressing byte. The sync nibble is assumed to be always correct. The TMC2241 responds only to correctly transmitted datagrams containing its own node address. It increases its datagram counter for each correctly received write access datagram.

$CRC = x^8 + x^2 + x^1 + x^0$

Serial calculation example:

CRC = (CRC << 1) OR (CRC.7 XOR CRC.1 XOR CRC.0 XOR [new incoming bit])

C-Code Example for CRC Calculation

```
void swuart_calcCRC(uint8_t* datagram, uint8_t datagramLength)
{
    // Initialization
    int i,j;
    uint8_t* crc = &datagram[datagramLength-1]; // CRC located in last byte of message
    uint8_t currentByte;
    *crc = 0;

    for (i = 0; i < (datagramLength-1); i++)
    {
        // Execute for all bytes of a message
        currentByte = datagram[i]; // Retrieve a byte to be sent from Array
        for (j = 0; j<8; j++)
        {
            if ((*crc >> 7) ^ (currentByte&0x01))
            {
                // update CRC based result of XOR operation
                *crc = (*crc << 1) ^ 0x07;
            }
            else
            {
                *crc = (*crc << 1);
            }
        currentByte = currentByte >> 1;
        } // for CRC bit
    } // for message byte
}
```

UART Signals

The UART interface on the TMC2241 comprises five signals. In UART mode, each node checks the single-wire pin DIAG1/SW for correctly received datagrams with its own address continuously. The pin is switched as input during this time. It adapts to the baud rate based on the sync nibble, as described earlier. In case of a read access, it switches on its output driver on the DIAG1/SW and sends its response using the same baud rate.

Table 7. TMC2241 UART Interface Signals

SIGNAL	DESCRIPTION
DIAG1/SW	Data input and output
CSN/AD2	Bit 2 of UART address increment (+4)
SCK/AD1	Bit 1 of UART address increment (+2)
SDI/AD0	Bit 0 of UART address increment (+1), tie to NAO of previous IC in chain
SDO/NAO	NAO pin for chained sequential addressing scheme (reset default = high)

Addressing Multiple Nodes

If only one or up to eight TMC2241 are addressed by a host using a single UART bus interface, a simple hardware address selection can be used. The individual UART node addresses are set by connecting the UART address pins (SDI, SCK, and CSN) to V_{CC_IO} and GND.

If more than eight nodes must be connected to the same UART bus, then a different approach must be used. This approach can address up to 255 nodes by using the output NAO (SDO) as a selection pin for the bit 0 address pin of the next device. Proceed as follows:

- Tie all address pins as well as SDI/AD0 of the first TMC2241 to GND.
- Connect the SDO/NAO output of the first TMC2241 to the next node's address[0] pin (SDI/AD0). Connect further nodes in the same fashion.
- Now, the first node responds to address 0. The following nodes are set to address 1.
- Program the first TMC2241 to its specific node address. **Note:** Once a node is initialized with its node address, its SDO/NAO output, which is tied to the next node's address[0] pin (SDI/AD0), must be programmed to logic 0 to differentiate the next node from all following nodes.
- Now, the second node is accessible and can get its specific node address. Further nodes can be programmed to their specific node addresses sequentially.

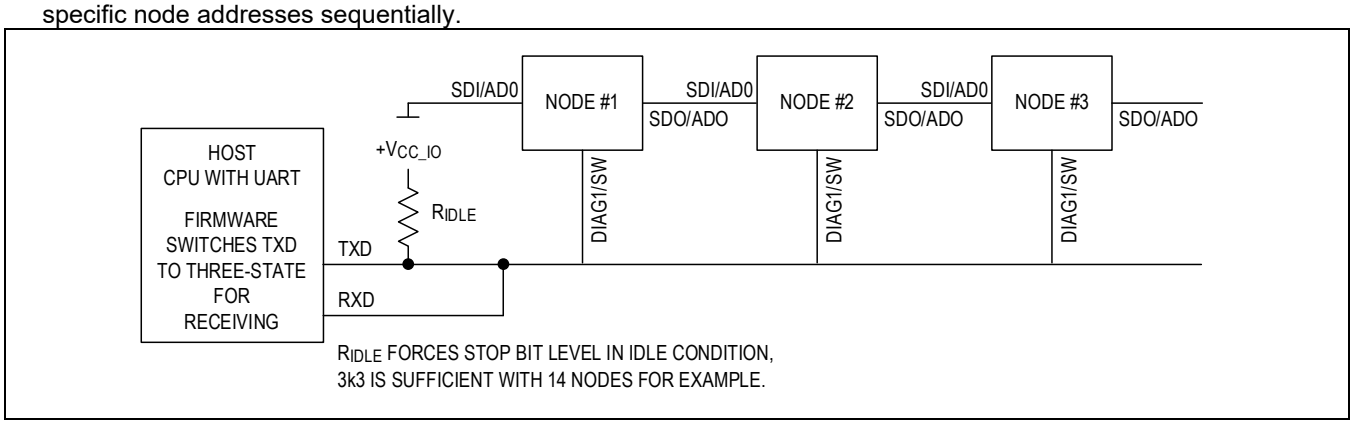


Figure 5. UART Daisy-Chaining Example

Table 8. UART Example for Addressing up to 255 Nodes

PHASE	NODE #1	NODE #2	NODE #3
Addressing phase 1	Address 0, NAO is high	Address 1	Address 1
Addressing phase 2	Program to address 254 and set NAO low	Address 0, NAO is high	Address 1
Addressing phase 3	Address 254	Program to address 253 and set NAO low	Address 0
Addressing phase 4	Address 254	Address 253	Program to address 252 and set NAO low
Addressing phase x	Continue procedure		

Step/Direction Interface

The STEP and DIR inputs provide a simple, standard interface compatible with many existing motion controllers. The MicroPlyer step pulse interpolator brings the smooth motor operation of high-resolution microstepping to applications originally designed for coarser stepping.

Timing

Figure 6 shows the timing parameters for the STEP and DIR signals. When the dedge mode bit in the CHOPCONF register is set, both edges of STEP are active. If the dedge is cleared, only rising edges are active. STEP and DIR are sampled and synchronized to the system clock. An internal analog filter of approximately 10ns removes glitches on the signals, such as those caused by long PCB traces. If the signal source is far from the chip, and especially if the signals are carried on cables, the signals should be filtered or transmitted differentially. See the **Electrical Characteristics** table for the specified timing parameters.

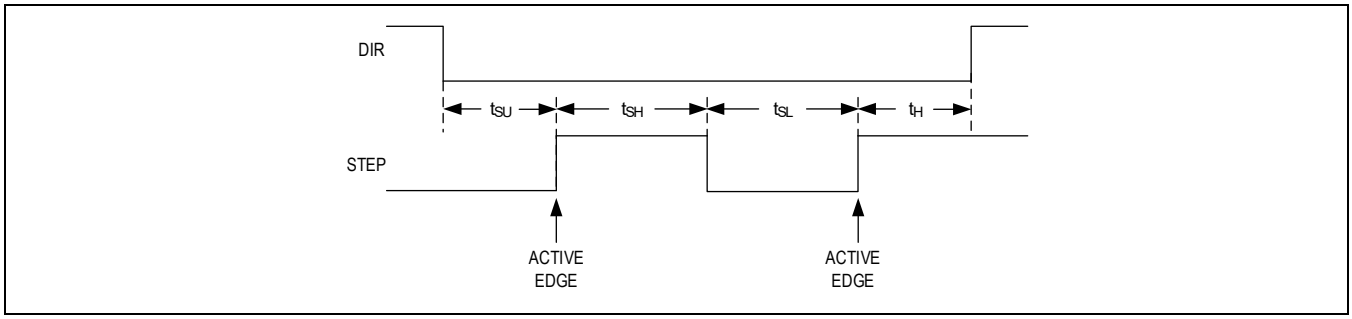


Figure 6. STEP/DIR Signal Timing

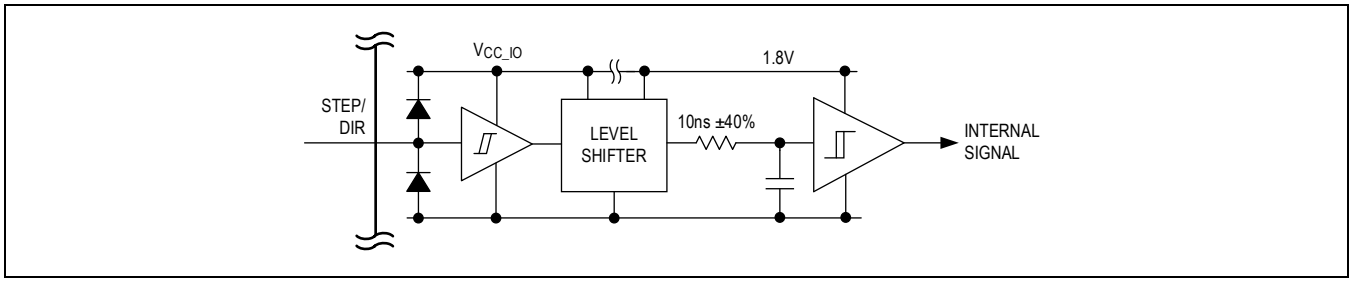


Figure 7. STEP/DIR Signal Input Filter Structure

Changing Resolution

A reduced microstep resolution allows to limit the step frequency for the STEP/DIR interface, or compatibility to an older, less performing driver. The internal microstep table with 1024 sine wave entries generates sinusoidal motor coil currents. These 1024 entries correspond to one electrical revolution or four fullsteps. The microstep resolution setting determines the step width taken within the table. Depending on the DIR input, the microstep counter is increased (DIR = 0) or decreased (DIR = 1) with each STEP pulse by the step width. The microstep resolution determines the increment, or respectively, the decrement. At maximum resolution, the sequencer advances one step for each step pulse. At half resolution, it advances two steps. The increment is up to 256 steps for fullstepping. The sequencer has special provision to allow seamless switching between different microstep rates at any time. When switching to a lower microstep resolution, it calculates the nearest step within the target resolution and reads the current vector at that position. This behavior especially is important for low resolutions like fullstep and halfstep, because any failure in the step sequence leads to an asymmetrical run when comparing a motor running clockwise and counterclockwise. **Examples:** Fullstep: Cycles through table positions: 128, 384, 640, and 896 (45°, 135°, 225°, and 315° electrical position, both coils on at identical current). The coil current in each position corresponds to the RMS value (0.71 x amplitude). The step size is 256 (90° electrical). Half step: The first table position is 64 (22.5° electrical). The step size is 128 (45° steps). Quarter step: The first table position is 32 (90°/8 = 11.25° electrical), The step size is 64 (22.5° steps). This way, equidistant steps result and they are identical in both rotation directions. Some older drivers also use zero current (table entry 0, 0°) as well as full current (90°) within the step tables. This kind of stepping is avoided because it provides less torque and has a worse power dissipation in the driver and motor.

Table 9. Fullstep/Half Step Lookup Table Values for Phase A/Phase B Coil Currents

STEP POSITION	TABLE POSITION	CURRENT COIL A	CURRENT COIL B
Half step 0	64	38.3%	92.4%
Full step 0	128	70.7%	70.7%
Half step 1	192	92.4%	38.3%
Half step 2	320	92.4%	-38.3%
Full step 1	384	70.7%	-70.7%
Half step 3	448	38.3%	-92.4%
Half step 4	576	-38.3%	-92.4%
Full step 2	640	-70.7%	-70.7%
Half step 5	704	-92.4%	-38.3%
Half step 6	832	-92.4%	38.3%
Fullstep 3	896	-70.7%	70.7%
Half step 7	960	-38.3%	92.4%

MicroPlyer Step Interpolator and Standstill Detection

For each active edge on STEP, MicroPlyer produces microsteps at 256x resolution. It interpolates the time in between the two step impulses at the step input based on the last step interval. This way, from two microsteps (128 microsteps to 256 microsteps interpolation) up to 256 microsteps (fullstep input to 256 microsteps) are driven for a single-step pulse.

MicroPlyer function is enabled by setting the intpol bit in the CHOPCONF register. The step rate for the interpolated two microsteps to 256 microsteps is determined by measuring the time interval of the previous step period and dividing it into up to 256 equal parts. The maximum time between two microsteps corresponds to 220 (roughly one million system clock cycles) for an even distribution of 256 microsteps. At 16MHz system clock frequency, this results in a minimum step input frequency of 16Hz for MicroPlyer operation. A lower step rate causes the STST bit to be set, which indicates a standstill event. At this frequency, microsteps occur at a rate of (system clock frequency)/216 ~ 256Hz. When a standstill is detected, the driver automatically switches the motor to holding current IHOLD.

Attention:

MicroPlyer only works perfectly with a stable STEP frequency. Do not use the DEDGE option if the STEP signal does not have a 50% duty cycle!

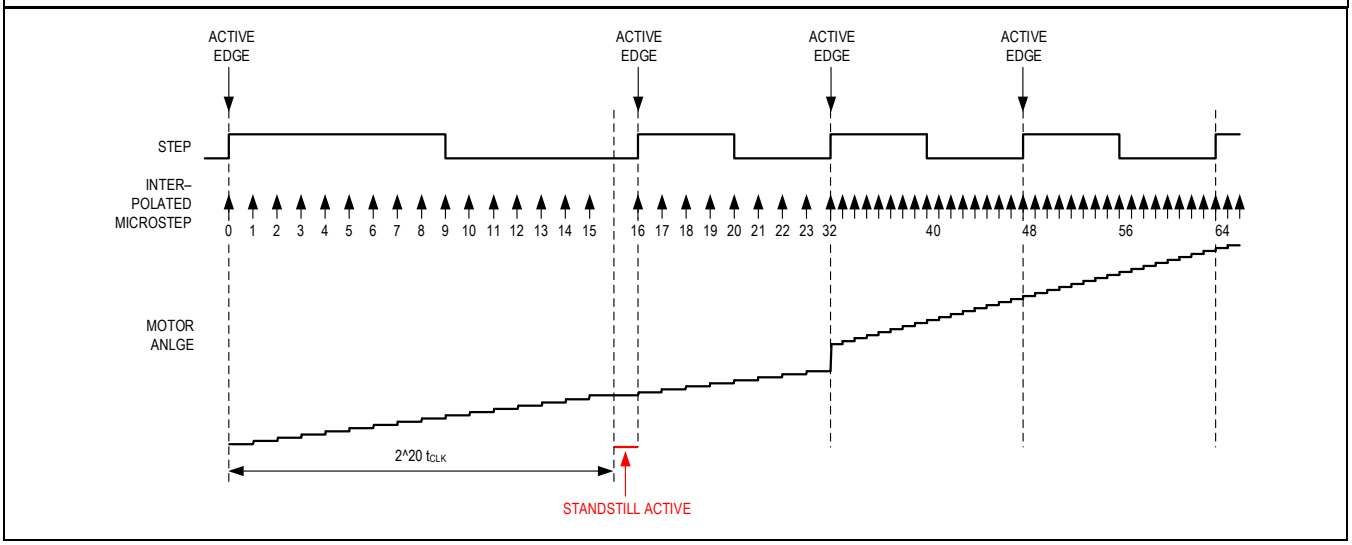


Figure 8. MicroPlyer Microstep Interpolation with Rising STEP Frequency (Example: 16 to 256)

The first STEP cycle is long enough to set the standstill bit stst in *Figure 8*. This bit is cleared on the next STEP active edge. Then, the external STEP frequency increases. After one cycle at the higher rate, MicroPlyer adapts the interpolated microstep rate to the higher frequency. During the last cycle at the slower rate, MicroPlyer does not generate all 16 microsteps. So, there is a small jump in motor angle between the first and second cycles at the higher rate.

StealthChop2

StealthChop2 is an extremely quiet mode of operation for stepper motors. It is based on a voltage mode pulse-width modulation (PWM). In case of standstill and at low velocities, the motor is absolutely noiseless. Thus, StealthChop2-operated stepper motor applications are highly suitable for indoor or home use. The motor operates absolutely free of vibration at low velocities.

With StealthChop, the motor current is applied by driving a certain effective voltage into the coil, using a voltage mode PWM. With the enhanced StealthChop2, the driver automatically adapts to the application for best performance. No more configurations are required. Optional configuration allows tuning the setting in special cases, or for setting initial values for the automatic adaptation algorithm. For high velocity drives, SpreadCycle should be considered in combination with StealthChop2.

Operate the motor within the application when exploring StealthChop2. Motor performance often is better with a mechanical load because it prevents the motor from stalling due to mechanical oscillations, which can occur without load.

Automatic Tuning

StealthChop2 integrates an automatic tuning (AT) procedure, which adapts the most important operating parameters to the motor automatically. This way, StealthChop2 allows high motor dynamics and supports powering down the motor to very low currents. Just two steps account for best results: start with the motor in standstill, but powered with nominal run current (AT#1). Move the motor at a medium velocity, for example, as part of a homing procedure (AT#2). The flowchart in *Figure 9* shows the tuning procedure.

Table 10. Constraints and Requirements for StealthChop2 Autotuning AT#1 and AT#2

STEP	PARAMETER	CONDITIONS	REQUIRED DURATION
AT#1	PWM_ OFS_AUTO	Motor in standstill and actual current scale (CS) is identical to run current (IRUN). If standstill reduction is enabled, an initial step pulse switches the drive back to run current, or set IHOLD to IRUN. Pin V_S at operating level.	≤ 2^{20} + 2 x 2^{18} t_{CLK}, ≤ 130ms (with internal clock)
AT#2	PWM_ GRAD_AUTO	Move the motor at a velocity, where a significant amount of back-EMF is generated and where the full run current can be reached. **Conditions:** 1.5 × PWM_OFS_AUTO × (IRUN +1)/32 < PWM_SCALE_SUM < 4 × PWM_OFS_AUTO × (IRUN + 1)/32 PWM_SCALE_SUM < 255 **Hint:** A typical range is 60RPM to 300RPM.	Eight fullsteps are required for a change of ±1. For a typical motor with PWM_GRAD_AUTO optimum at 50 or less, up to 400 fullsteps are required when starting from default value 0.

Hint: Determine the best conditions for automatic tuning with the evaluation board.

Use application-specific parameters for PWM_GRAD and PWM_OFS for initialization in the firmware to provide initial tuning parameters.

Monitor PWM_SCALE_AUTO going down to zero during the constant velocity phase in AT#2 tuning. This indicates a successful tuning.

Attention:

Operating in StealthChop2 without proper tuning can lead to high motor currents during a deceleration ramp, especially with low resistive motors and fast deceleration settings. Follow the automatic tuning process and check optimum tuning conditions using the evaluation board. It is recommended to use an initial value for settings PWM_OFS and PWM_GRAD determined per motor type.

Modifying GLOBALSCALER or V_S voltage invalidates the result of the automatic tuning process. Motor current regulation cannot compensate significant changes until the next AT#1 phase. Automatic tuning adapts to changed conditions whenever AT#1 and AT#2 conditions are fulfilled in the later operation.

StealthChop2 Options

To match the motor current to a certain level, the effective PWM voltage is scaled depending on the actual motor velocity. Several additional factors influence the required voltage level to drive the motor at the target current: the motor resistance, its back-EMF (for example, directly proportional to its velocity), as well as the actual level of the supply voltage. Two modes of PWM regulation are provided: the automatic tuning mode (AT) using current feedback (pwm_autoscale = 1, pwm_autograd = 1), and a feed-forward velocity-controlled mode (pwm_autoscale = 0).

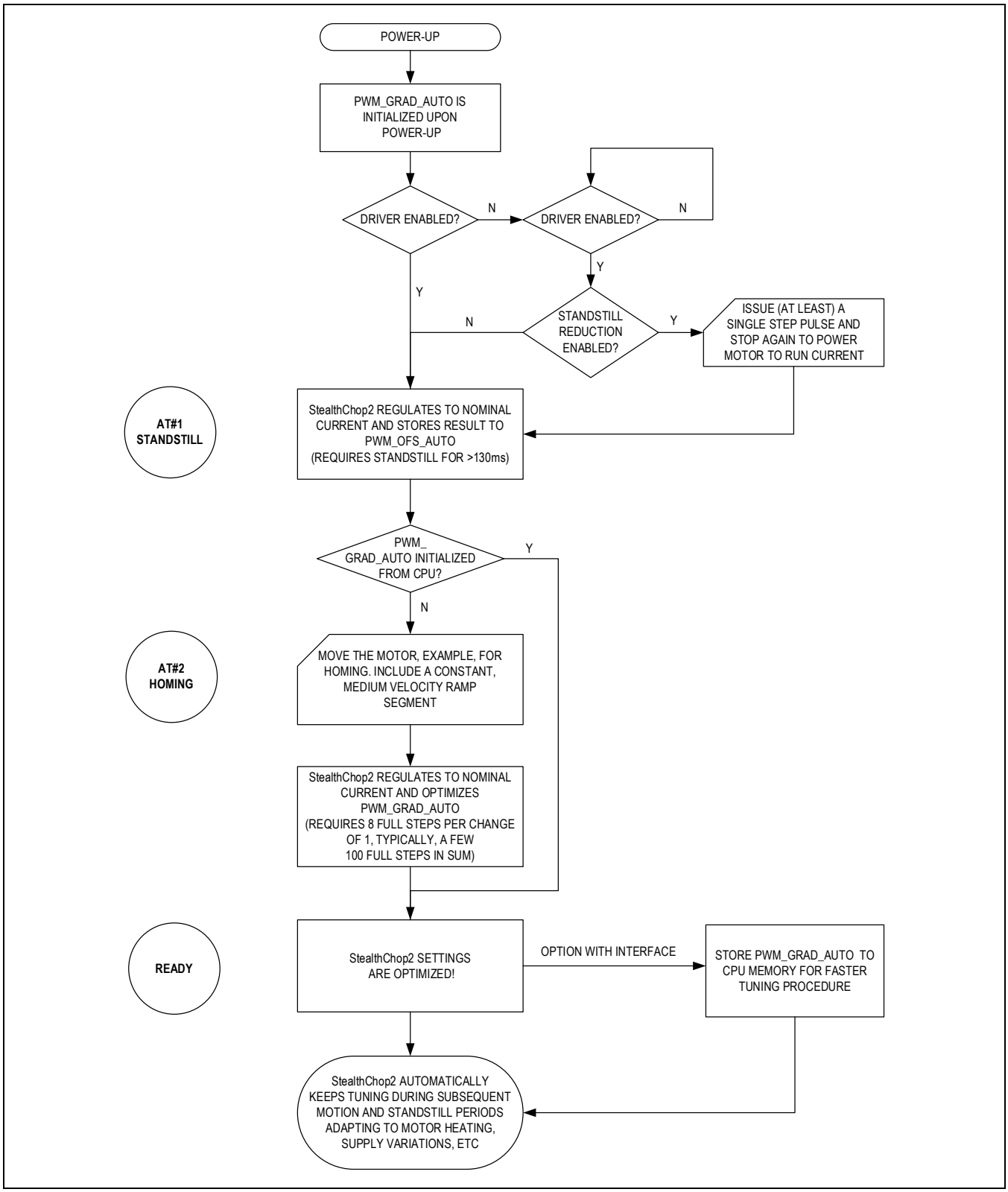


Figure 9. StealthChop2 Automatic Tuning Procedure

The feed-forward velocity-controlled mode does not react to a change of the supply voltage or to events like a motor stall, but it provides very stable amplitude. It does not use or require any means of current measurement. This is perfect when the motor type and supply voltage are well known. Therefore, the automatic mode is recommended, unless current regulation is not satisfying in the given operating conditions.

It is recommended to use application-specific initial tuning parameters, fitting the motor type and supply voltage. Additionally, operate in the automatic tuning mode to respond to parameter change, for example, due to motor heat-up or change of supply voltage.

The non-automatic mode (pwm_autoscale = 0) should be considered only with well-known motor and operating conditions. In this case, careful programming using the interface is required. The operating parameters PWM_GRAD and PWM_OFS can be determined initially in the automatic tuning mode.

The StealthChop2 PWM frequency can be chosen in four steps to adapt the frequency divider to the frequency of the clock source. A setting in the range of 20kHz to 50kHz is good for most applications. It balances low current ripple and good higher velocity performance vs. dynamic power dissipation.

Table 11. Choice of PWM Frequency for StealthChop2

CLOCK FREQUENCY f_{CLK}	PWM_FREQ = %00 $f_{PWM} = 2/1024\ f_{CLK}$	PWM_FREQ = %01 $f_{PWM} = 2/683\ f_{CLK}$	PWM_FREQ = %10 $f_{PWM} = 2/512\ f_{CLK}$	PWM_FREQ = %11 $f_{PWM} = 2/410\ f_{CLK}$
20MHz	39.1kHz	58.1kHz	78.1kHz	97.6kHz
18MHz	35.2kHz	52.7kHz	70.3kHz	87.8kHz
16MHz	31.3kHz	46.9kHz	62.5kHz	78.0kHz
12.5MHz (Internal)	24.4kHz	36.6kHz	48.8kHz	61.0kHz
10MHz	19.5kHz	29.3kHz	39.1kHz	48.8kHz
8MHz	15.6kHz	23.4kHz	31.2kHz	39.0kHz

StealthChop2 Current Regulator

In the StealthChop2 voltage PWM mode, the autoscaling function (pwm_autoscale = 1, pwm_auto_grad = 1) regulates the motor current to the desired current setting. Automatic scaling is used as part of the AT process, and for subsequent tracking of changes within the motor parameters. The driver measures the motor current during the chopper on-time and uses a proportional regulator to regulate PWM_SCALE_AUTO to match the motor current to the target current. PWM_REG is the proportionality coefficient for this regulator. Basically, the proportionality coefficient should be as small as possible to get a stable and soft regulation behavior, but it must be large enough to allow the driver to quickly react to changes caused by the variation of application parameters, for example, change of motor load or supply voltage. (V_{REF} is not variable on this device family). During the initial tuning step AT#2, PWM_REG also compensates for the change of motor velocity. Therefore, a high acceleration during AT#2 requires a higher setting of PWM_REG. With careful selection of homing velocity and acceleration, a minimum setting of the regulation gradient often is sufficient (PWM_REG = 1). The PWM_REG setting should be optimized for the fastest required acceleration and deceleration ramp (compare the following two figures).

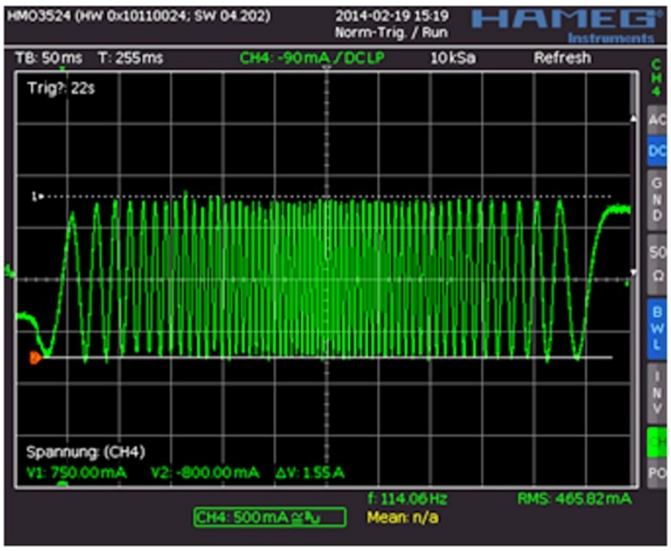


Figure 10. StealthChop2: Good Setting for PWM_REG

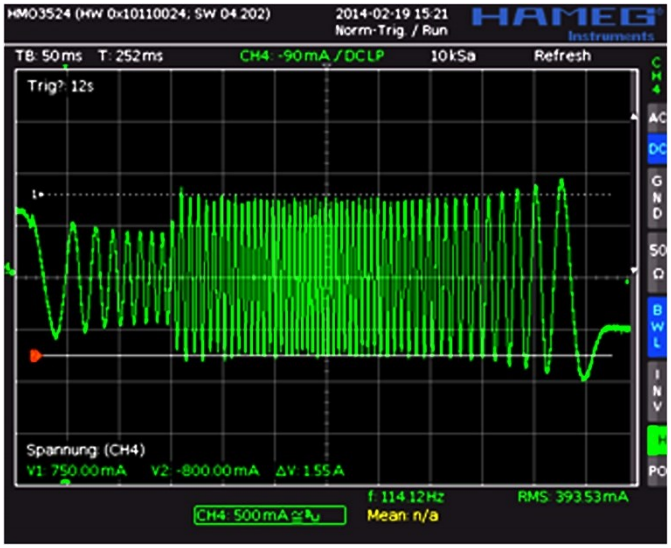


Figure 11. StealthChop2: Too Small Setting for PWM_REG During AT#2

The quality of the setting PWM_REG in phase AT#2 and the finished automatic tuning procedure (or non-automatic settings for PWM_OFS and PWM_GRAD) can be examined when monitoring the motor current during an acceleration phase, as shown in the following figure.

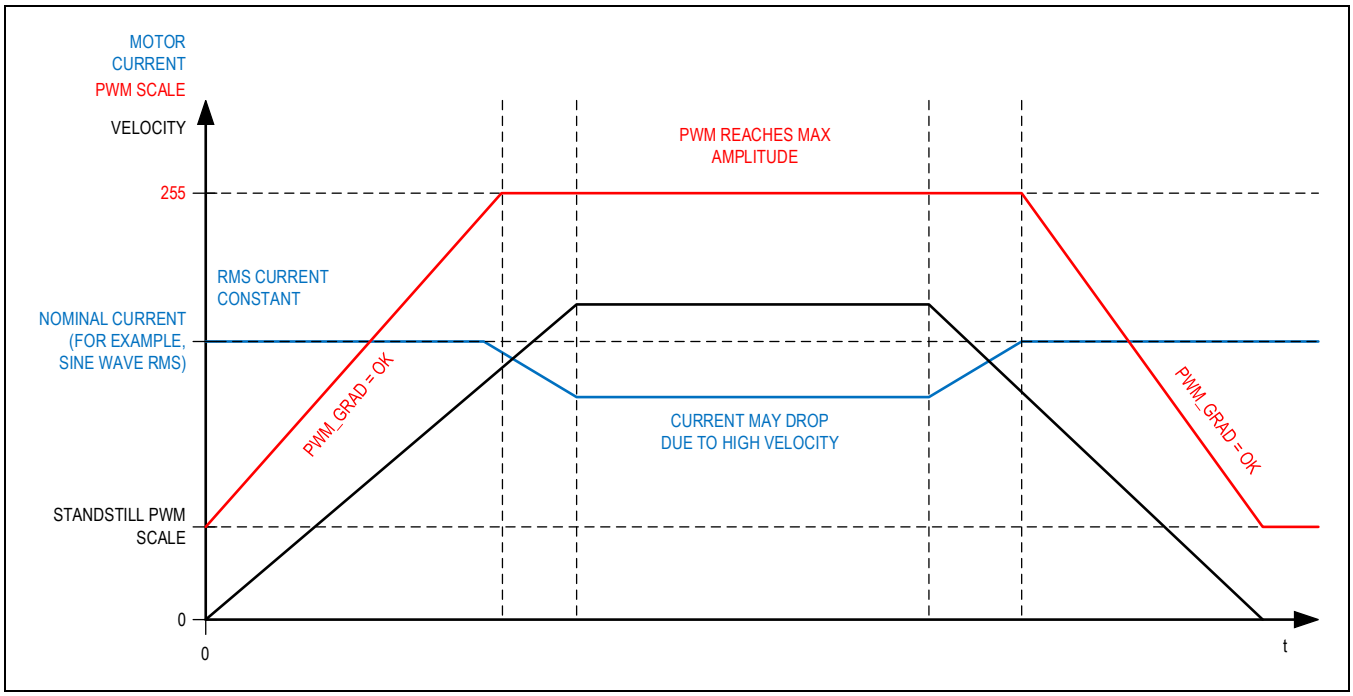


Figure 12. Successfully Determined PWM_GRAD(_AUTO) and PWM_OFS(_AUTO)

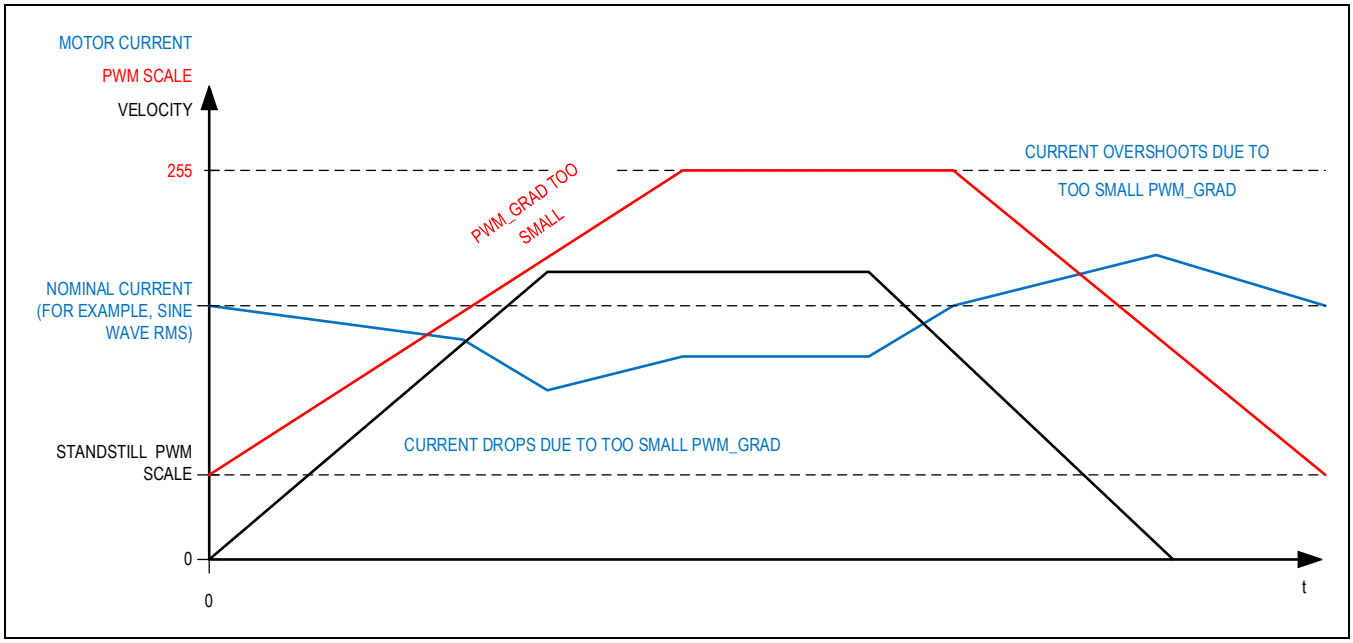


Figure 13. Example for Too Small PWM_GRAD Setting

Lower Current Limit

Depending on the setting of pwm_meas_sd_enable, the StealthChop2 current regulator principle imposes a lower limit to regulate the motor current. As the coil current is measured during chopper-on phase only (pwm_meas_sd_enable = 0), a minimum chopper duty cycle allowing coil current regulation is given by the blank time as set by TBL and by the chopper frequency setting. Therefore, the motor-specific minimum coil current in StealthChop2 autoscaling mode rises with the supply voltage and with the chopper frequency. A lower blanking time allows a lower current limit. It is important for the correct determination of PWM_OFS_AUTO, that in AT#1, the run current, GLOBALSCALER, and IRUN are well within the regulation range. Lower currents (example, for standstill power down) are automatically realized based on

PWM_OFS_AUTO and PWM_GRAD_AUTO, respectively, based on PWM_OFS and PWM_GRAD with non-automatic current scaling. The freewheeling option allows going to zero motor current.

Lower motor coil current limit for StealthChop2 automatic tuning (pwm_meas_sd_enable = 0):

$$I_{LowerLimit} = t_{BLANK} \times f_{PWM} \times \frac{V_S}{R_{COIL}}$$

V_S being the motor supply voltage and R_{COIL} the motor coil resistance.

$I_{LOWERLIMIT}$ can be treated as a rule-of-thumb value for the minimum nominal IRUN motor current setting. In case where the lower limit is not sufficient to reach the desired setting, be sure to set pwm_meas_sd_enable = 1.

f_{PWM} is the chopper frequency, as determined by setting PWM_FREQ.

Example: A motor has a coil resistance of 5Ω, the supply voltage is 24V. With TBL = %01 and PWM_FREQ = %00, t_{BLANK} is 24 clock cycles, f_{PWM} is 2/(1024 clock cycles):

$$I_{LOWERLIMIT} = 24t_{clk} \times \frac{2}{1024t_{CLK}} \times \frac{24V}{5\Omega} = \frac{24}{512} \times \frac{24V}{5\Omega} = 225mA$$

This means the motor target current for automatic tuning must be 225mA or more, taking into account all relevant settings. This lower current limit also applies when modifying the motor current through the GLOBALSCALER.

Attention:

For automatic tuning, a lower coil current limit applies.

IRUN ≥ 8: current settings for IRUN below 8 do not work with automatic tuning.

$I_{LOWERLIMIT}$: Depending on the setting of bit pwm_meas_sd_enable (in register PWM_CONF[22]) for automatic tuning, a lower coil current limit applies. The motor current in the automatic tuning phase AT#1 must exceed this lower limit. Calculate $I_{LOWERLIMIT}$ or measure it using a current probe. Setting the motor run-current or hold-current below the lower current limit during operation by modifying IRUN and IHOLD is possible after successful automatic tuning.

The lower current limit also limits the capability of the driver to respond to the changes of the GLOBALSCALER.

To overcome the restriction by the lower limit, set pwm_meas_sd_enable = 1. This allows the IC to additionally measure coil current in the slow decay phase.

Velocity-Based Scaling

Velocity-based scaling scales the StealthChop2 amplitude based on the time between every two steps, for example, based on TSTEP, measured in clock cycles. This concept basically does not require a current measurement, because no regulation loop is necessary. A pure velocity-based scaling is available through programming, only when setting pwm_autoscale = 0. The basic idea is to have a linear approximation of the voltage required to drive the target current into the motor. The stepper motor has a certain coil resistance, and thus, needs a certain voltage amplitude to yield a target current based on the basic formula I = U/R. With R being the coil resistance, U the supply voltage scaled by the PWM value, the current I results. The initial value for PWM_OFS can be calculated as:

$$PWM\_OFS = \frac{374 \times R_{COIL} \times I_{COIL}}{V_S}$$

V_S is the motor supply voltage and I_{COIL} the target RMS current.

The effective PWM voltage U_{PWM} (1/SQRT(2) x peak value) results, considering the 8-bit resolution and 248 sine wave peak for the actual PWM amplitude shown as PWM_SCALE:

$$U_{PWM} = V_S \times \frac{PWM\_SCALE}{256} \times \frac{248}{256} \times \left(\frac{CS\_ACTUAL + 1}{32}\right) + PWM\_GRAD \times \frac{PWM\_SCALE}{374}$$

With rising motor velocity, the motor generates an increasing back-EMF voltage. The back-EMF voltage is proportional to the motor velocity. It reduces the PWM voltage effective at the coil resistance, and thus, current decreases. The TMC2241 provides a second velocity dependent factor (PWM_GRAD) to compensate for this. The overall effective PWM amplitude (PWM_SCALE_SUM) in this mode is calculated automatically in dependence of the microstep frequency as:

$$PWM\_SCALE\_SUM = PWM_{OFS} \times \left(\frac{CS\_ACTUAL + 1}{32}\right) + PWM\_GRAD \times \frac{256}{TSTEP}$$

CS_ACTUAL takes into account the actual current scaling, as defined by IHOLD and IRUN, or respectively, by CoolStep.

f_{STEP} is the microstep frequency for 256 microsteps resolution equivalent and f_{CLK} the clock frequency supplied to the driver or the actual internal frequency.

As a first approximation, the back-EMF subtracts from the supply voltage, and thus, the effective current amplitude decreases. This way, a first approximation for the PWM_GRAD setting can be calculated as:

$$PWM\_GRAD = C_{BEMF} \left| \frac{V}{\frac{rad}{s}} \right| \times 2\pi \times \frac{f_{clk} \times 1.46}{V_M \times MSPR}$$

C_{BEMF} is the back-EMF constant of the motor in Volts per radian/second.

MSPR is the number of microsteps per rotation related to 1/256 microstep resolution, example, 51200 = 256 microsteps multiplied by 200 fullsteps for a 1.8° motor.

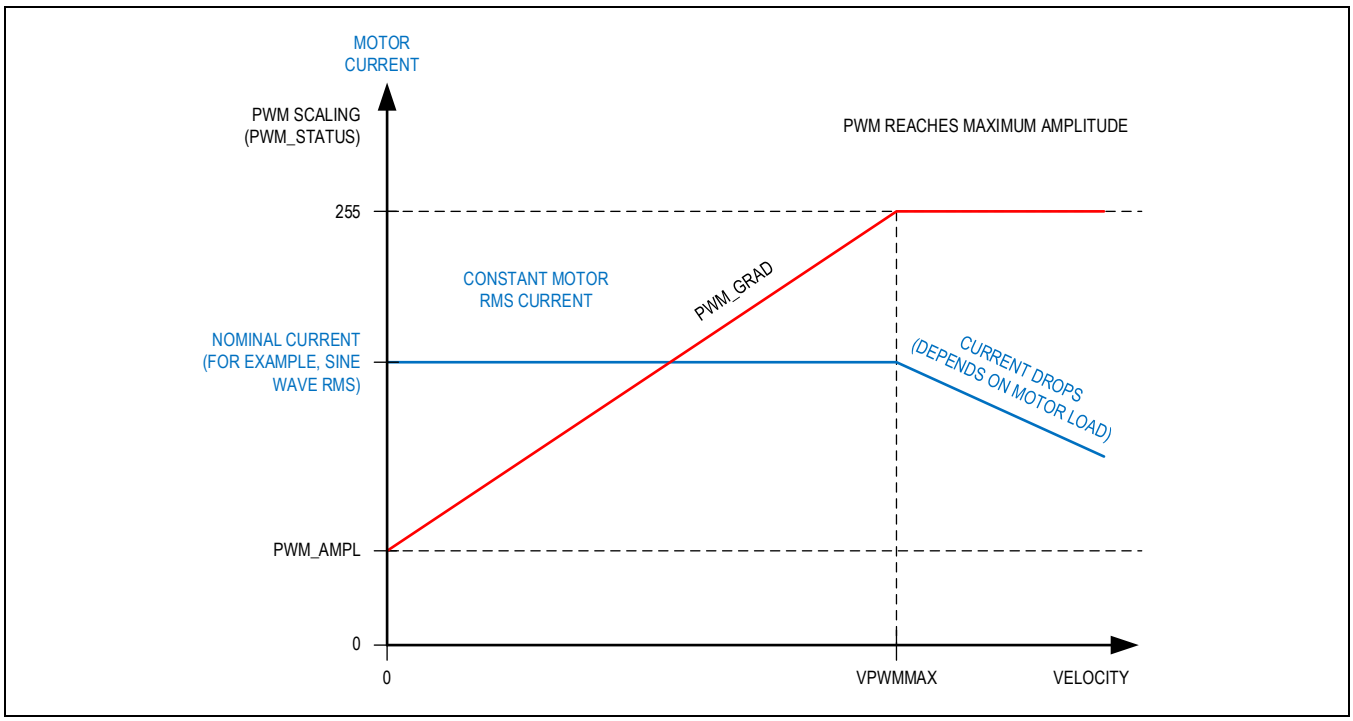


Figure 14. Velocity-Based PWM Scaling (pwm_autoscale = 0)

The values for PWM_OFS and PWM_GRAD can easily be optimized by tracing the motor current with a current probe on the oscilloscope. Alternatively, automatic tuning determines these values and they can be read out from PWM_OFS_AUTO and PWM_GRAD_AUTO.

Understanding the Back-EMF Constant of a Motor

The back-EMF constant is the voltage a motor generates when turned with a certain velocity. Often, motor data sheets do not specify this value, as it can be deducted from the motor torque and coil current rating. Within SI units, the numeric value of the back-EMF constant C_{BEMF} has the same numeric value as the numeric value of the torque constant. For example, a motor with a torque constant of 1 Nm/A has a C_{BEMF} of 1V/rad/s. Turning such a motor with 1rps (1rps = 1 revolution per second = 6.28 rad/s) generates a back-EMF voltage of 6.28V. Thus, the back-EMF constant can be calculated as:

$$C_{BEMF} = \left| \frac{V}{\frac{rad}{s}} \right| = \frac{HoldingTorque[Nm]}{2 \times I_{COILNOM[A]}}$$

$I_{COILNOM}$ is the motor's rated RMS phase current for the specified holding torque.

HoldingTorque is the motor-specific holding torque, for example, the torque reached at $I_{COILNOM}$ on both coils. The torque unit is [Nm], where 1Nm = 100Ncm = 1000mNm.

The voltage is valid as RMS voltage per coil. Thus, the nominal current is multiplied by two in this formula, as the nominal current assumes a fullstep position, with two coils operating.

Combining StealthChop2 and SpreadCycle

For applications requiring high velocity motion, SpreadCycle may bring more stable operation in the upper velocity range. To combine no-noise operation with highest dynamic performance, the TMC2241 allows combining StealthChop2 and SpreadCycle based on a velocity threshold. With this, StealthChop2 is only active at low velocities.

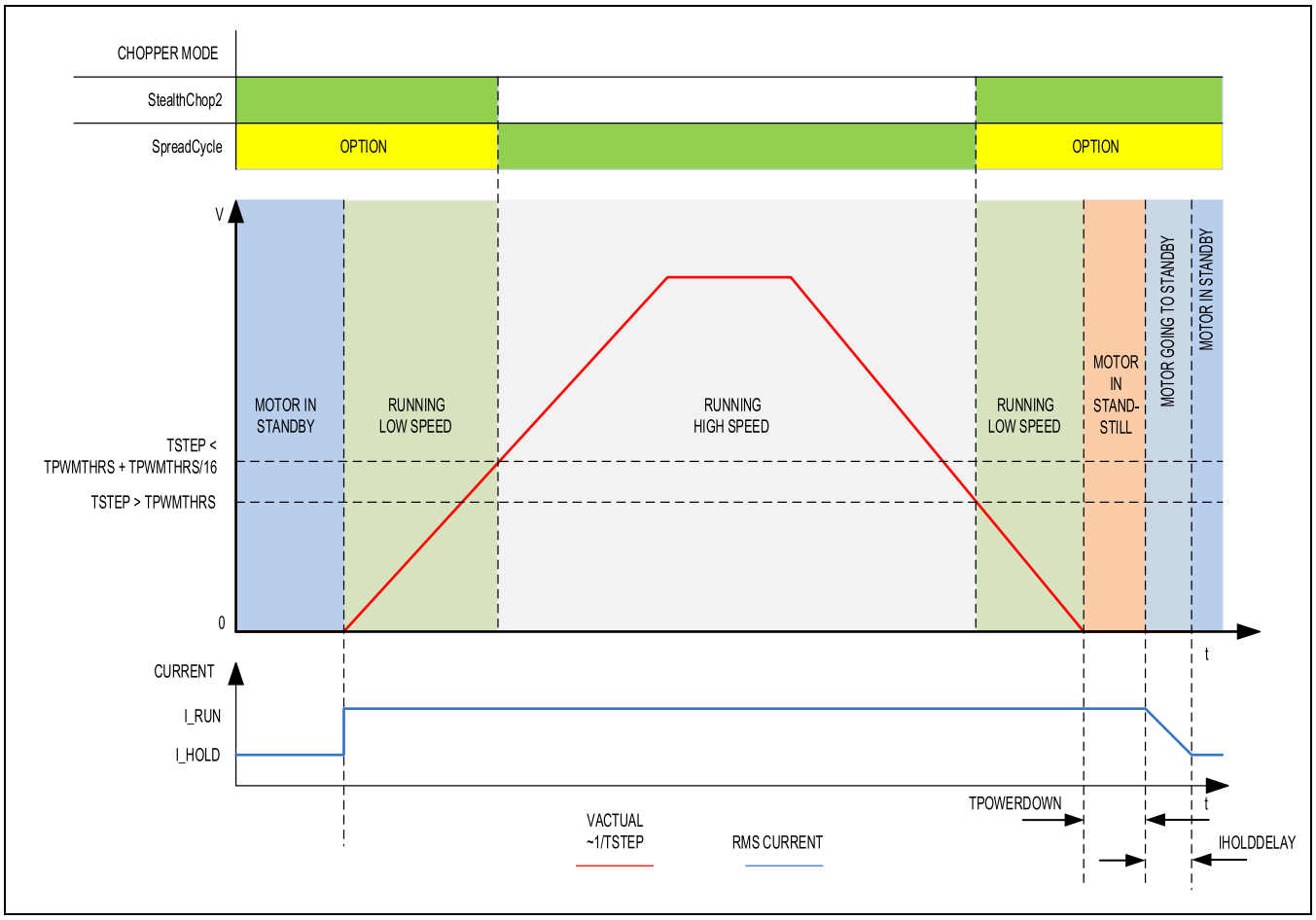


Figure 15. TPWMTHRS for Optional Switching to SpreadCycle

As a first step, both chopper principles should be parameterized and optimized individually.

In the next step, the switchover velocity must be defined. For example, StealthChop2 operation is used for precise low speed positioning, while SpreadCycle can be used for highly dynamic motion. TPWMTHRS determines this transition velocity. Read out TSTEP when moving at the desired velocity and program the resulting value to TPWMTHRS. Use a low transfer velocity to avoid a jerk at the switching point.

Jerkless Switching to SpreadCycle

A jerk occurs when switching at higher velocities because the back-EMF of the motor (which rises with the velocity) causes a phase shift of up to 90° between the motor voltage and motor current. So, when switching at higher velocities between the voltage PWM and current PWM mode, this jerk occurs with increased intensity. A high jerk may even produce a temporary overcurrent condition (depending on the motor coil resistance). At low velocities (example, 1RPM to a few 10RPM), it can be completely neglected for most motors. Therefore, consider the jerk when switching the driver between SpreadCycle and StealthChop2. With automatic switching controlled by TPWMTHRS, the driver can automatically eliminate the jerk using StallGuard4 to determine the phase shift. It applies the same phase shift to SpreadCycle until the velocity falls back below the switching threshold. Set flag SG4_THRS.sg_angle_offset to enable this function.

Set TPWMTHRS to zero to work with StealthChop2 only.

When enabling the StealthChop2 mode the first time using automatic current regulation, the motor must be at standstill to allow a proper current regulation. When the drive switches to SpreadCycle at a higher velocity, StealthChop2 logic stores the last current regulation setting until the motor returns to a lower velocity again. This way, the regulation has a known starting point when returning to a lower velocity, where StealthChop2 is re-enabled. Therefore, neither the velocity threshold nor the supply voltage must be considerably changed during the phase while the chopper is switched to a different mode, because otherwise, the motor might lose steps or the instantaneous current might be too high or too low.

A motor stall or a sudden change in the motor velocity may lead to the driver detecting a short circuit or to a state of automatic current regulation, from which it cannot recover. Clear the error flags and restart the motor from zero velocity to recover from this situation.

Start the motor from standstill when switching on StealthChop2 the first time and keep it stopped for at least 128 chopper periods to allow StealthChop2 to do the initial standstill current control.

Flags in StealthChop2

As StealthChop2 uses voltage mode driving, status flags based on current measurement respond slower, respectively, the driver reacts delayed to sudden changes of back-EMF, like on a motor stall.

A motor stall, or abrupt stop of the motion during operation in StealthChop2 can lead to an overcurrent condition. Depending on the previous motor velocity, and on the coil resistance of the motor, it significantly increases motor current for several 10ms. With low velocities, where the back-EMF is just a fraction of the supply voltage, there is no danger of triggering the short detection.

Switch the driver stage to the lowest current range (DRV_CONF.current_range) supporting the motor. This automatically adapts the overcurrent threshold in three steps, and thus, reduces peak currents in case of a sudden motor stall.

Open Load Flags

In StealthChop2 mode, the status information is different compared to the cycle-by-cycle regulated SpreadCycle mode for the flags OLA and OLB.

- If OLA and OLB are not set, the current regulation reaches the nominal current on both coils.
- If OLA and OLB flags are constant, an interrupted motor coil occurs.
- If OLA and OLB are flickering, differences in the motor coil resistance occur, exceeding roughly 5%.
- One or both flags are active, if the current regulation does not succeed in scaling up to the full target current within the last few fullsteps (because no motor is attached or a high velocity exceeds the PWM limit).

If desired, do an on-demand open load test using the SpreadCycle chopper as it delivers the safest result. With StealthChop2, PWM_SCALE_SUM can be checked to detect the correct coil resistance.

PWM_SCALE_SUM Informs about the Motor State

Information about the motor state is available with automatic scaling by reading out PWM_SCALE_SUM. As this parameter reflects the actual voltage required to drive the target current into the motor, it depends on several factors: motor load, coil resistance, supply voltage, and current setting. Therefore, an evaluation of the PWM_SCALE_SUM value allows checking the motor operation point. When reaching the limit (1023), the current regulator cannot sustain the full motor current, for example, due to a permanent or temporary drop in supply voltage.

Freewheeling and Passive Braking

StealthChop2 provides different options for motor standstill. These options can be enabled by setting the standstill current IHOLD to zero and choosing the desired option using the FREEWHEEL setting. The desired option is enabled after a time period specified by TPOWERDOWN and IHOLDDELAY. The current regulation is frozen once the motor target

current is at zero current to ensure a quick start-up. With the freewheeling options, both freewheeling and passive braking can be realized. Passive braking is an effective eddy current motor braking, which consumes a minimum amount of energy because no active current is driven into the coils. However, passive braking allows slow turning of the motor when a continuous torque is applied.

Parameters Controlling StealthChop2

The following table contains all parameters related to the StealthChop2 chopper mode.

Table 12. Parameters Controlling StealthChop2

PARAMETER	DESCRIPTION	SETTING	COMMENT
en_pwm_ mode	General enable for use of StealthChop2 (register GCONF). Default = 0	0	StealthChop2 disabled. SpreadCycle active.
		1	StealthChop2 enabled (depending on velocity thresholds). Enable only while in standstill and at IHOLD = nominal IRUN current.
pwm_meas_sd_enable	Control of current measurement during slow decay phase. Default = 0	0	Current measured during on-phases only. Lower current limit applies.
		1	Current measured during slow decay phases additionally to overcome lower current limit.
pwm_dis_reg_stst	This option eliminates any regulation noise during standstill. Default = 0	0	Current regulation always on.
		1	Disable current regulation when motor is in standstill and current is reduced (less than IRUN).
TPWMTHRS	Specifies the upper velocity for operation in StealthChop2. Enter the TSTEP reading (time between two microsteps) when operating at the desired threshold velocity. Default = 0	0 … 1048575	StealthChop2 is disabled if TSTEP falls under TPWMTHRS.
PWM_LIM	Limiting value for limiting the current jerk when switching from SpreadCycle to StealthChop2. Reduce the value to yield a lower current jerk. Default = 12	0 … 15	Upper four bits of 8-bit amplitude limit
pwm_ autoscale	Enable automatic current scaling using current measurement. If off, use forward-controlled velocity-based mode. Default = 1	0	Forward-controlled mode
		1	Automatic scaling with current regulator
pwm_ autograd	Enable automatic tuning of PWM_GRAD_AUTO. Default = 1	0	Disable, use PWM_GRAD from register instead.
		1	Enable
PWM_FREQ	PWM frequency selection. Use the lowest setting giving good results. The frequency measured at each of the chopper outputs is half of the effective chopper frequency f_{PWM}. Default = 0	0	$f_{PWM} = 2/1024\ f_{CLK}$
		1	$f_{PWM} = 2/683\ f_{CLK}$
		2	$f_{PWM} = 2/512\ f_{CLK}$
		3	$f_{PWM} = 2/410\ f_{CLK}$

PWM_REG	User-defined PWM amplitude regulation loop P-coefficient. A higher value leads to a higher adaptation speed when pwm_autoscale = 1. Default = 4	1 … 15	Results in 0.5 to 7.5 steps for PWM_SCALE_AUTO regulator per fullstep.
PWM_OFS	User-defined PWM amplitude (offset) for velocity-based scaling and initialization value for automatic tuning of PWM_OFFS_AUTO. Default = 0x1D	0 … 255	PWM_OFS = 0 disables linear current scaling based on current setting.
PWM_GRAD	User-defined PWM amplitude (gradient) for velocity-based scaling and initialization value for automatic tuning of PWM_GRAD_AUTO. Default = 0	0 … 255	
PWM_SCALE_SUM	Actual PWM scaling as determined by the actual settings. This value is shown in higher precision (10-bit) compared to 8-bit for PWM_GRAD/OFS_AUTO values. Default = 0	0 ... 1023	
FREEWHEEL	Standstill option when motor current setting is zero (I_HOLD = 0). Only available with StealthChop2 enabled. The freewheeling option makes the motor easily movable, while both coil short options realize a passive brake. Default = 0	0	Normal operation
		1	Freewheeling
		2	Coil short using LS drivers
		3	Coil short using HS drivers
PWM_SCALE _AUTO	Read back of the actual StealthChop2 voltage PWM scaling correction, as determined by the current regulator. Shall regulate close to 0 during tuning. Default = 0	-255 … 255	(Read-only) Scaling value is frozen when operating in SpreadCycle.
PWM_GRAD _AUTO PWM_OFS _AUTO	Allow monitoring of the automatic tuning and determination of initial values for PWM_OFS and PWM_GRAD. Default = 0	0 … 255	(Read-only)
TOFF	General enable for the motor driver. The actual value does not influence StealthChop2. Default = 0	0	Driver off
		1 … 15	Driver enabled
TBL	Comparator blank time. Choose a setting of 1 or 2 for typical applications. For higher capacitive loads, 3 may be required. Lower settings allow StealthChop2 to regulate down to lower coil current values. Default = 2	0	16 t_{CLK}
		1	24 t_{CLK}
		2	36 t_{CLK}
		3	54 t_{CLK}

SpreadCycle and Classic Chopper

While StealthChop2 is a voltage-mode PWM-controlled chopper, SpreadCycle is a cycle-by-cycle current control. Therefore, it can react extremely fast to changes in motor velocity or motor load. The currents through both motor coils are controlled using choppers. The choppers work independent of each other. The following figure shows the different chopper phases.

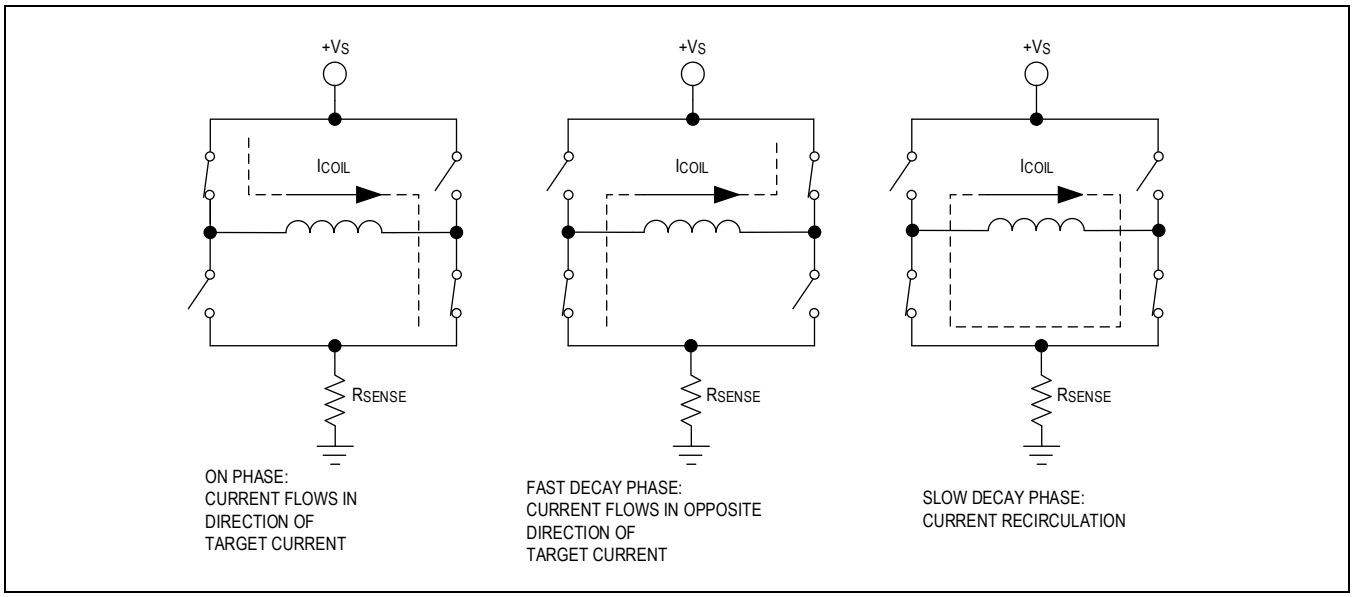


Figure 16. Typical Chopper Decay Phases

Although the current can be regulated using only on-phases and fast decay phases, insertion of the slow decay phase is important to reduce electrical losses and current ripple in the motor. The duration of the slow decay phase is specified in a control parameter and sets an upper limit on the chopper frequency. The current comparator measures the coil current during phases when the current flows through exactly one low-side transistor, but not during the slow decay phase. The slow decay phase is terminated by a timer. The on-phase is terminated by the comparator when the current through the coil reaches the target current. The fast decay phase may be terminated by either the comparator or another timer.

When the coil current is switched, spikes in the $R_{DS(ON)}$-based current measurement occur due to charging and discharging the parasitic capacitance. During this time, typically, one or two microseconds, the current cannot be measured. Blanking is the time when the input to the comparator is masked to block these spikes.

There are two cycle-by-cycle chopper modes available: a new high-performance chopper algorithm called SpreadCycle and a proven constant off-time chopper mode. The constant off-time mode cycles through three phases: on, fast decay, and slow decay. The SpreadCycle mode cycles through four phases: on, slow decay, fast decay, and a second slow decay.

The chopper frequency is an important parameter for a chopped motor driver. A too low frequency might generate audible noise. A higher frequency reduces current ripple in the motor, but with a too high frequency, magnetic losses may rise. Also, power dissipation in the driver rises with increasing frequency due to the increased influence of switching slopes causing dynamic dissipation. Therefore, a compromise is necessary. Most motors optimally work in a frequency range of 25kHz to 40kHz. The chopper frequency is influenced by a number of parameter settings as well as by the motor inductivity and supply voltage.

Hint: A chopper frequency in the range of 25kHz to 40kHz gives a good result for most motors when using SpreadCycle. A higher frequency leads to increased switching losses.

Table 13. Parameters Controlling SpreadCycle and Classic Constant Off-Time Chopper

PARAMETER	DESCRIPTION	SETTING	COMMENT
TOFF	Sets the slow decay time (off time). This setting also limits the maximum chopper frequency. For operation with StealthChop2, this parameter is not used, but it is required to enable the motor. In case of operation with StealthChop2 only, any setting is OK.	0	Chopper off
		1…15	Off time setting N_{CLK} = 24 + 32 × TOFF (1 works with minimum blank time of 24 clocks)

	Setting this parameter to zero completely disables all driver transistors and the motor can freewheel. Default = 0		
TBL	Selects the comparator blank time. This time must safely cover the switching event and duration of the ringing. For most applications, a setting of 1 or 2 is good. For highly capacitive loads, for example, when filter networks are used, a setting of 2 or 3 is required. Default = 2	0	16 t_{CLK} **Restriction:** Use this setting only in combination with an external clock oscillator <= 8MHz.
		1	24 t_{CLK} **Restriction:** May be used with internal clock, or if external clock frequency <=13MHz is applied.
		2	36 t_{CLK}
		3	54 t_{CLK}
chm	Selecting the chopper mode. Default = 0	0	SpreadCycle
		1	Classic constant off-time

SpreadCycle Chopper

The SpreadCycle (patented) chopper algorithm is a precise and simple-to-use chopper mode, which automatically determines the optimum length for the fast decay phase. The SpreadCycle provides superior microstepping quality even with default settings. Several parameters are available to optimize the chopper to the application.

Each chopper cycle comprises an on-phase, a slow decay phase, a fast decay phase, and a second slow decay phase. The two slow decay phases and the two blank times per chopper cycle put an upper limit to the chopper frequency. The slow decay phases typically make up for about 30% to 70% of the chopper cycle in standstill and are important for low motor and driver power dissipation.

Example: Calculation of a starting value for the slow decay time TOFF:

Target chopper frequency: 25kHz
TOFF = (1kHz/25kHz) × (50/100) × 1/2 = 10µs
Assumption: Two slow decay cycles make up for 50% of the overall chopper cycle time.
For the TOFF setting, this means: TOFF = (TOFF × f_{CLK} − 24)/32.
With a 12MHz clock, this results in TOFF = 3.0, which requires a setting of TOFF = 3.
With a 16MHz clock, this results in TOFF = 4.25, which requires a setting of TOFF = 4.
Hint: Highest motor velocities sometimes benefit from setting TOFF to 1 or 2 and a short TBL setting.

The hysteresis start setting forces the driver to introduce a minimum amount of current ripple into the motor coils. The current ripple must be higher than the current ripple, which is caused by resistive losses in the motor to give the best microstepping results. This allows the chopper to precisely regulate the current for both the rising and falling target current. The time required to introduce the current ripple into the motor coil also reduces the chopper frequency. Therefore, a higher hysteresis setting leads to a lower chopper frequency. The motor inductance limits the ability of the chopper to follow a changing motor current. Further, the duration of the on-phase and the fast decay must be longer than the blanking time, because the current comparator is disabled during blanking.

It is easiest to find the best setting by starting from a low hysteresis setting (example, HSTRT = 0, HEND = 0) and increasing HSTRT, until the motor runs smoothly at low velocity settings. This can best be checked when measuring the motor current with a current probe. Checking the sine wave shape near the zero transition shows a small ledge between both the half waves in case the hysteresis setting is too small. At medium velocities (example, 100 fullsteps to 400 fullsteps per second), a too low hysteresis setting leads to increased humming and vibration of the motor. A too high hysteresis setting leads to reduced chopper frequency and increased chopper noise but does not yield any benefit for the wave shape.

As experiments show, the setting is quite independent of the motor because higher current motors typically also have a lower coil resistance. Therefore, choosing a low to medium default value for the hysteresis (for example, effective hysteresis = 4) normally fits most applications. The setting can be optimized by experimenting with the motor: a too low

setting results in reduced microstep accuracy, while a too high setting leads to more chopper noise and motor power dissipation. When the fast decay time is slightly longer than the blanking time, the setting is optimum. Reduce the off-time setting if this is hard to reach.

The hysteresis principle can, in some cases, lead to the chopper frequency becoming too low, for example, when the coil resistance is high when compared to the supply voltage. This is avoided by splitting the hysteresis setting into a start setting (HSTRT + HEND) and an end setting (HEND). An automatic hysteresis decrementer (HDEC) interpolates between both settings, by decrementing the hysteresis value stepwise each 16 system clocks. At the beginning of each chopper cycle, the hysteresis begins with a value, which is the sum of the start and end values (HSTRT + HEND), and decrements during the cycle, until either the chopper cycle ends or the hysteresis end value (HEND) is reached. This way, the chopper frequency is stabilized at high amplitudes and low supply voltage situations, if the frequency gets too low. This avoids the frequency from reaching the audible range.

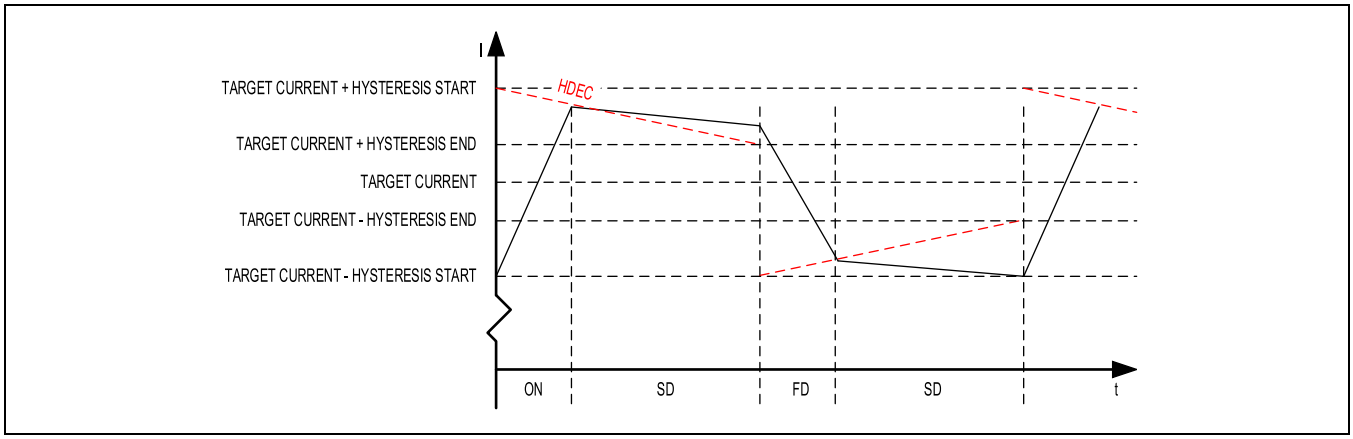


Figure 17. SpreadCycle Chopper Scheme Showing Coil Current during a Chopper Cycle

Table 14. SpreadCycle Mode Parameters

PARAMETER	DESCRIPTION	SETTING	COMMENT
HSTRT	Hysteresis start setting. This value is an offset from the hysteresis end value HEND. Default = 5	0…7	HSTRT = 1…8 This value adds to HEND.
HEND	Hysteresis end setting. Sets the hysteresis end value after a number of decrements. The sum HSTRT + HEND must be ≤16. At a current setting of max. 30 (amplitude reduced to 240), the sum is not limited. Default = 2	0…2	-3…-1: negative HEND
		3	0: zero HEND
		4…15	1…12: positive HEND

Even at HSTRT = 0 and HEND = 0, the TMC2241 sets a minimum hysteresis using analog circuitry.

Example:

A hysteresis of 4 is chosen. Decide to not use hysteresis decrement. In this case, set:

HEND = 6 (sets an effective end value of 6 - 3 = 3)

HSTRT = 0 (sets minimum hysteresis, example, 1: 3 + 1 = 4)

To take advantage of the variable hysteresis, set most of the value to the HSTRT, example, 4, and the remaining 1 to hysteresis end. The resulting configuration register values are as follows:

HEND = 0 (sets an effective end value of -3)

HSTRT = 6 (sets an effective start value of hysteresis end +7: 7 - 3 = 4)

Classic Constant Off-Time Chopper

The classic constant off-time chopper is an alternative to SpreadCycle. The constant off-time chopper uses a fixed-time fast decay following each on-phase. While the duration of the on-phase is determined by the chopper comparator, the fast decay time must be long enough for the driver to follow the falling slope of the sine wave, but it should not be so long that it causes excess motor current ripple and power dissipation. This can be tuned using an oscilloscope or evaluating motor smoothness at different velocities. A good starting value is a fast decay time setting similar to the slow decay time setting.

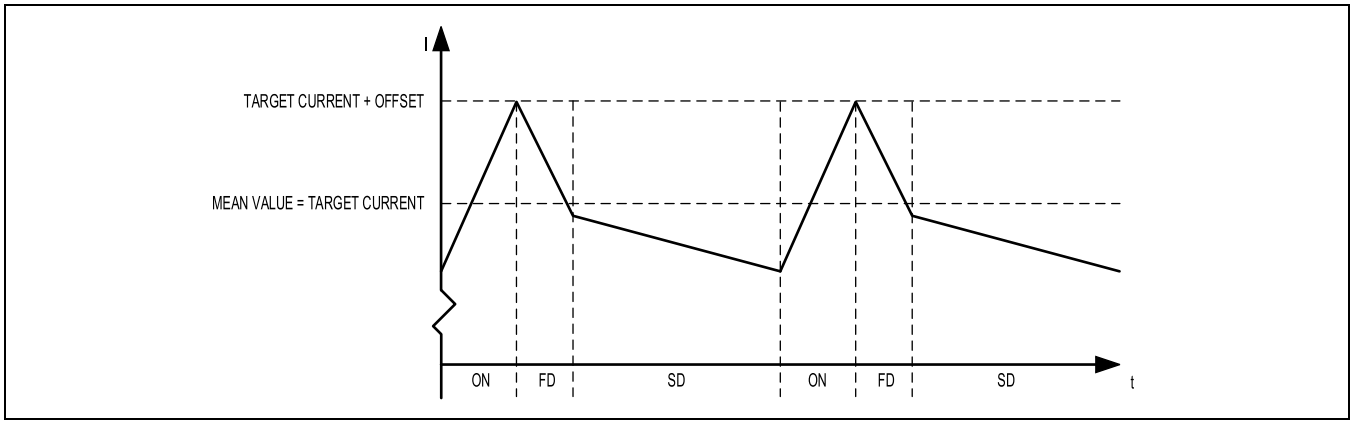


Figure 18. Classic Constant Off-Time Chopper with Offset Showing Coil Current

After tuning the fast decay time, the offset should be tuned for a smooth zero crossing. This is necessary because the fast decay phase makes the absolute value of the motor current lower than the target current (see the following figures). If the zero offset is too low, the motor stands still for a short moment during current zero crossing. If it is set too high, it makes a larger microstep. Typically, a positive offset setting is required for smoothest operation.

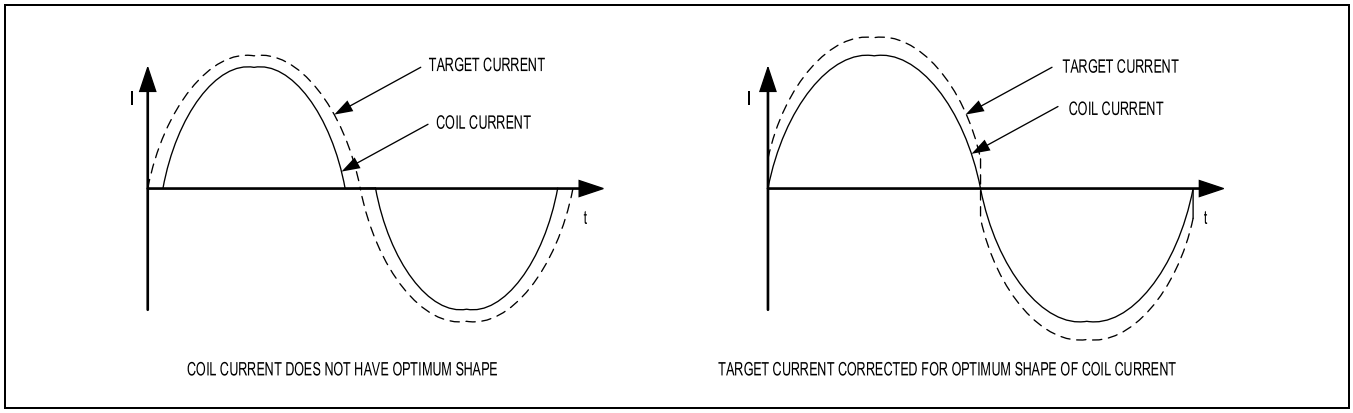


Figure 19. Zero Crossing with Classic Chopper and Correction Using Sine Wave Offset

Table 15. Parameters Controlling the Constant Off-Time Chopper Mode

PARAMETER	DESCRIPTION	SETTING	COMMENT
TFD (fd3 and HSTRT)	Fast decay time setting. With CHM = 1, these bits control the portion of fast decay for each chopper cycle. Default = 5	0	Slow decay only
		1…15	Duration of fast decay phase
OFFSET (HEND)	Sine wave offset. With CHM = 1, these bits control the sine wave offset. A positive offset corrects for zero crossing error. Default = 2	0…2	Negative offset: -3…-1
		3	No offset: 0
		4…15	Positive offset 1…12
disfdcc	Selects usage of the current comparator for termination of the fast decay cycle. If the current comparator is enabled, it terminates the fast decay cycle in case the current reaches a	0	Enable comparator termination of fast decay cycle
		1	End by time only

	higher negative value than the actual positive value. Default = 0		

Integrated Current Sense

Non-dissipative current sensing is integrated in the TMC2241 (ICS). This feature eliminates the bulky external power resistors, which are normally required with external current sensing. The ICS results in a dramatic space and power saving compared with mainstream applications based on the external sense resistor. For optimum performance, the ICS individually measures $R_{DS(ON)}$ for each of the power MOSFETs, considering individual MOSFET temperature to yield the best results.

Setting the Motor Current

The TMC2241 allows to set the motor phase current. The parameters given in the following table allow to adapt the current scaling as well as the current ramp up and down.

Table 16. Parameters Controlling the Motor Current

PARAMETER	DESCRIPTION	SETTING	COMMENT
IRUN	Current scale when motor is running. Scales coil current values as taken from the internal sine wave table. For high precision motor operation, work with a current scaling factor in the range of 16 to 31, because scaling down the current values reduces the effective microstep resolution by making microsteps coarser. This setting also controls the maximum current value set by CoolStep. Default = 31	0…31	Scaling factor 1/32, 2/32, … 32/32
IHOLD	Identical to IRUN, but for motor in standstill. Lower values <16 are OK with IHOLD in comparison to IRUN. Default = 8		
GLOBALSCALER	First adapt the motor current range by selection of reference resistor R_{REF} and CURRENT_RANGE in DRV_CONF. Precisely fit the motor current to the desired value using GLOBALSCALER. This allows keeping IRUN at 31 for the full-scale setting to optimize the scaler range available for CoolStep or scaling to different situations using IRUN. GLOBALSCALER should not be changed during operation, as any change invalidates StealthChop tuning results.	0…255	Fine current scaler 0 = no scaling down, full current; 1…255: 1/256 … 255/256 current
CURRENT_RANGE	Selection of motor current range. This setting does the first adaption of the driver current to the selected motor. Typically, use the lowest setting fitting the motor.	0…2	Motor current range
IHOLDDELAY	Allows smooth current reduction from the run current to hold current. IHOLDDELAY controls the number of clock cycles for the motor power down after TZEROWAIT in increments of 2^{18} clocks: 0 = instant power down, 1…15: current reduction delay per current step in multiples of 2^{18} clocks. **Example:** When using IRUN = 31 and IHOLD = 16, 15 current steps are required to reduce hold current. An IHOLDDELAY setting of 4, thus, results in a power down time of 4 × 15 × 2^{18} clock cycles, for example, roughly one second at 16MHz. Default = 1	0 1…15	Instant power down to IHOLD 1 × 2^{18} … 15 × 2^{18} clocks per current decrement
IRUNDELAY		0	Instant power up to IRUN

	Controls the number of clock cycles for motor power-up after start is detected. Allows smooth current increment upon start of a motion from hold current (IHOLD) to run current (IRUN). While a quick power-up is important to establish full motor torque, a small delay time helps to reduce the acoustic noise and avoids a jump on the power supply current. Default = 4	1...15	Delay per current increment step in multiples of IRUNDELAY × 512 clocks

Setting the Full-Scale Current Range

The full-scale current I_{FS} is a peak current setting.

The full-scale current is selected with an external reference resistor and two bits in the DRV_CONF register.

A standard low-power resistor with 1% accuracy is sufficient.

Three different full-scale current ranges can be configured to adapt to different motor sizes and applications.

This is needed to benefit from a best possible current control resolution.

Therefore, connect a resistor from I_{REF} to GND to set the full-scale chopping current I_{FS}.

Bits 1…0 in the DRV_CONF register define the typical ON resistance of the driver stage and further control the full-scale range based on the external resistor.

The following equation shows the full-scale current I_{FS} as a function of the R_{REF} resistor connected to pin I_{REF} and the DRV_CONF register bit setting.

The proportionality constant K_{IFS} depends on the selected full-scale range setting (DRV_CONF register bits 1...0). The external resistor R_{REF} can range between 12kΩ and 60kΩ.

$$I_{FS}\,(RMS) = \frac{K_{IFS}(CURRENT_{RANGE})}{RREF[k\Omega]} \times \frac{GLOBALSCALER}{256} \times \frac{CS+1}{32} \times \frac{248}{256} / \sqrt{2}$$

This equation gives the RMS motor current per coil.

- CS is IRUN or IHOLD, respectively. IRUN is scaled down by CoolStep.
- 248/256 is the amplitude of the default microstep table (up to 255 may be used with StealthChop only).
- GLOBALSCALER is in the range of 1 to 256 (256 corresponds to a setting of GLOBALSCALER = 0).
- 1/SQRT(2) is the factor to calculate the RMS value for a sine wave shape.

Table 17. I_{FS} Full-Scale Peak Range Settings (Example for R_{REF} = 12kΩ)

REGISTER CONFIG. DRV_CONF BITS 1...0	K_{IFS} (A x kΩ)	MAX. FS SETTING (PEAK)	TYPICAL $R_{DS(ON)}$ (HS + LS)	NOTES
11	36	3A	0.31Ω	Optimized efficiency and extended operating range up to 3A (FS).
10	36	3A	0.31Ω	Optimized efficiency and extended operating range up to 3A (FS).
01	24	2A	0.37Ω	Reduced operating range up to 2AFS. When high accuracy at lower current is required.
00 (default)	11.75	1A	0.53Ω	Reduced operating range up to 1AFS. When high accuracy at low current is required.

The following table is a matrix of different reference resistor values (at pin I_{REF}) versus the different pin configurations for the full-scale current. The resulting maximum RMS current is given in each cell.

Table 18. I_{FS} Full-Scale RMS Current in Ampere (A_{RMS}) Based on DRV_CONF Bits 1…0 Setting and Different R_{REF}

R_{REF} (kΩ)	MAX. FULL SCALE CURRENT (A_{RMS}) BASED ON CURRENT_SCALER (DRV_CONF BITS 1…0) SETTING AND K_{IFS} (A × kΩ)			
	DRV_CONF BITS 1…0 = 11	DRV_CONF BITS 1...0 = 10	DRV_CONF BITS 1…0 = 01	DRV_CONF BITS 1…0 = 00
	K_{IFS} = 36	K_{IFS} = 36	K_{IFS} = 24	K_{IFS} = 11.75
12	2,05	2,05	1,37	0,67
15	1,65	1,65	1,09	0,53
18	1,37	1,37	0,91	0,45
22	1,12	1,12	0,75	0,37
27	0,91	0,91	0,61	0,30
33	0,75	0,75	0,49	0,24
39	0,63	0,63	0,43	0,20
47	0,52	0,52	0,35	0,17
56	0,44	0,44	0,29	0,15

Hint: Current values are calculated for the default microstep table with a factor of 248/256. Slightly higher current values are possible with a custom-built table!

Velocity-Based Mode Control

The TMC2241 allows the configuration of different chopper modes and modes of operation for optimum motor control. Depending on the motor load, the different modes can be optimized for lowest noise and high precision, highest dynamics, or maximum torque at highest velocity. Some of the features like CoolStep or StallGuard2 are useful in a limited velocity range. A number of velocity thresholds allow combining the different modes of operation within an application requiring a wide velocity range.

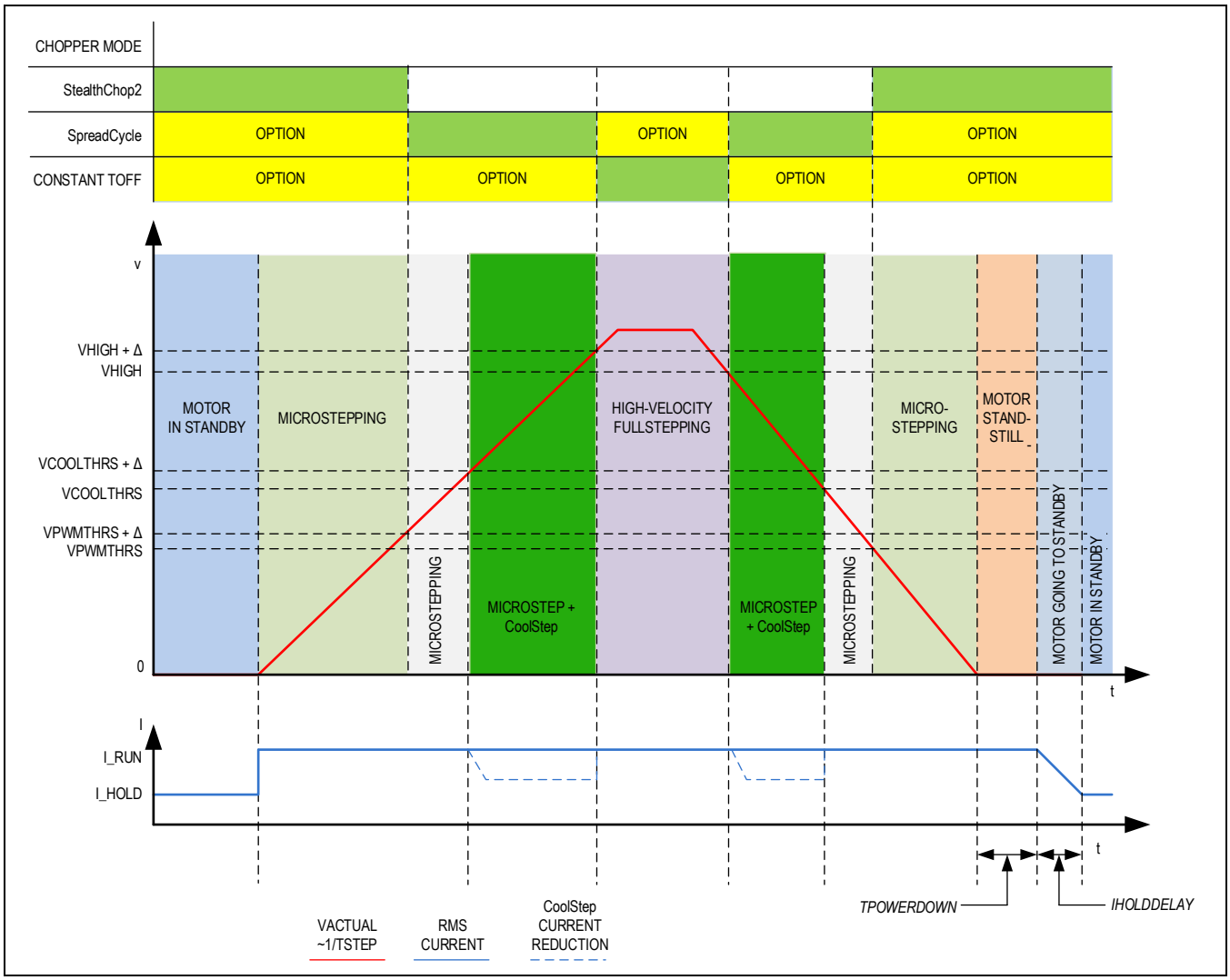


Figure 20. Choice of Velocity-Dependent Modes

Figure 20 shows all available thresholds and the required ordering. VPWMTHRS, VHIGH and VCOOLTHRS are determined by the settings TPWMTHRS, THIGH and TCOOLTHRS. The velocity is described by the time interval TSTEP between each two step pulses. This allows determination of the velocity when an external step source is used. TSTEP always is normalized to 256 microstepping. This way, the thresholds do not have to be adapted when the microstep resolution is changed. The thresholds represent the same motor velocity, independent of the microstep settings. TSTEP is compared to these threshold values. A hysteresis of 1/16 TSTEP, respectively, 1/32 TSTEP is applied to avoid continuous toggling of the comparison results when a jitter in the TSTEP measurement occurs. The upper switching velocity is higher by 1/16, respectively, 1/32 of the value set as threshold (can be selected with configuration bit small_hysteresis in the GCONF register). The motor current can be programmed to a run and a hold level, dependent on the standstill flag stst.

Using automatic velocity thresholds allows tuning the application for different velocity ranges. Features like CoolStep integrate completely and transparently in the setup. This way, once parameterized, these do not require any activation or deactivation using software.

Table 19. Velocity-Based Mode Control Parameters

PARAMETER	DESCRIPTION	SETTING	COMMENT
stst	Indicates motor standstill in each operation mode. Time is 2^{20} clocks after the last step pulse. Default/reset: 0	0/1	Status bit, read-only
TPOWER DOWN	This is the delay time after standstill (stst) of the motor to motor current power down. Time range is about 0 seconds to 4 seconds (with f_{CLK} = 16MHz). Setting 0 is no delay, 1 is one clock cycle delay. Further increment is in discrete steps of 218 clock cycles. Default: 0xA	0…255	Time in multiples of 2^{18} × tCLK
TSTEP	Actual measured time between two 1/256 microsteps derived from the step input frequency in units of 1/fCLK. Measured value is (2^{20}) - 1 in case of overflow or standstill. Default / reset: 0	0… 1048575	Status register, read-only. Actual measured step time in multiples of tCLK.
TPWMTHRS	TSTEP ≥ TPWMTHRS • StealthChop2 PWM mode is enabled, if configured. Default: 0	0… 1048575	Setting to control the upper velocity threshold for operation in StealthChop2.
TCOOLTHRS	TCOOLTHRS ≥ TSTEP ≥ THIGH: • StallGuard2 and CoolStep are enabled, if configured. • StealthChop2 voltage PWM mode is disabled. TCOOLTHRS ≥ TSTEP • StallGuard2 stall output signal is enabled (if configured) for use with external controller. Default: 0	0… 1048575	Setting to control the lower velocity threshold for operation with CoolStep and StallGuard2.
THIGH	TSTEP ≤ THIGH: • CoolStep is disabled (motor runs with normal current scale). • StealthChop2 voltage PWM mode is disabled. • If vhighchm is set, the chopper switches to chm = 1 with TFD = 0 (constant off time with slow decay, only). • Chopper sync is switched off (SYNC = 0). • If vhighfs is set, the motor operates in fullstep mode and the stall detection is switched over to fullstep stall detection. Default: 0	0… 1048575	Setting to control the upper threshold for operation with CoolStep and StallGuard2 as well as optional high velocity step mode.
small_ hysteresis	Hysteresis for step frequency comparison based on TSTEP (lower velocity threshold) and (TSTEP × 15/16) – 1, respectively, (TSTEP × 31/32) - 1 (upper velocity threshold). Default: 0	0	Hysteresis is 1/16.
		1	Hysteresis is 1/32.
vhighfs	This bit enables switching to fullstep, when VHIGH is exceeded. Switching takes place only at 45° position. The fullstep target current uses the current value from the microstep table at the 45° position. Default: 0	0	No switch to fullstep.
		1	Fullstep at high velocities.
vhighchm		0	No change of chopper mode.

	This bit enables switching to chm = 1 and fd = 0, when VHIGH is exceeded. This way, a higher velocity can be achieved. Can be combined with vhighfs = 1. If set, the TOFF setting automatically is doubled during high velocity operation to avoid doubling of the chopper frequency. Default: 0	1	Classic const. TOFF chopper at high velocities
en_pwm_ mode	StealthChop2 voltage PWM enable flag (depending on velocity thresholds). Switch from off to on state while in standstill only. Default: 0	0	No StealthChop2
		1	StealthChop2 active if configured and TSTEP > TPWMTHRS.

StallGuard2 Load Measurement

To fit different motor control schemes, the TMC2241 offers two types of StallGuard sensorless load detection schemes, covering the two basic chopper modes. StallGuard2 works in SpreadCycle operation, while StallGuard4 is optimized for StealthChop2 operation.

StallGuard2 provides an accurate measurement of the load on the motor. It can be used for stall detection as well as other uses at loads below those which stall the motor, such as CoolStep load-adaptive current reduction. The StallGuard2 measurement value changes linearly over a wide range of load, velocity, and current settings. As the load on the motor increases, the StallGuard value (SG_RESULT) decreases. Tuning is required to properly detect stalls. Set the StallGuard threshold (SGTHRS) such that SG_RESULT reaches 0 (or near to 0) when the motor is overloaded/stalls.

Hint: To use StallGuard2 and CoolStep, the StallGuard2 sensitivity should first be tuned using the SGT setting!

Attention: Unlike with TMC5240 and TMC2240, SG4_THRS covers the full 9-bit range of SG4_RESULT by doubling the value of SG4_THRS for comparison.

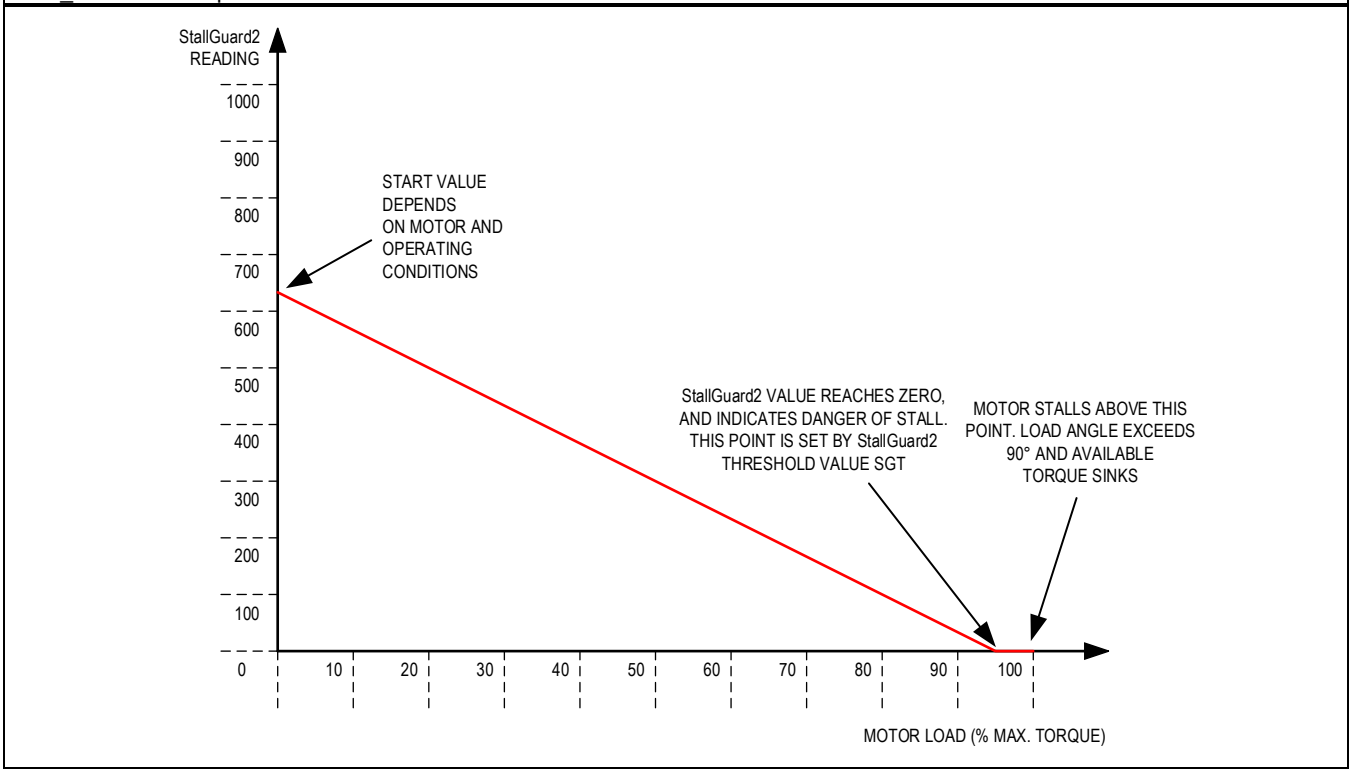


Figure 21. Function Principle of StallGuard2

Table 20. StallGuard2-Related Parameters

PARAMETER	DESCRIPTION	SETTING	COMMENT
SGT	This signed value controls the StallGuard2 threshold level for stall detection and sets the optimum measurement range for readout. A lower value gives a higher sensitivity. Zero is the starting value working with most motors. A higher value makes StallGuard2 less sensitive and requires more torque to indicate a stall.	0	Indifferent value
		+1…+63	Less sensitivity
		-1…-64	Higher sensitivity
sfilt	Enables the StallGuard2 filter for more precision of the measurement. If set, reduces the measurement frequency to one measurement per electrical period of the motor (4 fullsteps).	0	Standard mode
		1	Filtered mode
STATUS WORD	**DESCRIPTION**	**RANGE**	**COMMENT**
SG_RESULT	This is the StallGuard2 result. A higher reading indicates less mechanical load. A lower reading indicates a higher load, and thus, a higher load angle. Tune the SGT setting to show a SG_RESULT reading of roughly 0 to 100 at maximum load before motor stall.	0…1023	0: Highest load Low value: high load High value: less load

Tuning StallGuard2 Threshold SGT

The StallGuard2 value SG_RESULT is affected by motor-specific characteristics and application-specific demands on load, velocity, supply voltage, and current level. Therefore the easiest way to tune the StallGuard2 threshold SGT for a specific motor type and operating conditions is interactive tuning in the actual application.

Initial procedure for tuning StallGuard SGT:

- Operate the motor at the normal operation velocity, supply voltage, and current setting for the application and monitor SG_RESULT.
- Apply slowly increasing mechanical load to the motor. If the motor stalls before SG_RESULT reaches zero, decrease SGT. If SG_RESULT reaches zero before the motor stalls, increase SGT. A good SGT starting value is zero. SGT is signed. So, it can have negative or positive values.
- Now enable sg_stop and make sure the motor is safely stopped whenever it is stalled. Increase SGT if the motor is stopped before a stall occurs. Restart the motor by disabling sg_stop or by clearing event_stop_sg in the RAMP_STAT register (write to clear).
- The optimum setting is reached when SG_RESULT is between 0 and roughly 100 at increasing load shortly before the motor stalls, and SG_RESULT increases by 100 or more without load. SGT in most cases can be tuned for a certain motion velocity or a velocity range. Make sure the setting works reliably in a certain range (example, 80% to 120% of desired velocity) and also under extreme motor conditions (lowest and highest applicable temperature).

Optional procedure allowing automatic tuning of SGT:

The basic idea behind the SGT setting is a factor, which compensates the StallGuard measurement for resistive losses inside the motor. At standstill and very low velocities, resistive losses are the main factor for the balance of energy in the motor, because mechanical power is zero or near to zero. This way, SGT can be set to an optimum at near zero velocity. This algorithm is especially useful for tuning SGT within the application to give the best result independent of environment conditions, motor stray, etc.

- Operate the motor at low velocity < 10 RPM (that is, a few to a few fullsteps per second) and target operation current and supply voltage. In this velocity range, there is not much dependence of SG_RESULT on the motor load, because the motor does not generate significant back-EMF. Therefore, mechanical load does not make a big difference on the result.
- Switch on sfilt. Now increase SGT starting from 0 to a value, where SG_RESULT starts rising. With a high SGT, SG_RESULT rises to the maximum value. Reduce again to the highest value, where SG_RESULT stays at 0. Now the SGT value is set as sensibly as possible. When the SG_RESULT is increasing at higher velocities, there is useful stall detection.

- SG_RESULT goes to zero when the motor stalls. Set TCOOLTHRS to match the lower velocity threshold, where StallGuard delivers a good result to use sg_stop.

The upper velocity for the stall detection with this setting is determined by the velocity where the motor back-EMF approaches the supply voltage and the motor current starts dropping when further increasing velocity.

The system clock frequency affects SG_RESULT. An external crystal-stabilized clock should be used for applications that demand the highest performance. The power supply voltage also affects SG_RESULT. So, tighter regulation results in more accurate values. SG_RESULT measurement has a high resolution, and there are a few ways to enhance its accuracy, as described in the following sections.

Variable Velocity Limits TCOOLTHRS and THIGH

The SGT setting chosen as a result of the previously described SGT tuning can be used for a certain velocity range. Outside this range, a stall may not be detected safely, and CoolStep might not give the optimum result.

In many applications, operation at or near a single operation point is used most of the time and a single setting is sufficient. The driver provides a lower and an upper velocity threshold to match this. The stall detection is disabled outside the determined operation point, for example, during acceleration phases preceding a sensorless homing procedure when setting TCOOLTHRS to a matching value. An upper limit can be specified by THIGH.

The velocity limits VHIGH and VCOOLTHRS are determined by the settings THIGH and TCOOLTHRS.

In some applications, a velocity dependent tuning of the SGT value can be expedient, using a small number of support points and linear interpolation.

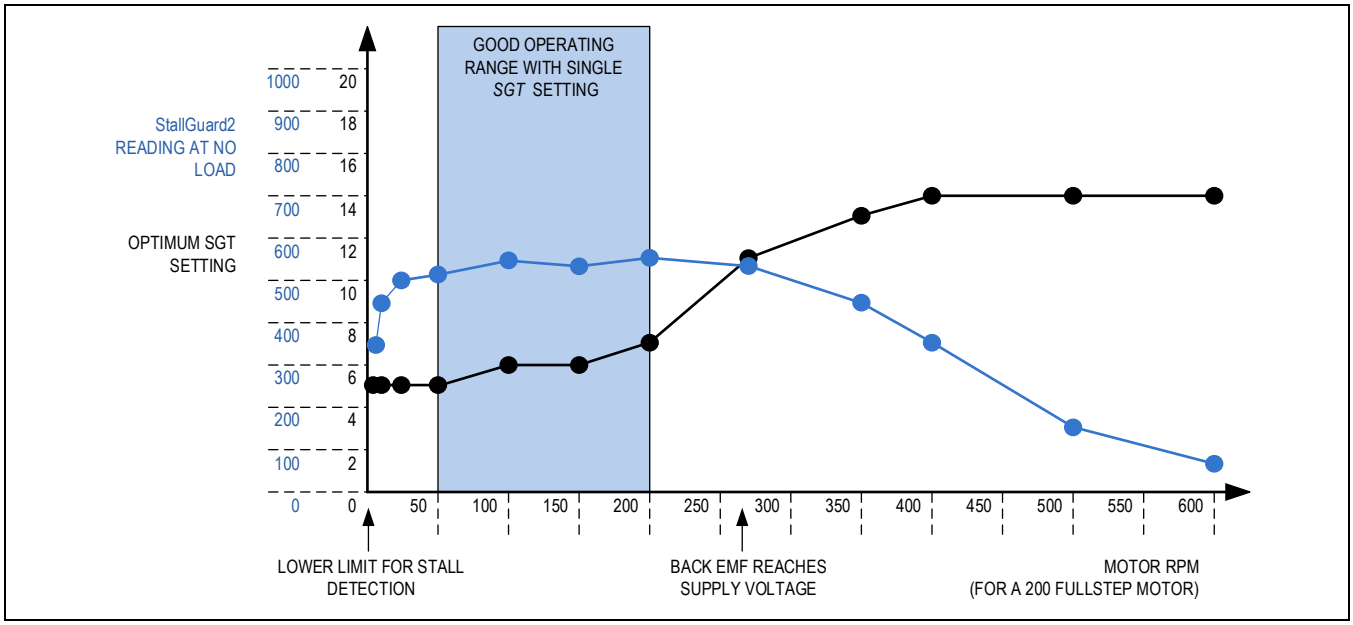


Figure 22. Example: Optimum SGT Setting and StallGuard2 Reading with an Example Motor

Small Motors with High Torque Ripple and Resonance

Motors with a high detent torque show an increased variation of the StallGuard2 measurement value SG_RESULT with varying motor currents, especially at low currents. For these motors, check the current dependency for the best result.

Temperature Dependence of Motor Coil Resistance

Motors working over a wide temperature range may require temperature correction, because motor coil resistance increases with rising temperature. This can be corrected as a linear reduction of SG_RESULT at increasing temperature, as motor efficiency is reduced.

Accuracy and Reproducibility of StallGuard2 Measurement

In a production environment, it may be desirable to use a fixed SGT value within an application for one motor type. Most of the unit-to-unit variation in StallGuard2 measurements results from manufacturing tolerances in motor construction. The measurement error of StallGuard2, provided that all other parameters remain stable, can be as low as:

stallGuard2 measurement error = +/- max.(1, |SGT|)

StallGuard2 Update Rate and Filter

The StallGuard2 measurement value SG_RESULT is updated with each fullstep of the motor. This is enough to safely detect a stall because a stall always means the loss of four fullsteps. In a practical application, especially when using CoolStep, a more precise measurement might be more important than an update for each fullstep because the mechanical load never changes instantaneously from one step to the next. For these applications, the sfilt bit enables a filtering function over four load measurements. The filter should always be enabled when high-precision measurement is required. It compensates for variations in motor construction, for example, due to misalignment of the phase A to phase B magnets. The filter should be disabled when a rapid response to increasing load is required and for best results of sensorless homing using StallGuard.

Detecting a Motor Stall

For best stall detection, work without StallGuard2 filtering (sfilt = 0). To safely detect a motor stall, the stall threshold must be determined using a specific SGT setting. Therefore, the maximum load must be determined, which the motor can drive without stalling. At the same time, monitor the SG_RESULT value at this load, for example, some value within the range 0 to 100. The stall threshold should be a value safely within the operating limits for parameter stray. The response at an SGT setting at or near 0 gives some idea on the quality of the signal: check the SG_RESULT value without load and with maximum load. These should show a difference of at least 100 or a few 100, which are largely compared to the offset. If the SGT value is set in a way that a reading of 0 occurs at maximum motor load, the stall can be automatically detected to issue a motor stop. In the moment of the step resulting in a step loss, the lowest reading is visible. After the step loss, the motor vibrates and shows a higher SG_RESULT reading.

Homing with StallGuard2

The homing of a linear drive requires moving the motor into the direction of a hard stop. As StallGuard2 needs a certain velocity to work (as set by TCOOLTHRS), make sure the start point is far enough away from the hard stop to provide the distance required for the acceleration phase. After setting up SGT, start a motion in the direction of the hard stop and activate the stop on stall function (set sg_stop in SW_MODE). The stop condition also is indicated by the flag StallGuard in DRV_STATUS. After setting up new motion parameters to prevent the motor from restarting right away, StallGuard2 can be disabled, or the motor can be re-enabled by reading RAMP_STAT. The read and clear function of the event_stop_sg flag in RAMP_STAT restart the motor after the expiration of TZEROWAIT in case the motion parameters are not modified.

Limits of StallGuard2 Operation

StallGuard2 does not operate reliably at extreme motor velocities: Very low motor velocities (for many motors, less than 1Rps) generate a low back-EMF and make the measurement unstable and dependent on environment conditions (temperature, etc.). The automatic tuning procedure described earlier compensates for this. Other conditions also lead to extreme settings of SGT and poor response of the measurement value SG_RESULT to the motor load.

Very high motor velocities, in which the full sinusoidal current is not driven into the motor coils, also leads to poor response. These velocities are typically characterized by the motor back-EMF reaching the supply voltage.

StallGuard4 Load Measurement

StallGuard4 is optimized for operation with StealthChop2, while its predecessor StallGuard2 works with SpreadCycle.

Anyway, the function is similar: both deliver a load value, going from a high value at low load, and to a low value at high load.

While StallGuard2 is tuned to show a “0” reading for stall detection, StallGuard4 uses a comparison value to trigger stall detection, rather than shifting the measurement result by applying an offset.

StallGuard4 provides an accurate measurement of the load on the motor and can be used for stall detection, load estimation, as well as CoolStep load-adaptive current reduction. The StallGuard4 measurement value changes linearly over a wide range of load, velocity, and current settings, as shown in the following figure. When approaching maximum motor load, the value goes down to a motor-specific lower value. This corresponds to a load angle of 90° between the magnetic field of the coils and magnets in the rotor. This also is the most energy-efficient point of operation for the motor.

To use StallGuard4, check the sensitivity of the motor at border conditions.

Attention: Unlike with TMC2240 and TMC5240, SG4_THRS covers the full 9-bit range of SG4_RESULT by doubling the value of SG4_THRS for comparison.

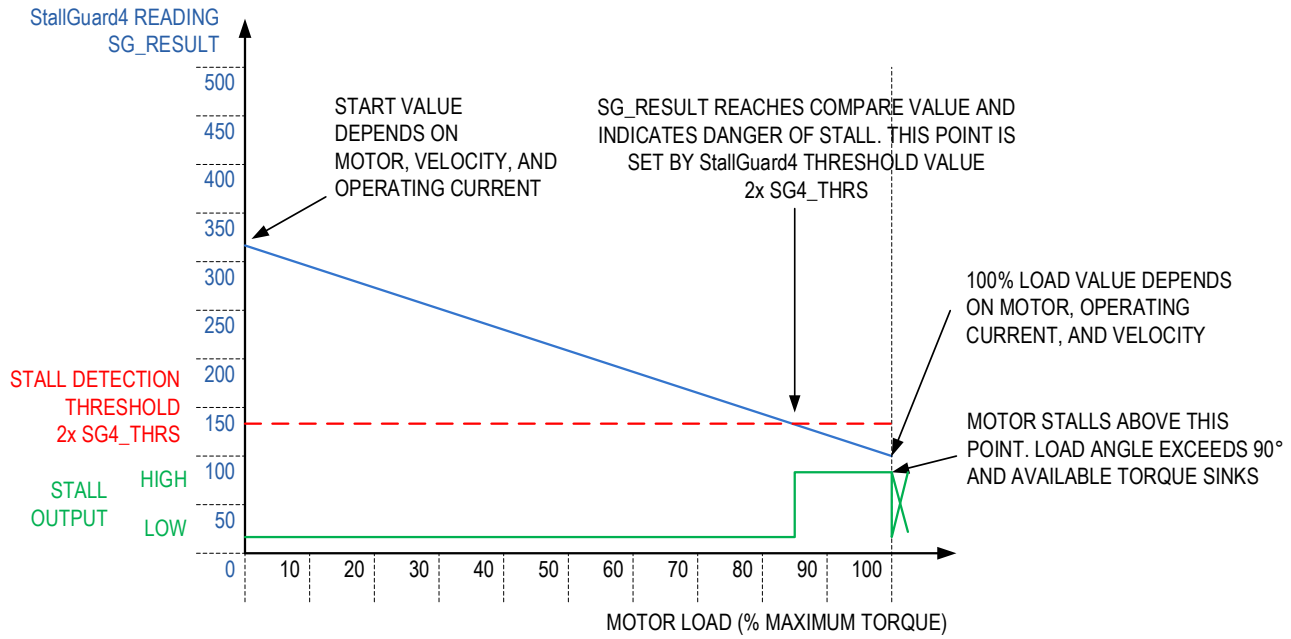


Figure 23. StallGuard4 Mode of Operation

Table 21. StallGuard4-Related Parameters

PARAMETER	DESCRIPTION	SETTING	COMMENT
SG4_THRS	This value controls the StallGuard4 threshold level for stall detection. It compensates for motor-specific characteristics and controls sensitivity. A higher value gives a higher sensitivity. A higher value makes StallGuard4 more sensitive and requires less torque to indicate a stall. The resulting threshold is the double of this value!	0… 255	The double of this value is compared to SG4_RESULT. The stall output is active if SG4_RESULT falls below 2 × SG4_THRS.
STATUS WORD	**DESCRIPTION**	**RANGE**	**COMMENT**
SG4_RESULT	This is the StallGuard4 result. A higher reading indicates less mechanical load. A lower reading indicates a higher load, and thus, a higher load angle. This value is generated independent of the enabling conditions like the actual chopper mode and velocity thresholds like VCOOLTHRS. The result is calculated from SG4_IND_x measurements, adding one bit for higher precision and similar range as StallGuard2.	0…510	Low value: highest load High value: low/no load
SG4_IND_3 SG4_IND_2 SG4_IND_1 SG4_IND_0	Individual measurements for motor phase A falling (SG4_IND_0)/rising (SG4_IND_1) transition, respectively, phase B falling (SG4_IND_2)/rising (SG4_IND_3) transition. Individual measurements are available in filtered mode only (sg4_filt_en = 1). SG4_IND_0 covers all cases in unfiltered mode (sg4_filt_en = 0).	0....255	Low value: highest load High value: low/no load

sg4_filt_en	0: Unfiltered operation, SG4_RESULT updates with each fullstep 1: Filtered operation, SG4_IND_0...3 available, SG4_RESULT gives the average of last four SG4_IND_x measurements.	0 1	0: Filter off 1: Filtered operation, SG4_IND values available
sg_angle_offset	This flag enables optimized switching between StealthChop2 and SpreadCycle by using the SG4_RESULT to determine the phase lag in StealthChop2 and compensate for the phase jump when switching from voltage-controlled to current-controlled operation in SpreadCycle. The phase offset is stored and is subtracted again when switching back to StealthChop2.	0 1	0: No angle correction 1: Optimized switching between StealthChop2 and SpreadCycle.

Tuning StallGuard4

The StallGuard4 value SG4_RESULT is affected by motor-specific characteristics and application-specific demands on load, coil current, and velocity. Therefore, the easiest way to tune the StallGuard4 threshold SG4_THRS for a specific motor type and operating conditions is interactive tuning in the actual application.

The initial procedure for tuning StallGuard SG4_THRS is as follows:

- Operate the motor at the normal operation velocity for the application and monitor SG4_RESULT.
- Apply slowly increasing mechanical load to the motor. Check the lowest value of SG4_RESULT before the motor stalls. Use this value as starting value for SG4_THRS (apply half of the value).
- Now, monitor the StallGuard output signal through the DIAG output (also set TCOOLTHRS to match the lower velocity limit for operation) and stop the motor when a pulse is seen on the respective output. Make sure the motor is safely stopped whenever it is stalled. Increase SG4_THRS if the motor is stopped before a stall occurs.
- The optimum setting is reached when a stall is safely detected and leads to a pulse at DIAG in the moment where the stall occurs. SG4_THRS in most cases can be tuned for a certain motion velocity or a velocity range. Make sure the setting works reliablly in a certain range (for example, 80% to 120% of the desired velocity) and under extreme motor conditions (lowest and highest applicable temperature).

DIAG is pulsed by StallGuard, when SG4_RESULT falls below 2 × SG4_THRS. It is only enabled in StealthChop2 mode, and when TCOOLTHRS ≥ TSTEP > TPWMTHRS.

The external motion controller should react to a single pulse by stopping the motor, if desired. Set TCOOLTHRS to match the lower velocity threshold where StallGuard delivers a good result.

SG4_RESULT measurement has a high resolution, and there are a few ways to enhance its accuracy, as described in the following sections.

StallGuard4 Update Rate

The StallGuard4 measurement value SG4_RESULT is updated with each fullstep of the motor. This is enough to safely detect a stall because a stall always means the loss of four fullsteps.

StallGuard4 provides two options for measurement:

- sg4_filt_en = 0: A single measurement, updated after each fullstep, and valid for each one fullstep. This measurement allows quickest reaction to load variations, as SG4_RESULT is fully updated with each zero transmission of a coil voltage. Therefore, it is optimum for stall detection with a hard obstacle.
- sg4_filt_en = 1: In this mode, four individual signals are generated: SG4_IND_0 upon falling 0-transition of the cosine wave (coil A), SG4_IND_1 upon rising 0-transition of the cosine wave, SG4_IND_2 upon falling 0-transition of the sine wave (coil B), and SG4_IND_3 upon rising 0-transition of the sine wave. The actual value for SG4_RESULT is the mean value of all four measurements, updated once each fullstep. With this, each fullstep has an influence of 25% only on the overall result. This mode is perfect for detecting soft obstacles, or for usage of CoolStep on imprecise motors. In filtered mode, sensitivity to a sudden load increase (hard motor blockage) is reduced.

Detecting a Motor Stall

To safely detect a motor stall, the stall threshold must be determined using a specific SG4_THRS setting and a specific motor velocity or velocity range. Further, the motor current setting has a certain influence and should not be modified once optimum values are determined. Therefore, the maximum load must be determined, which the motor can drive without stalling for the given application. At the same time, monitor SG4_RESULT at this load. The stall threshold should be a value safely within the operating limits for parameter stray. More refined evaluation may also react to a change of SG4_RESULT rather than comparing to a fixed threshold. This rules out certain effects that influence the absolute value.

Limits of StallGuard4 Operation

StallGuard4 does not operate reliably at extreme motor velocities: very low motor velocities (for many motors, less than 1Rps) generate a low back-EMF and make the measurement unstable and dependent on environment conditions (temperature, etc.). Other conditions also lead to a poor response of the measurement value SG4_RESULT to the motor load. Very high motor velocities, in which the full sinusoidal current is not driven into the motor coils, also lead to poor response. These velocities are typically characterized by the motor back-EMF exceeding the supply voltage.

CoolStep Load Adaptive Current Scaling

CoolStep is an automatic smart energy optimization for stepper motors based on the motor mechanical load, making them “green”. Depending on the actual chopper mode, CoolStep automatically uses StallGuard4 load measurement result in StealthChop2, or StallGuard2 in SpreadCycle. Coolstep requires that either StallGuard2 or StallGuard4 (depending on the chopper mode being used) must be tuned before use. A single tuning does not cover all operating points.

Setting Up for CoolStep

CoolStep is controlled by several parameters, but two are critical for understanding how it works.

Table 22. CoolStep Critical Parameters

PARAMETER	DESCRIPTION	RANGE	COMMENT
SEMIN	4-bit unsigned integer that sets a lower threshold. If SG_RESULT goes below this threshold (indicating a large load), CoolStep increases the current to both coils. The 4-bit SEMIN value is scaled by 32 to cover the lower half of the range of the 10-bit SG_RESULT value. (The name of this parameter is derived from smartEnergy, an earlier name for CoolStep.)	0	Disable CoolStep
		1…15	Threshold is SEMIN × 32
SEMAX	4-bit unsigned integer that controls an upper threshold. If SG_RESULT is sampled equal to or above this threshold enough times (indicating a light load), CoolStep decreases the current to both coils. The upper threshold is (SEMIN + SEMAX + 1) × 32.	0…15	Threshold is (SEMIN + SEMAX + 1) × 32

Figure 24 shows the operating regions of CoolStep.

- The black line represents the SG_RESULT measurement value.
- The blue line represents the mechanical load applied to the motor.
- The red line represents the current into the motor coils.

When the load increases, SG_RESULT falls below SEMIN × 32, and CoolStep increases the current. When the load decreases, SG_RESULT rises above (SEMIN + SEMAX + 1) × 32, and the current is reduced.

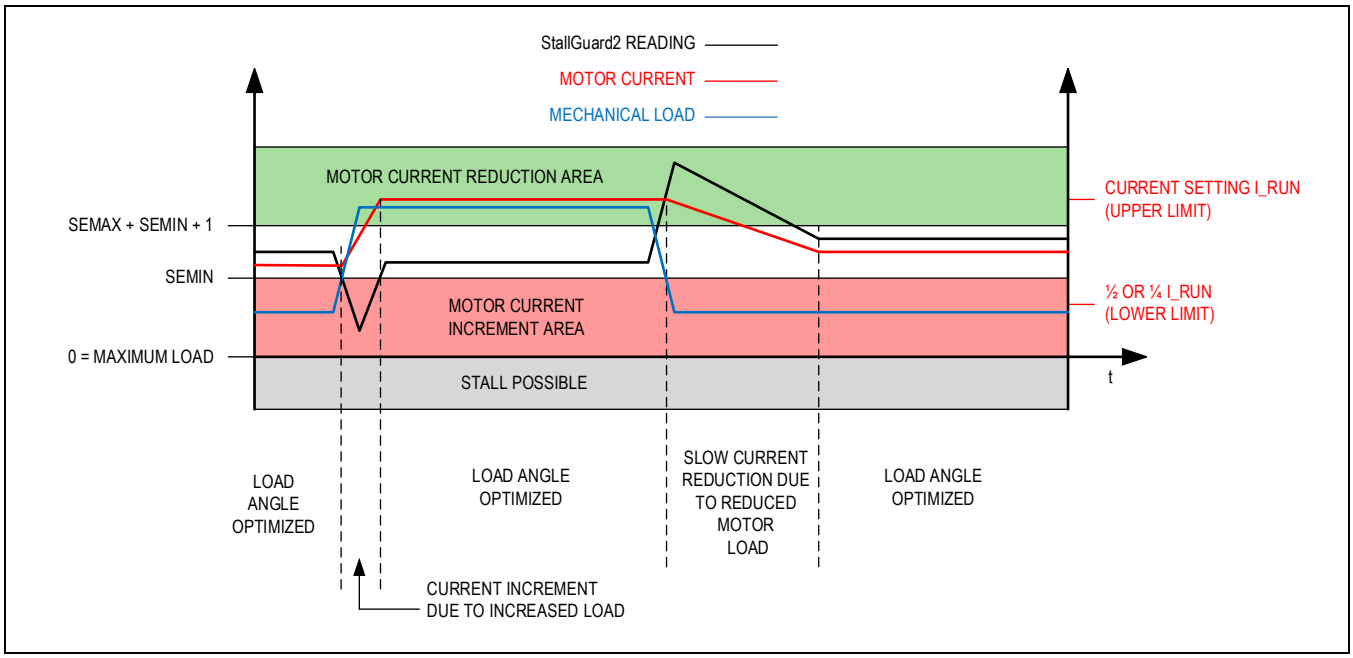


Figure 24. CoolStep Adapts Motor Current to the Load

Table 23. CoolStep Additional Parameters and Status Information

PARAMETER	DESCRIPTION	RANGE	COMMENT
SEUP	Sets the current increment step. The motor current is incremented by this setting whenever a new StallGuard2 or StallGuard4 value is measured that lies below the lower threshold as set by SEMIN.	0…3	Step width of CS value CS_ACTUAL is 1, 2, 4, 8.
SEDN	Sets the number of StallGuard2/StallGuard4 readings above the upper threshold necessary for each current decrement of the motor current.	0…3	Number of StallGuard2 measurements per decrement: 32, 8, 2, 1
SEIMIN	Sets the lower motor current limit for CoolStep operation by scaling the IRUN current setting. When using StealthChop2, make sure to operate well above the minimum motor current as determined for StealthChop2 current regulation, especially when a reduction down to 25% is desired.	0	0: 1/2 of IRUN (when used with StealthChop requires IRUN ≥ 16)
		1	1: 1/4 of IRUN (when used with StealthChop requires IRUN ≥ 28)
TCOOLTHRS	Lower velocity threshold for switching on CoolStep. Below this velocity, CoolStep is disabled. Adapt to the lower limit of the velocity range where StallGuard2 gives a stable result. **Hint:** May be adapted to disable CoolStep during the acceleration and deceleration phase by setting VCOOLTHRS identical to VMAX.	1… 2^{20} - 1	Specifies lower CoolStep velocity by comparing the threshold value to TSTEP.
THIGH	Upper velocity threshold value for CoolStep. Above this velocity, CoolStep is disabled. Adapt to the velocity range where StallGuard2/StallGuard4 gives a stable result.	1… 2^{20} - 1	Also controls additional functions like switching to fullstepping.
STATUS WORD	**DESCRIPTION**	**RANGE**	**COMMENT**
CS_ACTUAL	This status value provides the actual motor current scale as controlled by CoolStep. The value goes up to the IRUN value and down to the portion of IRUN, as specified by SEIMIN.	0…31	1/32, 2/32, … 32/32

Tuning CoolStep

Before tuning CoolStep in conjunction with SpreadCycle, first tune the StallGuard2 threshold level SGT, which affects the range of the load measurement value SG_RESULT. CoolStep uses SG_RESULT to operate the motor near the optimum load angle of +90°. In conjunction with StealthChop2, CoolStep uses SG4_RESULT. In this mode, the leveling is done through SEMIN.

The current increment speed is specified in SEUP, and the current decrement speed is specified in SEDN. They can be tuned separately because they are triggered by different events that may need different responses. The encodings for these parameters allow the coil currents to be increased much more quickly than decreased, because crossing the lower threshold is a more serious event that may require a faster response. If the response is too slow, the motor may stall. In contrast, a slow response to crossing the upper threshold does not risk anything more serious than missing an opportunity to save power.

CoolStep operates between limits controlled by the current scale parameter IRUN and the seimin bit.

Response Time

For fast response to increasing motor load, use a high current increment step SEUP. If the motor load changes slowly, a lower current increment step can be used to avoid motor oscillations. If the filter controlled by sfilt is enabled, the measurement rate and regulation speed are cut by a factor of four.

Advice: The most common and beneficial use is to adapt CoolStep for operation at the typical system target operation velocity and to set the velocity thresholds accordingly. As acceleration and decelerations normally can be quick, these require the full motor current, while they have only a small contribution to the overall power consumption due to their short duration.

Low Velocity and Standby Operation

Because CoolStep is not able to measure the motor load in standstill and at very low RPM, a lower velocity threshold is provided in the ramp generator. It should be set to an application-specific default value. Below this threshold, the normal current setting through IRUN, respectively, IHOLD is valid. An upper threshold is provided by the VHIGH setting. The velocity limits VHIGH and VCOOLTHRS are determined by the settings THIGH and TCOOLTHRS.

Both thresholds can be set as a result of the StallGuard2 and StallGuard4 tuning process.

Diagnostic Outputs

The DIAG outputs deliver a position compare signal to allow the exact triggering of external logic, and an interrupt signal to trigger the software to certain conditions. Either an open drain (active low) output signal can be chosen (default, GCONF register, bit diag0_int_pushpull = 0), or an active high push-pull output signal (GCONF register, bit diag0_int_pushpull = 1). When using the open drain output, multiple driver output signals can be ORed. An external pullup resistor in the range 4.7kΩ to 100kΩ is required. DIAG0 also is driven low upon a reset condition. However the end of the reset condition cannot be determined by monitoring DIAG0 in this configuration, because the event_pos_reached flag also is active upon reset, and thus, the pin stays actively low after the reset condition. To safely determine a reset condition, monitor the reset flag by SPI or read out any register to confirm the chip is powered up.

For more flexibility, an additional register DIAG_CONF is added to the TMC2241. Setting bits in this register enables free assignment of signals independently for each diagnostic output DIAG0/1.

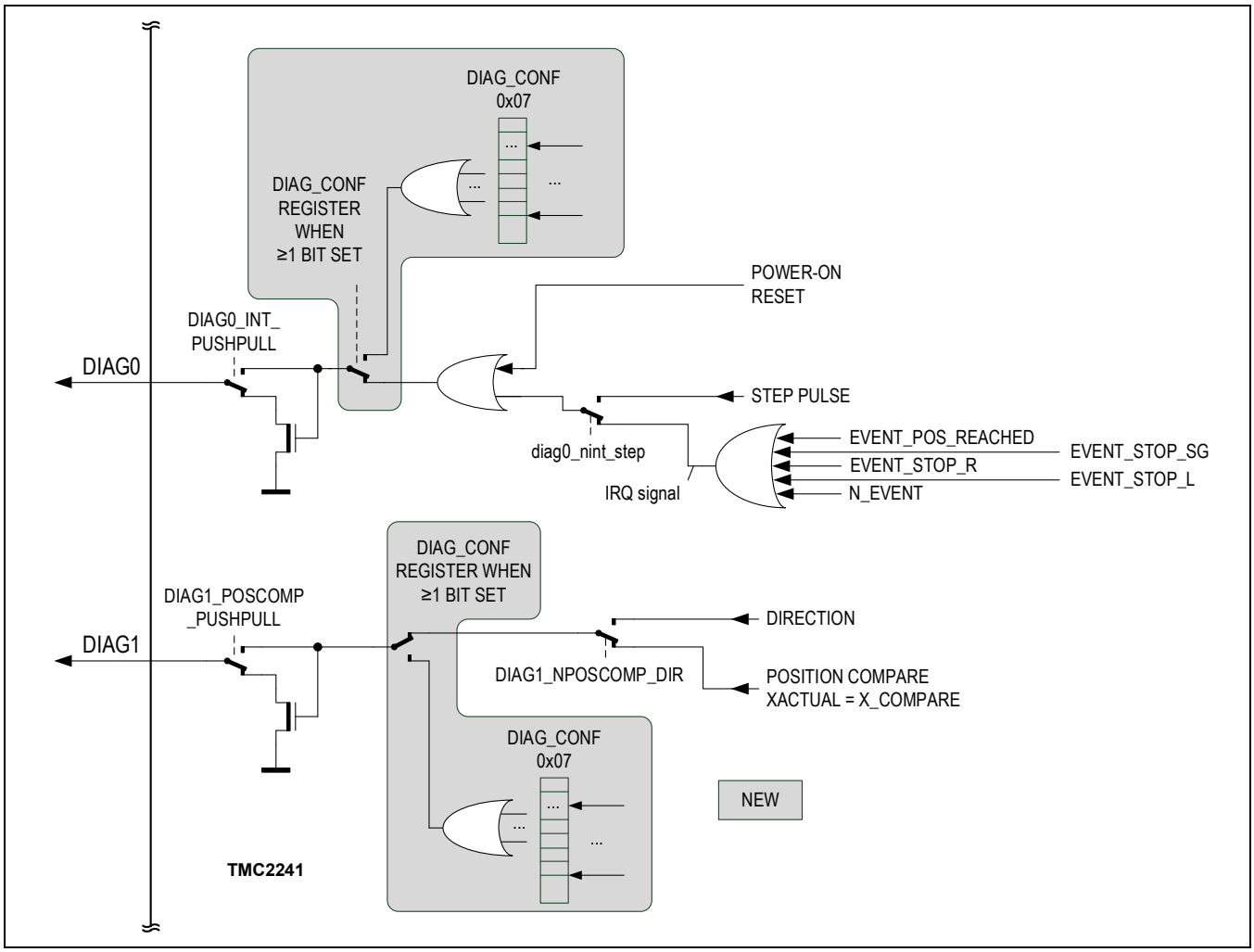


Figure 25. Diagnostic Outputs Configuration Options

Sine Wave Lookup Table

The TMC2241 provides a programmable lookup table to store the microstep current wave. As a default, the table is preprogrammed with a sine wave, which is a good starting point for most stepper motors. Reprogramming the table to a motor-specific wave allows drastically improved microstepping, especially with low-cost motors. The user benefits are:

- Microstepping – extremely improved with low cost motors.
- Motor – runs smooth and quiet.
- Torque – reduced mechanical resonances yield improved torque.
- Low frequency motor noise - reduced by adapting the sine and cosine wave shift for the actual motor's manufacturing tolerance.

Microstep Table

To minimize the required memory and the amount of data to be programmed, only a quarter of the wave is stored. The internal microstep table maps the microstep wave from 0° to 90°. It is symmetrically extended to 360°. When reading out the table, the 10-bit microstep counter MSCNT addresses the fully extended wave table. The table is stored in an incremental fashion, using each one bit per entry. Therefore, only 256 bits (ofs00 to ofs255) are required to store the quarter wave. These bits are mapped to eight 32-bit registers. Each ofs bit controls the addition of an inclination Wx or Wx + 1 when advancing one step in the table. When Wx is 0, a 1 bit in the table at the actual microstep position means “add one” when advancing to the next microstep. As the wave can have a higher inclination than 1, the base inclinations Wx can be programmed to -1, 0, 1, or 2 using up to four flexible programmable segments within the quarter wave. This way, even a negative inclination can be realized. The four inclination segments are controlled by the position registers X1

to X3. Inclination segment 0 goes from microstep position 0 to X1-1 and its base inclination is controlled by W0, segment 1 goes from X1 to X2-1 with its base inclination controlled by W1, etc.

When modifying the wave, take care to ensure a smooth and symmetrical zero transition when the quarter wave is expanded to a full wave. The maximum resulting swing of the wave should be adjusted to a range of -248 to 248 to give the best possible resolution while leaving headroom for the hysteresis-based chopper to add an offset.

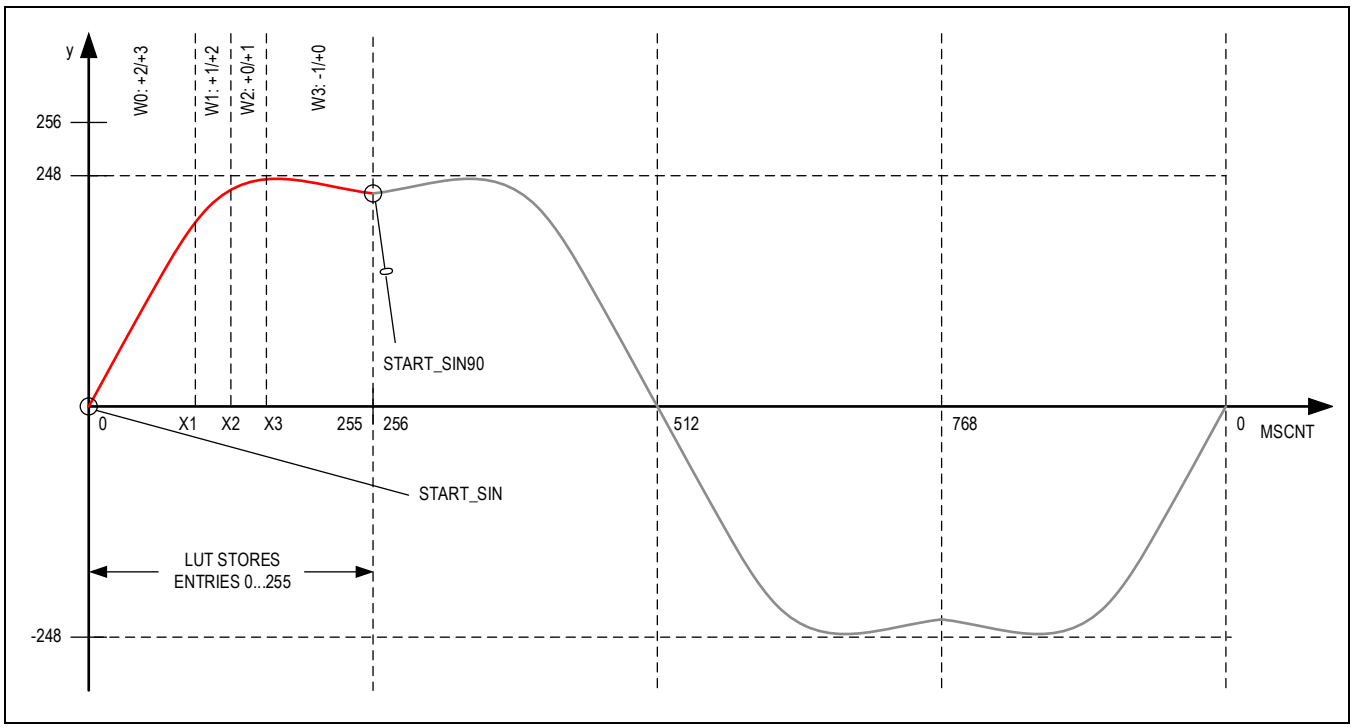


Figure 26. LUT Programming Example

When the microstep sequencer advances within the table, it calculates the actual current values for the motor coils with each microstep and stores them to the registers CUR_A and CUR_B. However, the incremental coding requires an absolute initialization, especially when the microstep table is modified. Therefore, CUR_A and CUR_B are initialized whenever MSCNT passes zero.

Matching the phase shift to the motor:

Two registers control the starting values of the tables.

- As the starting value at zero is not necessarily 0 (it can be 1 or 2), it can be programmed into the starting point register START_SIN.
- Similarly, the start of the second wave for the second motor coil must be stored in START_SIN90. This register stores the resulting table entry for a phase shift of 90° for a two-phase motor. To adapt for motor tolerances, the phase shift can be modified from 90° (256 microsteps) to anywhere between 45° and 135° by adding a microstep offset in the range of -127 to +127 (register OFFSET_SIN90). Motor tolerance requires moderate adaptations to a few 10 steps (maximum). The required correction offset can be found using StallGuard4 individual values SG4_IND and trimming the offset until both coils give a symmetrical result.

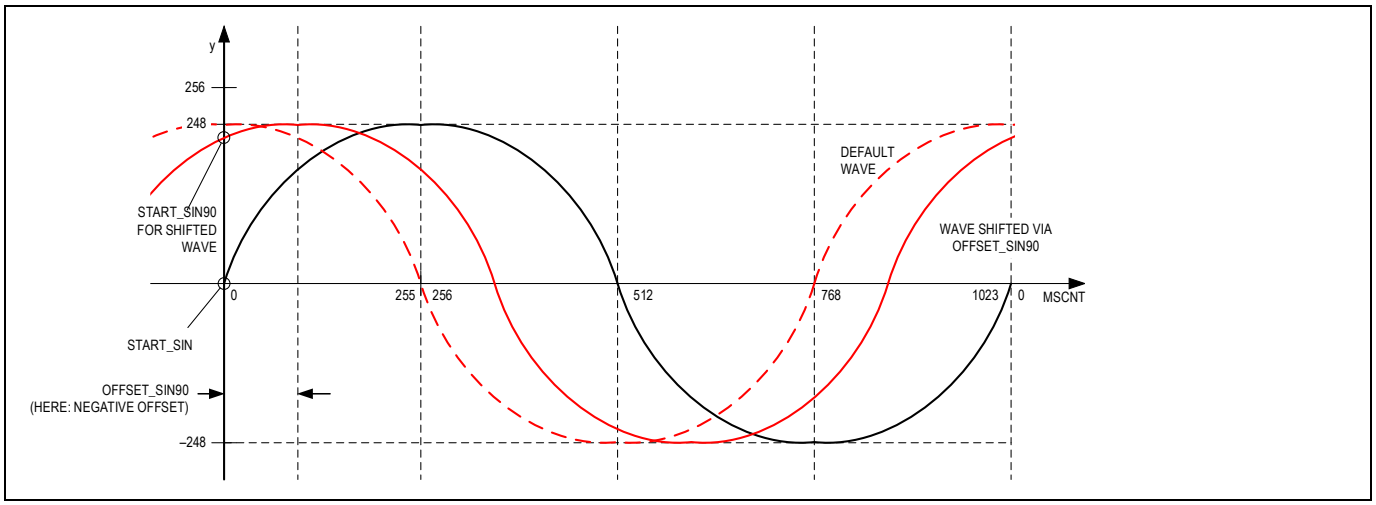


Figure 27. Shifting the Cosine Wave through OFFSET_SIN90

The default table is a good base for realizing an own table. This is an initialization example for the reset default microstep table:

MSLUT[0] = %10101010101010101011010101010100 = 0xAAAAB554

MSLUT[1] = %01001010100101010101010010101010 = 0x4A9554AA

MSLUT[2] = %00100100010010010010100100101001 = 0x24492929

MSLUT[3] = %00010000000100000100001000100010 = 0x10104222

MSLUT[4] = %11111011111111111111111111111111 = 0xFBFFFFFF

MSLUT[5] = %10110101101110110111011101111101 = 0xB5BB777D

MSLUT[6] = %01001001001010010101010101010110 = 0x49295556

MSLUT[7] = %00000000010000000100001000100010 = 0x00404222

MSLUTSEL = 0xFFFF8056:

X1 = 128, X2 = 255, X3 = 255

W3 = %01, W2 = %01, W1 = %01, W0 = %10

MSLUTSTART = 0x00F70000:

START_SIN_0 = 0, START_SIN90 = 247

To optimize the motor phase shift, run the motor at a medium velocity in StealthChop2 and set sg4_filt_en = 1. Adapt the phase offset to match the StallGuard4 results for phase A (SG4_IND_0+SG4_IND_1) to phase B (SG4_IND_2+SG4_IND_3).

If phase A value is > phase B value, increment OFFSET_SIN90, otherwise decrement. Repeat until best match is found. Be sure to enter the correct value for START_SIN90. For an offset of -10 to +9, use START_SIN90 = 247; up to -17 or +17, use START_SIN90 = 246. START_SIN is always 0.

ABN Incremental Encoder Interface

The TMC2241 is equipped with an incremental encoder interface for ABN encoders. The encoder gives positions through digital incremental quadrature signals (usually named A and B) and an index signal (usually named N for null, Z for zero, or I for index).

N Signal

The N signal can be used to clear the position counter or to take a snapshot. To continuously monitor the N channel and trigger the clearing of the encoder position or latching of the position, where the N channel event is detected, set the flag clr_cont. Alternatively, it is possible to react to the next encoder N channel event only, and automatically disable the

clearing or latching of the encoder position after the first N signal event (flag clr_once). This might be desired because the encoder gives this signal once for each revolution.

Checking for encoder latched event:

- **Option 1:** Check ENC_LATCH for change. It starts up with 0, and shows the encoder count where the N-event occurred, after starting motion for the first time. For consecutive rotations, it shows increased/decreased values, and thus, always changes.
- **Option 2:** Check for the interrupt output active and read the flag only following the active interrupt output. The DIAG0 pin must be configured for the interrupt lines using the bit diag0_nint_step from the GCONF register.

Some encoders require a validation of the N signal by a certain configuration of A and B polarity. This can be controlled by the pol_A and pol_B flags in the ENCMODE register. For example, when both pol_A and pol_B are set, an active N-event is only accepted during a high polarity of both A and B channels.

For clearing the encoder position ENC_POS with the next active N-event, set clr_enc_x = 1 and clr_once = 1, or clr_cont = 1.

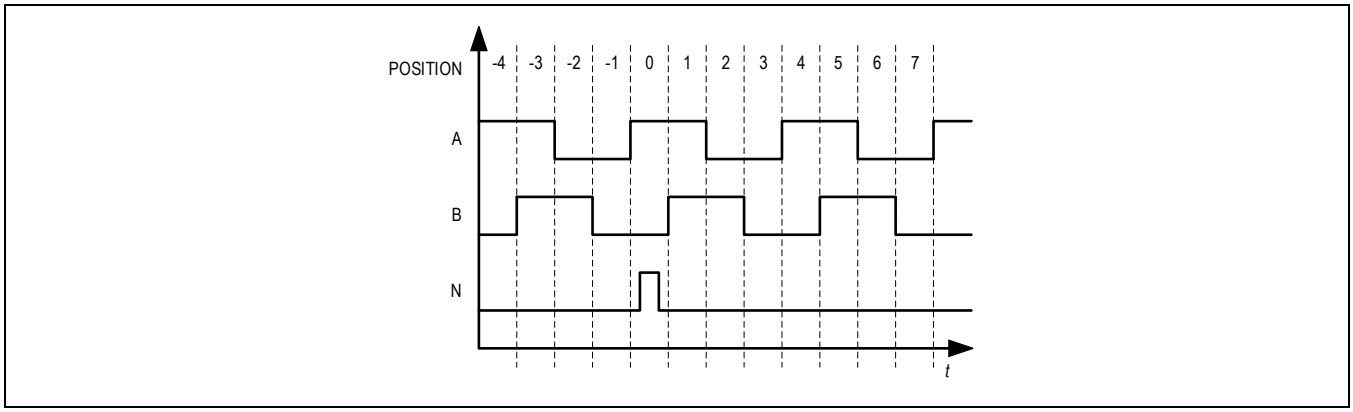


Figure 28. Outline of ABN Signals of an Incremental Encoder

The Encoder Counter X_ENC

The encoder counter X_ENC holds the current encoder position ready for read out. Different modes concerning handling of the signals A, B, and N consider active low and active high signals found with different types of encoders.

The Register ENC_STATUS

The register ENC_STATUS holds the status concerning the event of an encoder clear upon an N channel signal. The register ENC_LATCH always stores the actual encoder position on an N signal event.

The Encoder Constant ENC_CONST

The encoder constant (or encoder factor) ENC_CONST is added to or subtracted from the encoder counter on each polarity change of the quadrature signals AB of the incremental encoder. The encoder constant ENC_CONST represents a signed fixed point number (16.16) to facilitate the generic adaption between motors and encoders. In decimal mode, the lower 16 bits represent a number between 0 and 9999. For stepper motors equipped with incremental encoders, the fixed number representation allows very comfortable parameterization. Additionally, mechanical gearing can easily be considered. Negating the sign of ENC_CONST allows the inversion of the counting direction to match the motor and encoder direction.

Examples:

- Encoder factor of 1.0: ENC_CONST = 0x0001.0x0000 = FACTOR.FRACTION
- Encoder factor of -1.0: ENC_CONST = 0xFFFF.0x0000. This is the two's complement of 0x00010000. It equals (216 - (FACTOR + 1)) × (2^{16} - FRACTION).
- Decimal mode encoder factor 25.6: 00025.6000 = 0x0019.0x1770 = FACTOR.DECIMALS (DECIMALS = first four digits of fraction)
- Decimal mode encoder factor -25.6: (2^{16} – (25 + 1)) × (10000 - 6000) = (2^{16} – 26) × (4000) = 0xFFE6.0x0FA0
- A negative encoder constant is calculated using the following equation: (2^{16} - (FACTOR + 1)) × (10000 - DECIMALS)

Setting the Encoder to Match Motor Resolution

Encoder example settings for motor parameters:

- USC = 256 microsteps
- FSC = 200 fullstep motor
- Factor = FSC x USC/encoder resolution

Table 24. Encoder Example Settings for a 200 Fullstep Motor with 256 Microsteps

ENCODER RESOLUTION	REQUIRED ENCODER FACTOR	COMMENT
200	256	
360	142.2222 = 9320675.5555/216 = 1422222.2222/10000	No exact match possible!
500	102.4 = 6710886.4/216 = 1024000/10000	Exact match with decimal setting.
1000	51.2	Exact match with decimal setting.
1024	50	
4000	12.8	Exact match with decimal setting.
4096	12.5	
16384	3.125	

Example:

The encoder constant register can be programmed to 51.2 in decimal mode. Therefore, set:

ENC_CONST = 51 × 2 ^{16} + 0.2 × 10000

Reset, Disable/Stop, and Power Down

Emergency Stop

The driver provides a negative active enable pin DRV_ENN to safely switch off all power MOSFETs. This allows putting the motor into freewheeling. Further, it is a safe hardware function whenever an emergency stop not coupled to software is required. Some applications may require the driver to be put into a state with active holding current or with a passive braking mode. This is possible by programming the pin ENCA to act as a step disable function. Set GCONF flag stop_enable to activate this option. Whenever ENCA is pulled high and as long as it stays high, the motor stops abruptly and goes to the power-down state, as configured through IHOLD, IHOLD_DELAY, and StealthChop2 standstill options (in case StealthChop2 is in use).

External Reset and Sleep Mode

The reset and sleep mode are controlled with the SLEEPN pin.

A short pulse on SLEEPN with a duration >30µs results in a chip reset (also visible at the diagnostics outputs).

Very short pulses < 30µs are filtered out and do not have an effect on operation.

If SLEEPN is kept at GND, the IC goes into low-power standby state (sleep mode). All internal supplies are switched off.

In both cases (reset and standby), all internal register values and configurations are cleared and set to their defaults and power bridges are off.

After power-up or leaving sleep mode and reset condition, the registers must be reconfigured.

While reconfiguring the IC, it is advised to still hold the bridge drivers disabled with DRV_ENN.

Do not use during high motor velocity as energy fed back from the motor might damage the chip!

If not used, connect to V_S or V_{CC_IO} (this is a high-voltage pin).

Protections and Driver Diagnostics

The TMC2241 drivers supply a complete set of diagnostic and protection capabilities, like short-to-GND protection and undervoltage detection. A detection of an open load condition allows testing if a motor coil connection is interrupted. See the DRV_STATUS register table for details.

Besides the status flags, the TMC2241 allows measurement and readout of the chip temperature as well as feedback on the motor phase winding temperature.

For improved system reliability and overall circuit protection, the TMC2241 contains an overvoltage comparator and a trigger output OV to control external switches in terms of excessive supply voltage increase.

Overcurrent Protection

Overcurrent protection (OCP) protects the device against short circuits to the rails (supply voltage and ground) and between the outputs (OUT1A, OUT2A, OUT1B, OUT, and 2B).

The OCP threshold depends on the selected full-scale current range or see the *Electrical Characteristics* table for the respective threshold values.

The full-scale range is selected with the CURRENT_RANGE parameter in the DRV_CONF register.

If the output current is greater than the OCP threshold for longer than the deglitch time (blanking time), then an OCP event is detected.

When an OCP event is detected, the H-bridge is immediately disabled.

The short protection tries thrice before a fault flag (s2ga, s2gb, ss 2vsa, and s2vsb in DRV_STATUS register) is set and the bridge is continuously disabled.

The device is still alive and allows for configuration and status readout.

To re-enable the power bridge, the DRV_ENN pin must be cycled. Another option is to disable the power bridge with TOFF = 0 in CHOPCONF and re-enable the bridges with TOFF > 0.

Thermal Protection and Shutdown

The TMC2241 has an internal thermal protection.

If the die temperature exceeds 165°C (typical value), a fault indication as a fault flag (ot in DRV_STATUS) is raised and the driver is three-stated until the junction temperature drops below approximately 145°C (typical value). After that, the driver is re-enabled.

In addition, the TMC2241 supports ADC-based configurable thermal prewarning levels. This can be configured in the register OTW_OV_VTH using the parameter OVERTEMPPREWARNING_VTH. The ADC senses the chip average temperature, while the driver stages may be at a much higher temperature. This is only to specify that the TMC2241 can go into thermal shutdown and the prewarning may not be asserted, even if it is set at a low temperature.

Heat is mainly generated by the motor driver stages, and at increased voltage, by the internal voltage regulator. Most critical situations, where the driver MOSFETs can be overheated, are avoided when enabling the short-to-GND protection. For many applications, the overtemperature prewarning indicates an abnormal operation situation and can be used to initiate user warning or power reduction measures like motor current reduction. The thermal shutdown is just an emergency measure and temperature rising to the shutdown level should be prevented by design.

Temperature Measurement

The TMC2241 offers functions to measure the internal chip temperature as well as the motor temperature.

These diagnostic functions can be helpful in applications to monitor the chip or PCB temperature and the motor temperature development over time to increase system robustness or gather additional information for predictive maintenance.

Chip Temperature Measurement

Besides the overtemperature prewarning and overtemperature flags, the chip temperature itself can be determined using the ADC_TEMP parameter in the ADC_TEMP register.

The final temperature in degree Celsius can be calculated using the following formula:

$$TEMP[°C] = \frac{ADC_{TEMP} - 2038}{7.7}$$

Motor Temperature Measurement

The PWM_SCALE register shows the actual duty cycle in StealthChop2 operation. For a given motor current, the duty cycle depends on the phase resistance of the motor.

As the phase resistance is temperature dependent, PWM_SCALE can be used to estimate the actual motor temperature and monitor changes in the motor temperature over time.

This measurement is preferably done during motor standstill or slow movements.

Typically, the motor temperature does not change quickly.

Overvoltage Protection and OV Pin

A stepper motor application can generate significant overvoltage, especially when the motor is quickly decelerated from a high velocity, or when the motor stalls.

This voltage is fed back to the supply rails by the driver output stage.

For typical NEMA17 or larger motors, and also for smaller motors with sufficient flywheel mass, the energy fed back can be substantial, so that the power capacitors and circuit consumption are not sufficient to keep the supply within its limits.

To protect the driver as well as connected circuitry, the TMC2241 has an overvoltage detection and protection mechanism.

The OV output allows attaching an NPN or MOSFET with a power resistor (brake resistor) to dump the excess energy into the resistor.

The transistor chops with approximately 3kHz to 4kHz (depending on the clock frequency) to keep the supply within the limits.

The supply voltage is permanently monitored with the internal ADC.

The upper level for the supply voltage for a given application can be configured in the register OTW_OV_VTH using the parameter OVERVOLTAGE_VTH.

The actual ADC value for the supply voltage can be read using the register ADC_VSUPPLY_AIN as the parameter ADC_VSUPPLY.

Use the following equation to convert from the ADC value to V_S and vice versa:

V_S = ADC_VSUPPLY × 17.6mV

The OV output pin shows the actual state of the overvoltage monitor.

As soon as and as long as ADC_VSUPPLY is greater or equal to OVERVOLTAGE_VTH, the OV output pin changes to three-state/'Z'.

The OV output pin is an open-drain pin. *Figure 29* shows an example of a brake chopper circuit.

Take special care if the device is put into sleep mode (SLEEPN = LOW). In this case, OV is floating.

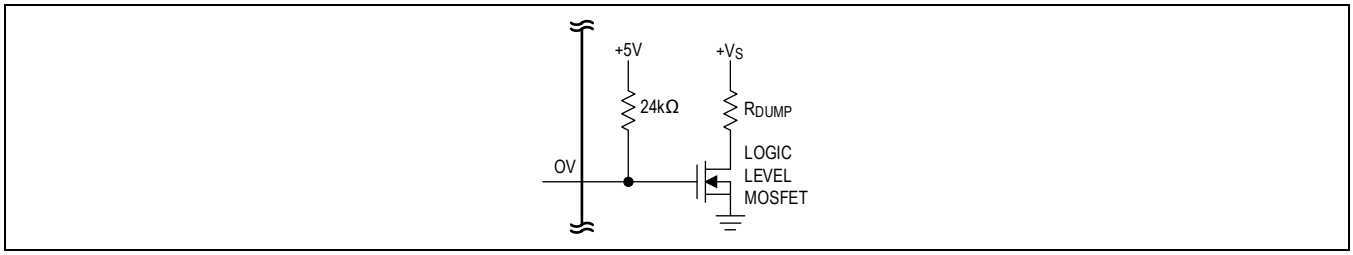


Figure 29. Brake Chopper Circuit Example

Short Protection (Short-to-GND and Short-to-VS)

The TMC2241 power stages are protected against a short-circuit condition by an additional measurement of the current flowing through the high-side MOSFETs. This is important, as most short circuit conditions result from a motor cable insulation defect, for example, when touching the conducting parts connected to the system ground. The short detection is protected against spurious triggering, for example, by electrostatic discharges (ESD), by retrying thrice before switching off the motor.

Once a short condition is safely detected, the corresponding driver bridge is switched off, and the s2ga or s2gb flag is set. To restart the motor, intervene by disabling and re-enabling the driver. Note that the short-to-GND protection cannot protect the system and the power stages for all possible short events, as a short event is rather undefined and a complex network of external components may be involved. Therefore, short circuits should basically be avoided.

Depending on the full-scale current setting, the low-side short protection triggers at different overcurrent protection thresholds.

Table 25. Overcurrent Protection Thresholds Based on the Full-Scale Current Setting

FULL-SCALE CURRENT SETTING (BITS)	OVERCURRENT PROTECTION THRESHOLD [A]
10 (and 11)	5.0
01	3.33
00	1.67

Open Load Diagnostics

Interrupted cables are a common cause for systems failing, for example, when connectors are not firmly plugged. The TMC2241 detects open load conditions by checking if it can reach the desired motor coil current. This way, undervoltage conditions, high motor velocity settings or short, and overtemperature conditions may cause triggering of the open load flag. In motor standstill, open load cannot be measured as the coils might eventually have zero current.

To safely detect an interrupted coil connection, operate in SpreadCyle and check the open load flags following a motion of minimum four times the selected microstep resolution (= four fullsteps) into a single direction using low or nominal motor velocity operation only. However, the ola and olb flags have just informative character and do not cause any action of the driver.

Undervoltage Lockout Protection

The TMC2241 features an UVLO protection for V_S, V_{CC_IO}, and the charge pump.

The UVLO condition on V_S is triggered below 4.05V (max).

The UVLO condition on V_{CC_IO} is triggered below 1.95V (max).

The UVLO condition on the charge pump is triggered in case of an error condition of the charge pump, for example, due to a wrong capacitor value.

A V_S UVLO condition can be read from the register GSTAT as flag vm_uvlo. This flag is a write-clear flag. It must be actively set to 1 to clear it.

During a V_{CC_IO} UVLO, no communication with the IC is possible and the driver is disabled. The DIAG0 pin is active low (open-drain).

Electrostatic Discharge (ESD) Protection

The chip has internal ESD protection on every pin.

The TMC2241 motor phase output pins are protected up to 8kV HBM in the application when using a bypass capacitor of at least 1µF on the positive voltage supply (V_S pins).

This is not protection against the hot plugging of a motor.

External Analog Input AIN Monitoring

The TMC2241 offers an external analog input AIN, which is continuously sampled with the internal ADC.

The ADC sample value can be read out from the parameter ADC_AIN in the register ADC_VSUPPLY_AIN.

Use the following equation to convert from the ADC value to V_{AIN} and vice versa:

V_{AIN} = ADC_AIN × 305.2µV

The AIN input can be used to monitor the external analog variables and parameters that may represent system level conditions and provide additional feedback on the system state.

Clock Oscillator and Clock Input

Using the Internal Clock

Directly tie the CLK input pin to GND close to the IC if the internal clock oscillator is to be used. The internal clock runs at a typical frequency of 12.5MHz.

Using an External Clock

When an external clock is available, a frequency of 8MHz to 20MHz is recommended for optimum performance.

The required minimum and maximum duty cycle of the clock signal is defined in the *Electrical Characteristics.*

Especially at clock frequencies close to 20MHz, the clock's duty cycle requirements must be satisfied.

Make sure the clock source supplies clean CMOS output logic levels and steep slopes when using a high clock frequency.

The external clock input is enabled as soon as an external clock is provided at the CLK pin.

Reading out bit ext_clk in the register IOIN gives feedback on which clock source is currently in use (1 = external clock).

In case the external clock fails or is switched off, the internal clocks takes over seamlessly and automatically to protect the driver from damage.

Quick Configuration Guide

This guide is meant as a practical tool for a first register configuration and a minimum set of measurements and decisions to tune the driver. It does not cover all advanced functionalities and options but concentrates on the basic function set to run a motor smoothly. Once the motor runs, explore additional features and further functionality in more detail. A current probe on one motor coil is a good aid to find the best settings.

Current Setting

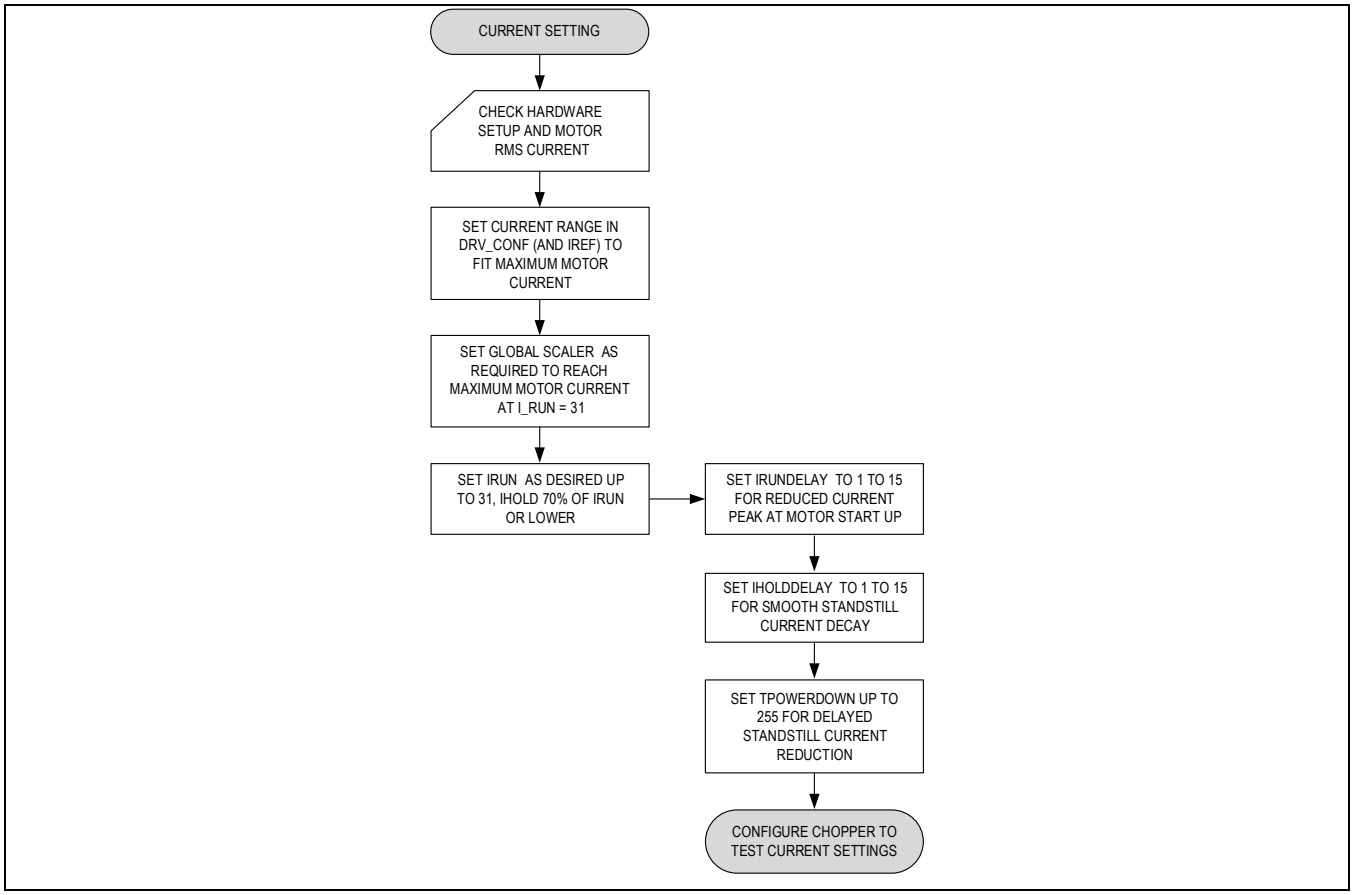


Figure 30. Quick Configuration Guide for Current Setting

StealthChop2 Configuration

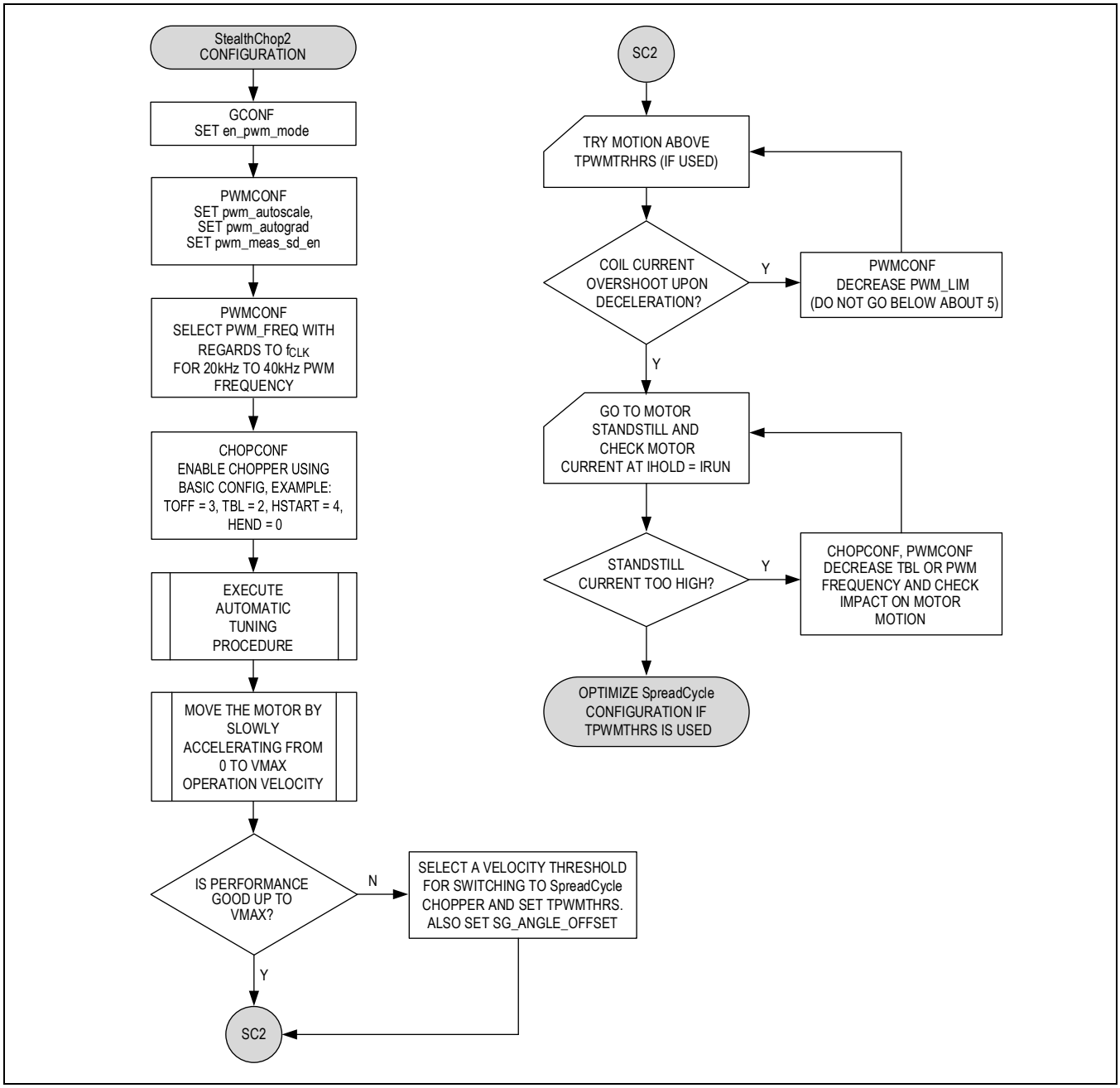


Figure 31. Quick Configuration Guide for StealthChop2 Configuration

SpreadCycle Configuration

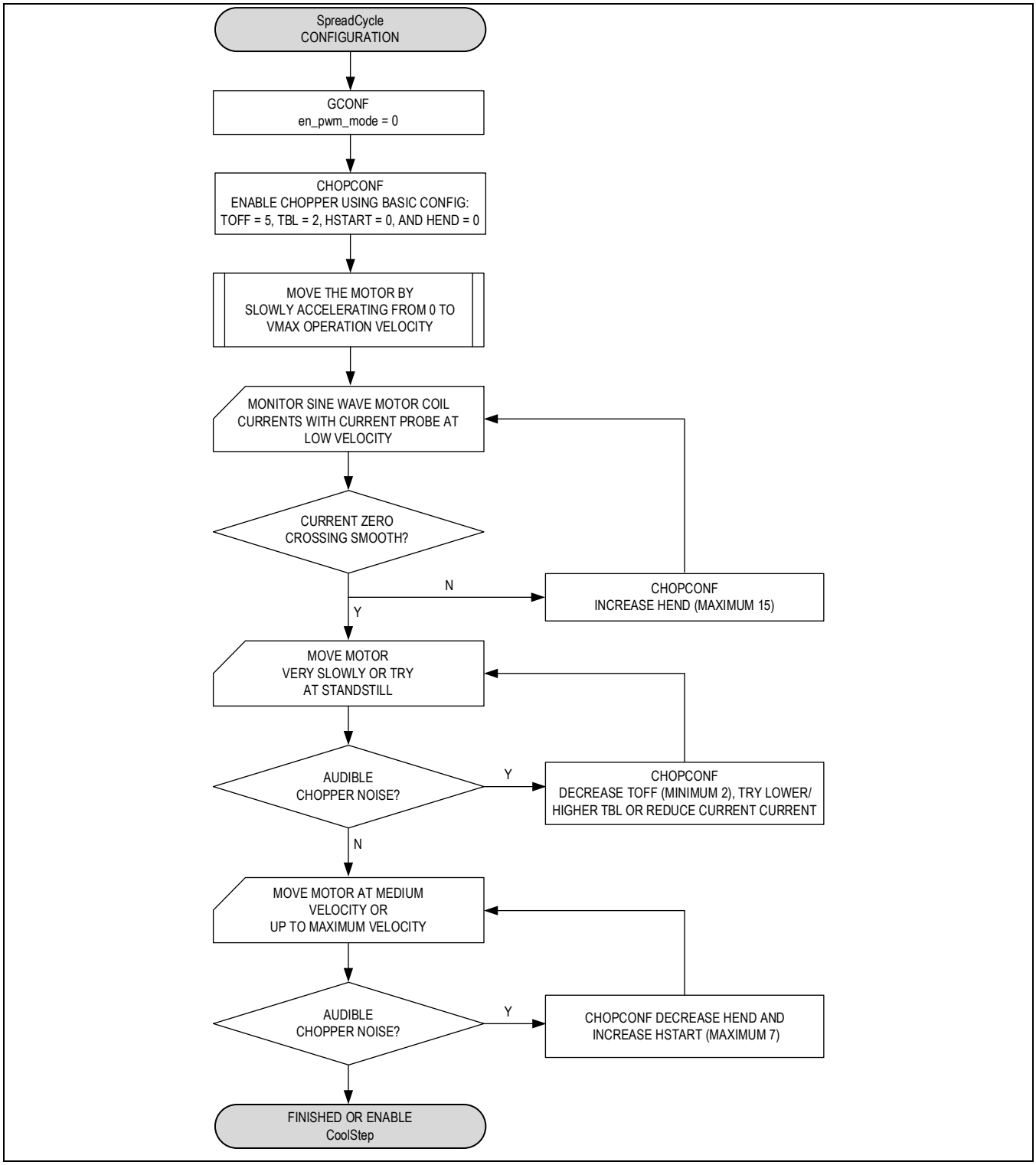


Figure 32. Quick Configuration Guide for SpreadCycle

Enabling CoolStep in Combination with StealthChop2

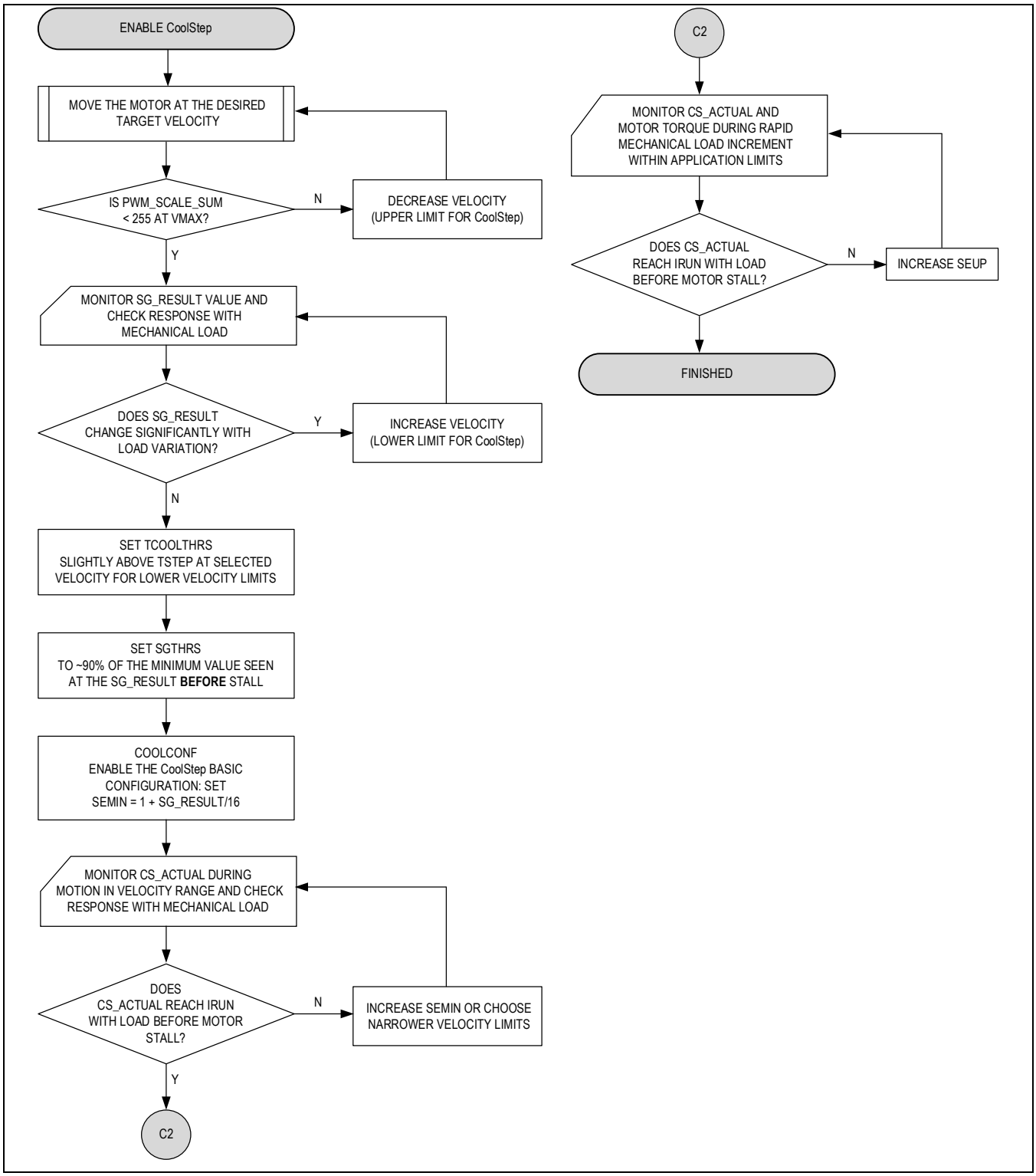


Figure 33. Quick Configuration Guide for CoolStep with StealthChop2

Enabling CoolStep in Combination with SpreadCycle

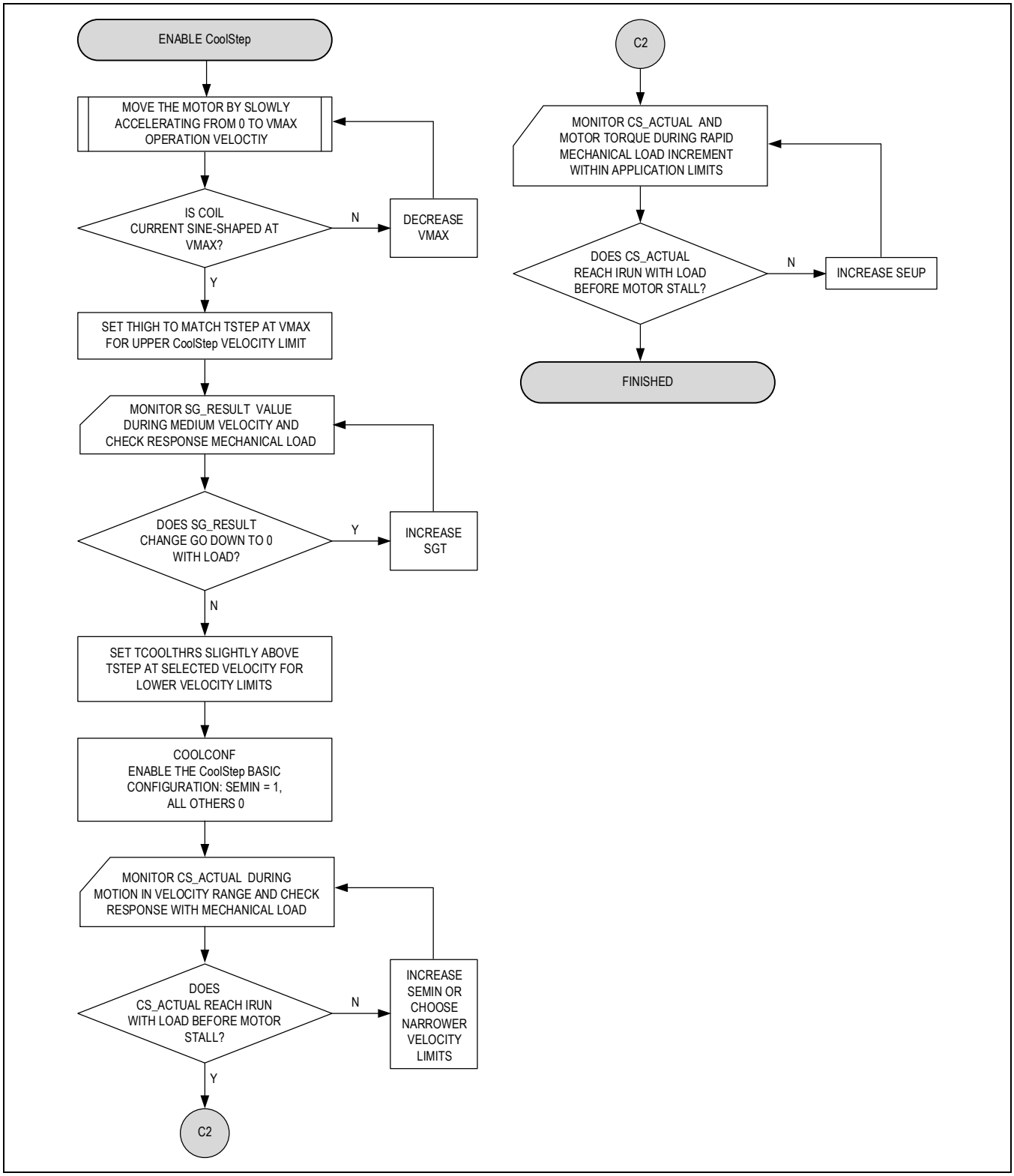


Figure 34. Quick Configuration Guide for CoolStep with SpreadCycle

General Register Mapping and Register Information

This section gives some general information on the register map.

The Register Map section gives details on all the registers and their content.

- All registers are reset to 0 upon power up, unless otherwise noted.

- Add 0x80 to the address Addr for write accesses!

Table 26. Overview of Register Map

REGISTERS	DESCRIPTION
General Configuration Registers	These registers contain: • Global configuration • Global status flags • Interface configuration • I/O signal configuration
Velocity Dependent Driver Feature Control Register Set	This register set offers registers for: • Driver current control • Setting thresholds for CoolStep operation • Setting thresholds for different chopper modes
Direct Mode Registers	This register group offers registers used for the direct coil current control mode.
Encoder Register Set	The encoder register set offers all registers needed for proper ABN encoder operation.
ADC Registers	This register group offers registers to control and read the internal ADC.
Motor Driver Register Set	This register set offers registers for: • Setting/reading out microstep table and counter • Chopper and driver configuration • CoolStep and StallGuard configuration • Reading out StallGuard values and driver error flags

Typical Application Circuits

Standard Application Circuit

The standard application circuit uses a minimum set of additional components. Use low ESR electrolytic capacitors to filter the power supply. The capacitors must cope with the current ripple caused by the chopper operation. A minimum capacity of 100µF at V_S is recommended for best performance. The current ripple in the supply capacitors also depends on the power supply internal resistance and cable length. V_{CC_IO} must be supplied from an external source, for example, a low drop 3.3V regulator.

Place all the filter capacitors as close as possible to the related IC pins. Use a solid common ground plane for all GND connections. Connect the V_{DD1V8} filtering capacitor directly to the V_{DD1V8} pin.

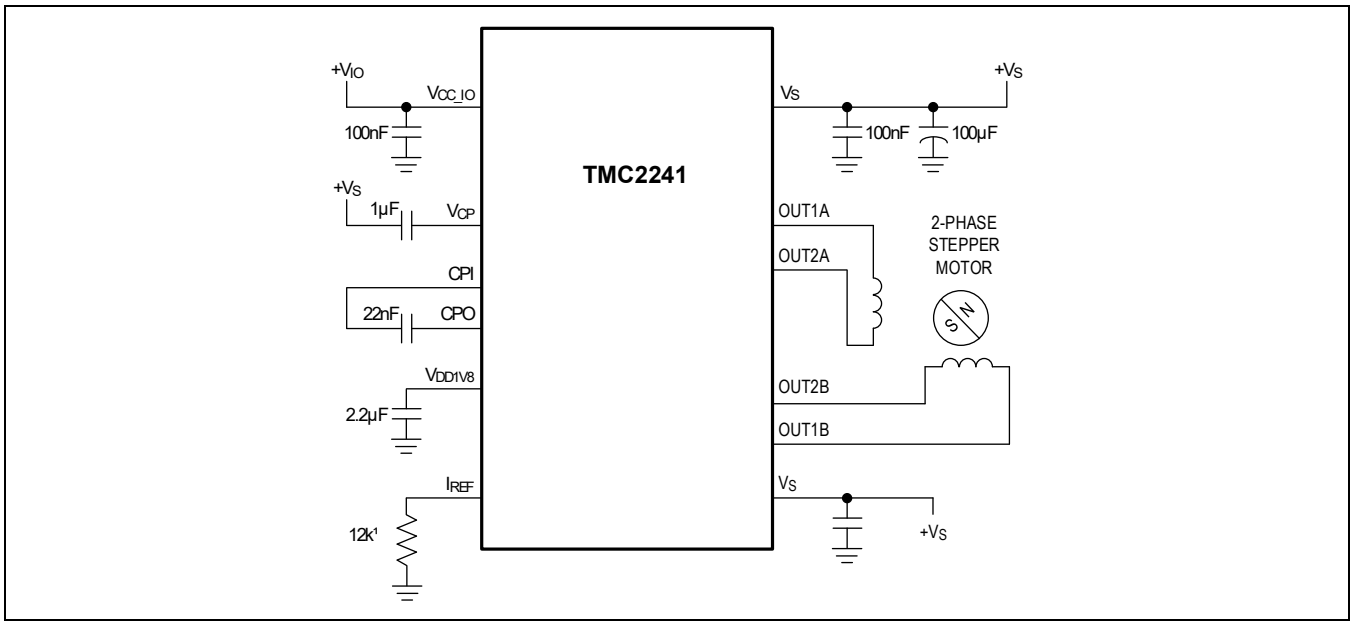


Figure 35. Standard Application Circuit

High Motor Current

When operating at a high motor current, the driver power dissipation due to MOSFET switch-on resistance significantly heats up the driver. This power dissipation heats up the PCB cooling infrastructure also, if operated at an increased duty cycle. This in turn leads to a further increase of driver temperature. An increase of temperature by about 100°C increases MOSFET resistance by roughly 50%. This is a typical behavior of MOSFET switches. Therefore, under high duty cycle and high load conditions, thermal characteristics must be carefully considered, especially when increased environment temperatures are to be supported. See the **Package Information** for the thermal characteristics and online evaluation kit information for the layout example.

As a rule of thumb, thermal properties of the PCB design may become critical at supply voltages above 24V or with a motor current above $1.5A_{RMS}$ for increased periods of time. Note that the resistive power dissipation rises with the square of the motor current. On the other hand, this means that a small reduction of motor current significantly saves heat dissipation and energy.

Slope Control

The driver allows the selection of slope control in four steps from 100V/µs to 800V/µs. A faster slope generates less driver power dissipation, while a slower slope produces less electromagnetic emission. Generally, the fastest slope setting matches most applications, as keeping power dissipation low is essential to reduce device heat-up. Especially, applications working at motor current >1A and supply voltage >24V benefit from fastest slope setting. If electromagnetic emission proves critical, try reducing slope, but carefully monitor the device temperature. The slope settings of 100V/µs should only be used in low supply voltage applications like 14V and below.

Driver Protection and EME Circuitry

Some applications have to cope with ESD events caused by motor operation or external influence. Despite ESD circuitry within the driver chips, ESD events occurring during operation can cause a reset or even a destruction of the motor driver, depending on their energy. Especially, plastic housings and belt drive systems tend to cause ESD events of several kV. It is best practice to avoid ESD events by attaching all conductive parts, especially the motors themselves to PCB ground, or to apply electrically conductive plastic parts. In addition, the driver can be protected up to a certain degree against ESD events or live plugging/pulling the motor, which also causes high voltages and high currents into the motor connector terminals.

A simple scheme uses capacitors at the driver outputs to reduce the dV/dt caused by ESD events. Larger capacitors bring more benefit concerning ESD suppression, but cause additional current flow in each chopper cycle, and thus, increase driver power dissipation, especially at high supply voltages. The values shown are example values (they might be varied between 100pF and 1nF). The capacitors also dampen high-frequency noise injected from the digital parts of the application PCB circuitry, and thus, reduce electromagnetic emission.

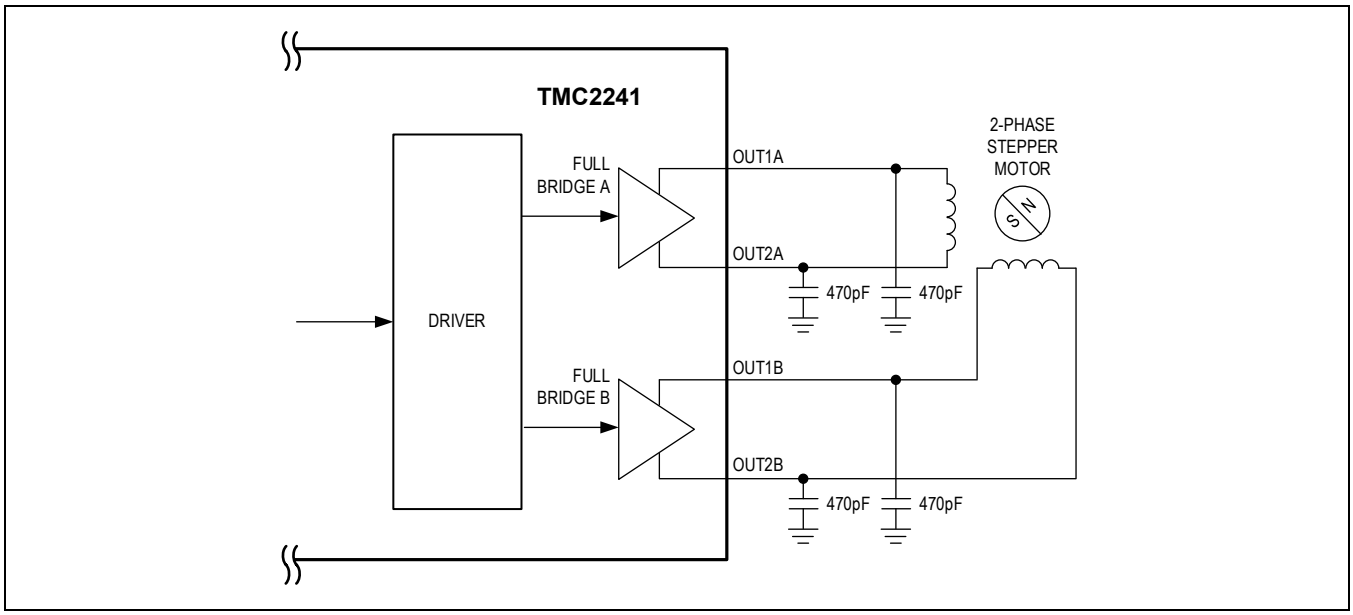


Figure 36. Simple ESD Enhancement

A more elaborate scheme uses LC filters to decouple the driver outputs from the motor connector. Varistors V1 and V2 between the coil terminals eliminate coil overvoltage caused by live plugging. Optionally, protect all outputs by a varistor (V1A, V1B, V2A, and V2B) against the ESD voltage. Fit the varistors to the supply voltage rating. The surface-mount device (SMD) inductivities conduct full motor coil current and must be selected accordingly.

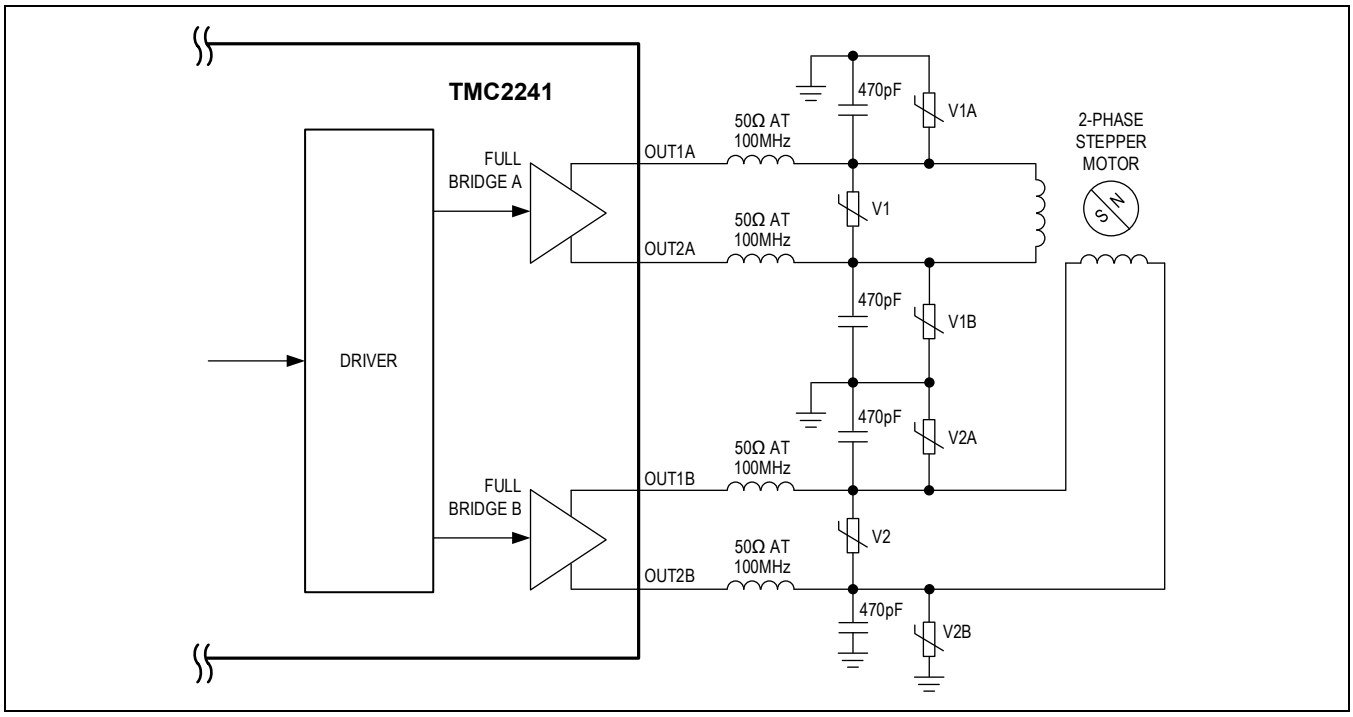


Figure 37. Extended Motor Output Protection

Register Map

GCR Register Overview

Shows all related registers of the GCR block

ADDRESS AND NAME	FIELDS				MSB (TOP LEFT) TO LSB (BOTTOM RIGHT)			
0x00 **GCR.GCONF**								
								direct_mode
	stop_enable	small_ hysteresis	diag1_ pushpull	diag0_ pushpull		diag1_ onstate	diag1_index	diag1_stall
	diag0_stall	diag0_otpw	diag0_error	shaft	multistep_filt	en_pwm_ mode	fast_ standstill	
0x01 **GCR.GSTAT**								
				vm_uvlo	register_ reset	uv_cp	drv_err	reset
0x02 **GCR.IFCNT**								
	IFCNT							
0x03 **GCR.NODECONF**								
					SENDDELAY			
	NODEADDR							
0x04 **GCR.IOIN**	VERSION							
						SILICON_RV		
	ADC_ERR	EXT_CLK	EXT_RES_ DET	OUTPUT	COMP_B1_ B2	COMP_A1_ A2	COMP_B	COMP_A
	reserved	UART_EN	ENCN	DRV_ENN	ENCA	ENCB	DIR	STEP
0x07 **GCR.DIAG_CONF**					diag1_ overvoltage	diag1_ev_n		
					diag1_index	diag1_stall	diag1_otpw	diag1_error
					diag0_ overvoltage	diag0_ev_n		
					diag0_index	diag0_stall	diag0_otpw	diag0_error
0x0A **GCR.DRV_CONF**								
			SLOPE_CONTROL				CURRENT_RANGE	

ADDRESS AND NAME	FIELDS							MSB (TOP LEFT) TO LSB (BOTTOM RIGHT)
0x0B **GCR.GLOBAL_SCALER**								
	GLOBALSCALER							
0x10 **VDR.IHOLD_IRUN**					IRUNDELAY			
					IHOLDDELAY			
				IRUN				
				IHOLD				
0x11 **VDR.TPOWERDOWN**								
	TPOWERDOWN							
0x12 **VDR.TSTEP**								
					TSTEP[19:16]			
	TSTEP[15:8]							
	TSTEP[7:0]							
0x13 **VDR.TPWMTHRS**								
					TPWMTHRS[19:16]			
	TPWMTHRS[15:8]							
	TPWMTHRS[7:0]							
0x14 **VDR.TCOOLTHRS**								
					TCOOLTHRS[19:16]			
	TCOOLTHRS[15:8]							
	TCOOLTHRS[7:0]							
0x15 **VDR.THIGH**								
					THIGH[19:16]			
	THIGH[15:8]							
	THIGH[7:0]							
0x2D **DMR.DIRECT_MODE**								DIRECT_ COIL_B[8]
	DIRECT_COIL_B[7:0]							
								DIRECT_ COIL_A[8]
	DIRECT_COIL_A[7:0]							
0x38 **ER.ENCMODE**								
						enc_sel_ decimal		clr_enc_x
	pos_neg_edge		clr_once	clr_cont	ignore_AB	pol_N	pol_B	pol_A

ADDRESS AND NAME	FIELDS	MSB (TOP LEFT) TO LSB (BOTTOM RIGHT)
0x39 **ER.X_ENC**	X_ENC[31:24]	
	X_ENC[23:16]	
	X_ENC[15:8]	
	X_ENC[7:0]	
0x3A **ER.ENC_CONST**	ENC_CONST[31:24]	
	ENC_CONST[23:16]	
	ENC_CONST[15:8]	
	ENC_CONST[7:0]	
0x3B **ER.ENC_STATUS**		
		n_event
0x3C **ER.ENC_LATCH**	ENC_LATCH[31:24]	
	ENC_LATCH[23:16]	
	ENC_LATCH[15:8]	
	ENC_LATCH[7:0]	
0x50 **ADC_Registers.ADC_VSUPPLY_AIN**		ADC_AIN[12:8]
	ADC_AIN[7:0]	
		ADC_VSUPPLY[12:8]
	ADC_VSUPPLY[7:0]	
0x51 **ADC_Registers.ADC_TEMP**		RESERVED[12:8]
	RESERVED[7:0]	
		ADC_TEMP[12:8]
	ADC_TEMP[7:0]	
0x52 **ADC_Registers.OTW_OV_VTH**		OVERTEMPPREWARNING_VTH[12:8]
	OVERTEMPPREWARNING_VTH[7:0]	
		OVERVOLTAGE_VTH[12:8]
	OVERVOLTAGE_VTH[7:0]	
0x60 **MDR.MSLUT_0**	MSLUT_0[31:24]	
	MSLUT_0[23:16]	
	MSLUT_0[15:8]	
	MSLUT_0[7:0]	
0x61 **MDR.MSLUT_1**	MSLUT_1[31:24]	
	MSLUT_1[23:16]	
	MSLUT_1[15:8]	
	MSLUT_1[7:0]	

ADDRESS AND NAME	FIELDS	MSB (TOP LEFT) TO LSB (BOTTOM RIGHT)							
0x62 **MDR.MSLUT_2**	MSLUT_2[31:24]								
	MSLUT_2[23:16]								
	MSLUT_2[15:8]								
	MSLUT_2[7:0]								
0x63 **MDR.MSLUT_3**	MSLUT_3[31:24]								
	MSLUT_3[23:16]								
	MSLUT_3[15:8]								
	MSLUT_3[7:0]								
0x64 **MDR.MSLUT_4**	MSLUT_4[31:24]								
	MSLUT_4[23:16]								
	MSLUT_4[15:8]								
	MSLUT_4[7:0]								
0x65 **MDR.MSLUT_5**	MSLUT_5[31:24]								
	MSLUT_5[23:16]								
	MSLUT_5[15:8]								
	MSLUT_5[7:0]								
0x66 **MDR.MSLUT_6**	MSLUT_6[31:24]								
	MSLUT_6[23:16]								
	MSLUT_6[15:8]								
	MSLUT_6[7:0]								
0x67 **MDR.MSLUT_7**	MSLUT_7[31:24]								
	MSLUT_7[23:16]								
	MSLUT_7[15:8]								
	MSLUT_7[7:0]								
0x68 **MDR.MSLUTSEL**	X3								
	X2								
	X1								
	W3		W2		W1		W0		
0x69 **MDR.MSLUTSTART**	OFFSET_SIN90								
	START_SIN90								
	START_SIN								
0x6A **MDR.MSCNT**									
							MSCNT[9:8]		
	MSCNT[7:0]								

ADDRESS AND NAME	FIELDS				MSB (TOP LEFT) TO LSB (BOTTOM RIGHT)			
0x6B **MDR.MSCURACT**								CUR_A[8]
	CUR_A[7:0]							
								CUR_B[8]
	CUR_B[7:0]							
0x6C **MDR.CHOPCONF**	diss2vs	diss2g	dedge	intpol	MRES			
	TPFD				vhighchm	vhighfs		TBL[1]
	TBL[0:0]	chm		disfdcc	fd3	HEND_OFFSET[3:1]		
	HEND_OFFSET[0:0]	HSTRT_TFD210			TOFF			
0x6D **MDR.COOLCONF**								sfilt
		sgt						
	seimin	sedn			semax			
		seup			semin			
0x6F **MDR.DRV_STATUS**	stst	olb	ola	s2gb	s2ga	otpw	ot	stallguard
				CS_ACTUAL				
	fsactive	stealth	s2vsb	s2vsa			SG_RESULT[9:8]	
	SG_RESULT[7:0]							
0x70 **MDR.PWMCONF**	PWM_LIM			PWM_REG				
	pwm_dis_reg_stst	pwm_meas_sd_enable	FREEWHEEL		pwm_autograd	pwm_autoscale	PWM_FREQ	
	PWM_GRAD							
	PWM_OFS							
0x71 **MDR.PWM_SCALE**								PWM_SCALE_AUTO[8]
	PWM_SCALE_AUTO[7:0]							
							PWM_SCALE_SUM[9:8]	
	PWM_SCALE_SUM[7:0]							
0x72 **MDR.PWM_AUTO**								
	PWM_GRAD_AUTO							
	PWM_OFS_AUTO							
0x74 **MDR.SG4_THRS**								
						sg4_thrs_shl	sg_angle_offset	sg4_filt_en
	SG4_THRS							

ADDRESS AND NAME	FIELDS						MSB (TOP LEFT) TO LSB (BOTTOM RIGHT)	
0x75 **MDR.SG4_RESULT**								
							SG4_RESULT[9:8]	
	SG4_RESULT[7:0]							
0x76 **MDR.SG4_IND**	SG4_IND_3							
	SG4_IND_2							
	SG4_IND_1							
	SG4_IND_0							

0x00: GCR.GCONF

Global Configuration Flags

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[16] **direct_mode**	RW 0x0	Enable direct motor phase current control using serial interface.
	0: NORMAL_MODE 1: DIRECT_MODE	Normal operation Motor coil currents and polarity directly programmed using serial interface: Register DIRECT_MODE(0x2D) specifies signed coil A current (bits 8..0) and coil B current (bits 24..16). In this mode, the current is scaled by the IHOLD setting. Velocity-based current regulation of StealthChop2 is not available in this mode. The automatic StealthChop2 current regulation works only for low stepper motor velocities.
[15] **stop_enable**	RW 0x0	Motor hard stop function enable.
	0: NORMAL 1: EM_STOP	Normal operation Emergency stop: ENCA stops the sequencer when tied high (no steps are executed by the sequencer, motor goes to standstill state).
[14] **small_hysteresis**	RW 0x0	
	0: HYST_1_16 1: HYST_1_32	Hysteresis for step frequency comparison is 1/16. Hysteresis for step frequency comparison is 1/32
[13] **diag1_pushpull**	RW 0x0	DIAG1 output type configuration.
	0: OPEN_DRAIN 1: PUSH_PULL	DIAG1 is open collector output (active low). Enable DIAG1 push pull output (active high).
[12] **diag0_pushpull**	RW 0x0	DIAG0 output type configuration.
	0: OPEN_DRAIN 1: PUSH_PULL	DIAG0_SW is open collector output (active low). Enable DIAG0_SW push pull output (active high).
[10] **diag1_onstate**	RW 0x0	DIAG1 output configuration.
	0: DISABLED 1: ONSTATE	Disable DIAG1active on chopper on. diag1_onstate. Enable DIAG1 active when chopper is on (for the coil in the second half of the fullstep).

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[9] **diag1_index**	RW 0x0	DIAG1 output configuration.
	0: DISABLED 1: INDEX	Disable DIAG1 active on index position. diag1_index. Enable DIAG1 active on index position (microstep lookup table position 0).
[8] **diag1_stall**	RW 0x0	DIAG1 output configuration.
	0: DISABLED 1: STALL_1	diag1_stall. Motor stallnot indicated at DIAG1. diag1_stall. Enable DIAG1 active on motor stall (set TCOOLTHRS before using this feature).
[7] **diag0_stall**	RW 0x0	DIAG0 output configuration.
	0: DISABLED 1: STALL_0	diag0_stall. Motor stallnot indicated at DIAG0 diag0_stall. Enable DIAG0 active on motor stall (set TCOOLTHRS before using this feature).
[6] **diag0_otpw**	RW 0x0	DIAG0 output configuration.
	0: DISABLED 1: OTPW	Disable DIAG0 active on driver over temperature prewarning. Enable DIAG0 active on driver over temperature prewarning (otpw).
[5] **diag0_error**	RW 0x0	DIAG0 output configuration. DIAG0 always shows the reset-status, that is, it is active low during reset condition.
	0: DISABLED 1: ERROR	Disable DIAG0 active on driver errors. Enable DIAG0 active on driver errors: Overtemperature (ot), short-to-GND (s2g), undervoltage chargepump (uv_cp).
[4] **shaft**	RW 0x0	Change motor direction/direction sign.
	0: DIR 1: DIR_INV	Default motor direction Inverse motor direction
[3] **multistep_filt**	RW 0x0	Enable step input filtering for StealthChop2.
	0: FILT_DIS 1: FILT_EN	Step input filtering disabled. Enable step input filtering for StealthChop2 optimization with external step source (default = 1).
[2] **en_pwm_mode**	RW 0x0	Enable the StealthChop2 mode.
	0: SPREADCYCLE 1: STEALTHCHOP	No StealthChop2 StealthChop2 voltage PWM-mode enabled (depending on velocity thresholds). Switch from off to on state while in standstill and at IHOLD = nominal IRUN current only.
[1] **fast_standstill**	RW 0x0	Timeout for step execution until standstill detection.
	0: STST_2_20 1: STST_2_18	Normal time: 2^20 clocks Short time: 2^18 clocks

0x01: GCR.GSTAT

Global Status Flags
(Rewrite with '1' bit to clear respective flags).

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[4] **vm_uvlo**	RW, W1C 0x1	1: VM undervoltage occured since last reset. (**Hint:** Is active after initial bootup. Clear flag after bootup to detect fault when device is operating).
	0: OPERATIONAL 1: VM_UVLO_DET	Normal operation VM undervoltage is detected since last reset.
[3] **register_reset**	RW, W1C 0x1	**Hint:** IS active after initial bootup. Clear flag after bootup to detect regmap reset when device is operating.
	0: OPERATIONAL 1: REG_RES_DET	Normal operation Indicates the registermap is reset. All registers are cleared to reset values.
[2] **uv_cp**	RW, W1C 0x1	Charge pump undervoltage condition flag. (**Hint:** Is active after initial bootup. Clear flag after bootup to detect fault when device is operating) #type=COW
	0: OPERATIONAL 1: UV_CP_DET	Normal operation Indicates an undervoltage on the charge pump. The driver is disabled during undervoltage. This flag is latched for information.
[1] **drv_err**	RW, W1C 0x0	Driver error flag #type=COW
	0: OPERATIONAL 1: DRV_DIS_DET	Normal operation Indicates, the driver is shut down due to overtemperature or short circuit detection. Read DRV_STATUS for details. The flag can only be cleared when the temperature is below the limit again.
[0] **reset**	RW, W1C 0x1	Reset flag (**hint:** is active after initial bootup. Clear flag after bootup to detect device is reset during operation) #type=COW
	0: NO_RESET 1: RESET_DET	Normal operation Indicates the IC is reset.

0x02: GCR.IFCNT

Interface Transmission Counter
This register is incremented with each successful UART interface write access. It can be read out to check the serial transmission for lost data. Read accesses do not change the content. Disabled in SPI operation. The counter wraps around from 255 to 0.

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[7:0] **IFCNT**	R, unsigned 0x00	Interface transmission counter. This register is incremented with each successful UART interface write access. It can be read out to check the serial transmission for lost data. Read accesses do not change the content. Disabled in SPI operation. The counter wraps around from 255 to 0.

0x03: GCR.NODECONF

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[11:8] **SENDDELAY**	RW 0x0	SWUART programmable response delay after read request.
	0: BIT_T_8 2: BIT_T_24 4: BIT_T_40 6: BIT_T_56 8: BIT_T_72 10: BIT_T_88 12: BIT_T_104 14: BIT_T_120	8-bit times (not allowed with multiple nodes) 3 × 8-bit times 5 × 8-bit times 7 × 8-bit times 9 × 8-bit times 11 × 8-bit times 13 × 8-bit times 15 × 8-bit times
[7:0] **NODEADDR**	RW, unsigned 0x00	NODEADDR: These eight bits set the address of unit for the UART interface. The address is incremented by one up to seven, as defined by SDI, SCK, CSN. CSN, SCK, and SDI. 000: +0 001: +1 010: +2 011: +3 100: +4 101: +5 110: +6 111: +7 Range: 0 to 254 (do not increment beyond 254).

0x04: GCR.IOIN

Reads the state of all input pins available and returns IC revision in highest byte.

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:24] **VERSION**	R, unsigned 0x00	0x40 = first version of the IC. Identical numbers mean full digital compatibility.
[18:16] **SILICON_RV**	R, unsigned 0x0	Silicon revision number
[15] **ADC_ERR**	R 0x0	1: Signals the ADC is not working correctly. Do not utilize ADC-features. ADC is stuck in configuration mode and very likely does not receive an ACK_OUT.
[14] **EXT_CLK**	R 0x0	0: The internal oscillator is used for generating the clock-signal (12.5 MHz). 1: The external oscillator is used for generating the clock-signal.
	0: INT_OSC 1: EXT_OSC	Uses internal 12.5 MHz oscillator. External clock is detected and used.
[13] **EXT_RES_DET**	R 0x0	External reference resistor detection. Check to see if I_{REF} current through the resistor is provided and the device is operational.
	0: REF_RES_FAULT 1: REF_RES_DET	No resistor detected. Normal operation

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[12] **OUTPUT**	RW 0x1	Output polarity of SDO pin when UART is enabled using pin UART_EN. Its main purpose is to use SDO as NAO next address output signal for chain addressing of multiple ICs. **Attention:** reset value is 1 for use as NAO to next IC in single-wire chain.
	0: NAO_LOW 1: NAO_HI	SDO/NAO is set to low logic level. SDO/NAO is set to high logic level.
[11] **COMP_B1_B2**	R 0x0	COMP_B1_B2 (StallGuard4 comparator B, for IC test)
[10] **COMP_A1_A2**	R 0x0	COMP_A1_A2 (StallGuard4 comparator A, for IC test)
[9] **COMP_B**	R 0x0	COMP_B (chopper comparator B, for IC test)
[8] **COMP_A**	R 0x0	COMP_A (chopper comparator A, for IC test)
[7] **reserved**	R 0x0	
[6] **UART_EN**	R 0x0	1 = UART interface is enabled
	0: LOW 1: HIGH	UART_EN is logic level low UART_EN is logic level high
[5] **ENCN**	R 0x0	N-channel state
	0: LOW 1: HIGH	ENC_N is logic level low ENC_N is logic level high
[4] **DRV_ENN**	R 0x0	Driver disabled/enabled state.
	0: LOW 1: HIGH	DRV_ENN is logic level low DRV_ENN is logic level high
[3] **ENCA**	R 0x0	A-channel state
	0: LOW 1: HIGH	ENCA is logic level low. ENCB is logic level high.
[2] **ENCB**	R 0x0	B-channel state
	0: LOW 1: HIGH	ENCB is logic level low. ENCB is logic level high.
[1] **DIR**	R 0x0	State of pin DIR
	0: LOW 1: HIGH	DIR pin is logic level low. DIR pin is logic level high.
[0] **STEP**	R 0x0	State of pin STEP
	0: LOW 1: HIGH	STEP pin is logic level low. STEP pin is logic level high.

0x07: GCR.DIAG_CONF

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[27] **diag1_overvoltage**	RW 0x0	Maps OV pin to DIAG1
	0: DISABLED 1: ENABLED	Disabled OV enabled on DIAG1
[26] **diag1_ev_n**	RW 0x0	Map N event to DIAG1
	0: DISABLED 1: ENABLED	Disabled N event enabled on DIAG1
[19] **diag1_index**	RW 0x0	Map index signal to DIAG1
	0: DISABLED 1: ENABLED	Disabled Index pulse mapped to DIAG1
[18] **diag1_stall**	RW 0x0	Map StallGuard signal SG to DIAG1
	0: DISABLED 1: ENABLED	Disabled Stall information mapped to DIAG1
[17] **diag1_otpw**	RW 0x0	Map OTPW (overtemperature prewarning) to DIAG1
	0: DISABLED 1: ENABLED	Disabled OTPW enabled on DIAG1
[16] **diag1_error**	RW 0x0	Map driver error condition to DIAG1
	0: DISABLED 1: ENABLED	Disabled Error condition enabled on DIAG1
[11] **diag0_overvoltage**	RW 0x0	Maps OV pin to DIAG0
	0: DISABLED 1: ENABLED	Disabled OV enabled on DIAG0
[10] **diag0_ev_n**	RW 0x0	Map N event to DIAG0
	0: DISABLED 1: ENABLED	Disabled N event enabled on DIAG0
[3] **diag0_index**	RW 0x0	Map index signal to DIAG0
	0: DISABLED 1: ENABLED	Disabled Index pulse mapped to DIAG0
[2] **diag0_stall**	RW 0x0	Map StallGuard signal SG to DIAG0. Will be enabled after reaching TCOOLTHRS.
	0: DISABLED 1: ENABLED	Disabled Stall information mapped to DIAG0
[1] **diag0_otpw**	RW 0x0	Map OTPW (overtemperature pre-warning) to DIAG0
	0: DISABLED 1: ENABLED	Disabled OTPW enabled on DIAG0
[0] **diag0_error**	RW 0x0	Map driver error condition to DIAG0
	0: DISABLED 1: ENABLED	Disabled Error condition enabled on DIAG0

0x0A: GCR.DRV_CONF

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[5:4] **SLOPE_CONTROL**	RW 0x0	Slope Control Setting
	0: SC_100V_US 100V/µs 1: SC_200V_US 200V/µs 2: SC_400V_US 400V/µs 3: SC_800V_US 800V/µs	
[1:0] **CURRENT_RANGE**	RW 0x0	This setting allows a basic adaptation of the drivers RDSon current sensing to the motor current range. Select the lowest fitting range for best current precision. The value is the peak current setting.
	0: CR_1A 1A 1: CR_2A 2A 2: CR_3A 3A 3: CR_3A_RED 3A	

0x0B: GCR.GLOBAL_SCALER

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[7:0] **GLOBALSCALER**	RW, unsigned 0x00	Global scaling of motor current. This value is multiplied to the current scaling to adapt a drive to a certain motor type. This value should be chosen before tuning other settings, because it also influences chopper hysteresis. This value is just intended for finetuning the motor current. 0: Full scale (or write 256) 1 … 31: Not allowed for operation 32 … 255: 32/256 … 255/256 of maximum current. **Hint:** Values >128 recommended for best results.

0x10: VDR.IHOLD_IRUN

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[27:24] **IRUNDELAY**	RW 0x4	Controls the number of clock cycles for motor power-up after start is detected. 0: instant power up 1…15: Delay per current increment step in multiple of IRUNDELAY × 512 clocks.
	0: INSTANT 1: DELAY_512 2: DELAY_1024 3: DELAY_1536 4: DELAY_2048 5: DELAY_2560 6: DELAY_3072 7: DELAY_3584 8: DELAY_4096 9: DELAY_4608 10: DELAY_5120 11: DELAY_5632 12: DELAY_6144 13: DELAY_6656 14: DELAY_7168 15: DELAY_7680	Instant jump to IRUN on start of a motion. Delay of 512 × t_clk per current increment. Delay of 1024 × t_clk per current increment. Delay of 1536 × t_clk per current increment. Delay of 2048 × t_clk per current increment. Delay of 2560 × t_clk per current increment. Delay of 3072 × t_clk per current increment. Delay of 3584 × t_clk per current increment. Delay of 4096 × t_clk per current increment. Delay of 4608 × t_clk per current increment. Delay of 5120 × t_clk per current increment. Delay of 5632 × t_clk per current increment. Delay of 6144 × t_clk per current increment. Delay of 6656 × t_clk per current increment. Delay of 7168 × t_clk per current increment. Delay of 7680 × t_clk per current increment.
[19:16] **IHOLDDELAY**	RW 0x1	Controls the number of clock cycles for motor power down after a motion as soon as standstill is detected (stst =1) and TPOWERDOWN has expired. The smooth transition avoids a motor jerk upon power down. 0: Instant power down 1..15: Delay per current reduction step in multiples of 2^18 clocks
	0: INSTANT 1: DELAY_1_218 2: DELAY_2_218 3: DELAY_3_218 4: DELAY_4_218 5: DELAY_5_218 6: DELAY_6_218 7: DELAY_7_218 8: DELAY_8_218 9: DELAY_9_218 10: DELAY_10_218 11: DELAY_11_218 12: DELAY_12_218 13: DELAY_13_218 14: DELAY_14_218 15: DELAY_15_218	Instant reduction to IHOLD current after TPOWERDOWN has expired. One decrement every 2^18 × t_clk One decrement every 2 × 2^18 × t_clk One decrement every 3 × 2^18 × t_clk One decrement every 4 × 2^18 × t_clk One decrement every 5 × 2^18 × t_clk One decrement every 6 × 2^18 × t_clk One decrement every 7 × 2^18 × t_clk One decrement every 8 × 2^18 × t_clk One decrement every 9 × 2^18 × t_clk One decrement every 10 × 2^18 × t_clk One decrement every 11 × 2^18 × t_clk One decrement every 12 × 2^18 × t_clk One decrement every 13 × 2^18 × t_clk One decrement every 14 × 2^18 × t_clk One decrement every 15 × 2^18 × t_clk
[12:8] **IRUN**	RW, unsigned 0x1F	Motor run current (0 = 1/32…31 = 32/32) **Hint:** Choose sense resistors in a way that normal IRUN is 16 to 31 for best microstep performance.
[4:0] **IHOLD**	RW, unsigned 0x08	Standstill current (0 = 1/32…31 = 32/32) In combination with StealthChop2 mode, setting IHOLD = 0 allows to choose freewheeling or coil short circuit for motor stand still.

0x11: VDR.TPOWERDOWN

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[7:0] **TPOWERDOWN**	RW, unsigned 0x0A	TPOWERDOWN sets the delay time after standstill (stst) of the motor to motor current power down. Time range is about 0 seconds to 4 seconds. **Attention:** A minimum setting of 2 is required to allow the automatic tuning of StealthChop2 PWM_OFFS_AUTO. Reset default = 10 0…((2^8) - 1) × 2^18 t CLK

0x12: VDR.TSTEP

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[19:0] **TSTEP**	R, unsigned 0x00000	Actual measured time between two 1/256 microsteps derived from the step input frequency in units of 1/fCLK. Measured value is (2^20)-1 in case of overflow or standstill. All TSTEP related thresholds use a hysteresis of 1/16 of the compare value to compensate for jitter in the clock or the step frequency. The flag small_hysteresis modifies the hysteresis to a smaller value of 1/32. (Txxx × 15/16) - 1 or (Txxx × 31/32) - 1 is used as a second compare value for each comparison value. This means the lower switching velocity equals the calculated setting, but the upper switching velocity is higher as defined by the hysteresis setting.

0x13: VDR.TPWMTHRS

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[19:0] **TPWMTHRS**	RW, unsigned 0x00000	This is the upper velocity for StealthChop2 voltage PWM mode. TSTEP ≥ TPWMTHRS StealthChop2 PWM mode is enabled, if configured.

0x14: VDR.TCOOLTHRS

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[19:0] **TCOOLTHRS**	RW, unsigned 0x00000	This is the lower threshold velocity for switching on smart energy CoolStep and StallGuard feature. (unsigned) Set this parameter to disable CoolStep at low speeds, where it cannot work reliably. The stall output signal is enabled when exceeding this velocity. It is disabled again once the velocity falls below this threshold. TCOOLTHRS ≥ TSTEP ≥ THIGH : CoolStep is enabled, if configured. TCOOLTHRS ≥ TSTEP Stall output signal (DIAG0/1) is enabled, if configured.

0x15: VDR.THIGH

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[19:0] **THIGH**	RW, unsigned 0x00000	This velocity setting allows velocity-dependent switching into a different chopper mode and fullstepping to maximize torque. (unsigned) The stall detection feature is switched off for 2 to 3 electrical periods whenever passing the THIGH threshold to compensate for the effect of switching modes. TSTEP ≤ THIGH: CoolStep is disabled (motor runs with normal current scale). StealthChop2 voltage PWM mode is disabled. If vhighchm is set, the chopper switches to chm = 1 with TFD = 0 (constant off time with slow decay only). If vhighfs is set, the motor operates in fullstep mode and the stall detection is switched over to fullstep mode stall detection.

0x2D: DMR.DIRECT_MODE

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[24:16] **DIRECT_COIL_B**	RW, signed 0x000	When direct mode in GCONF is selected: Signed coil B current
[8:0] **DIRECT_COIL_A**	RW, signed 0x000	When direct mode in GCONF is selected: Signed coil A current

0x38: ER.ENCMODE

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[10] **enc_sel_decimal**	RW 0x0	Encoder prescaler mode selection
	0: BINARY 1: DECIMAL	Encoder prescaler divisor binary mode: counts ENC_CONST(fractional part)/65536. Encoder prescaler divisor decimal mode: counts in ENC_CONST(fractional part)/10000.
[8] **clr_enc_x**	RW 0x0	Encoder latch configuration
	0: KEEP 1: CLEAR	Upon N event, X_ENC becomes latched to ENC_LATCH only. Latch and additionally clear encoder counter X_ENC at N-event.
[7:6] **pos_neg_edge**	RW 0x0	N channel event sensitivity
	0: HIGH_ACTIVE 1: RISING_EDGE 2: FALLING_EDGE 3: BOTH_EDGES	N channel event is active during an active N event level. N channel is valid upon active going N event. N channel is valid upon inactive going N event. N channel is valid upon active going and inactive going N event.
[5] **clr_once**	RW 0x0	Position latch configuration
	0: OFF 1: LATCH_ONCE	Disabled Latch or latch and clear X_ENC on the next N event following the write access.
[4] **clr_cont**	RW 0x0	Position latch configuration
	0: OFF 1: LATCH_CONT	Disabled Always latch or latch and clear X_ENC upon an N event (once per revolution, it is recommended to combine this setting with edge sensitive N event).
[3] **ignore_AB**	RW 0x0	N event configuration
	0: N_AB_MATCH 1: N_AB_IGNORED	An N event occurs only when polarities given by pol_N, pol_A, and pol_B match. Ignore A and B polarity for N channel event
[2] **pol_N**	RW 0x0	Defines active polarity of N
	0: LOW_ACTIVE 1: HIGH_ACTIVE	Low active High active
[1] **pol_B**	RW 0x0	Required B polarity for an N channel event
	0: NEG 1: POS	Negative polarity Positive polarity
[0] **pol_A**	RW 0x0	Required A polarity for an N channel event
	0: NEG 1: POS	Negative polarity Positive polarity

0x39: ER.X_ENC

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **X_ENC**	RW, signed 0x00000000	Actual encoder position (signed)

0x3A: ER.ENC_CONST

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **ENC_CONST**	RW, signed 0x00010000	Accumulation constant (signed) 16-bit integer part, 16-bit fractional part X_ENC accumulates +/- ENC_CONST / (2^16 × X_ENC) (binary) or +/- ENC_CONST / (10^4 × X_ENC) (decimal) ENCMODE bit enc_sel_decimal switches between decimal and binary setting. Use the sign to match rotation direction! Binary: ± [µsteps/2^16] ±(0 … 32767.999847) Decimal: ±(0.0 … 32767.9999) Reset default = 1.0 (= 65536)

0x3B: ER.ENC_STATUS

Encoder status information

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[0] **n_event**	RW, W1C 0x0	An N event is detected since last clearing this bit. #type=COW
	0: NO_EVENT 1: EVENT_DETECTED	No event Event detected. To clear the status bit, write with a 1-bit at the corresponding position.

0x3C: ER.ENC_LATCH

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **ENC_LATCH**	R, unsigned 0x00000000	Encoder position X_ENC latched on N event.

0x50: ADC_Registers.ADC_VSUPPLY_AIN

BITS AND NAME	TYPE AD RESET	DESCRIPTION
[28:16] **ADC_AIN**	R, signed 0x0000	Value of voltage at AIN pin in integer. Update rate: each 2048 clocks
[12:0] **ADC_VSUPPLY**	R, signed 0x0000	Actual value of voltage on V_S (filtered with low pass filter). Update rate: each 2048 clocks

0x51: ADC_Registers.ADC_TEMP

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[28:16] **RESERVED**	R, unsigned 0x0000	
[12:0] **ADC_TEMP**	R, signed 0x0000	Actual temperature (filtered with low pass filter) Udate rate: each 2048 clocks

0x52: ADC_Registers.OTW_OV_VTH

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[28:16] **OVERTEMPPREWARNING_VTH**	RW, unsigned 0x0B92	Overtemperature warning threshold register: ADC_TEMP >= OVERTEMPPREWARNING_VTH Overtemperatureprewarning is triggered. (Reset: 0xB92 equals 120°C).
[12:0] **OVERVOLTAGE_VTH**	RW, unsigned 0x0F25	Overvoltage threshold for output OV. Default: 38V, 36 V equals 1.125 V at ADC inputs.

0x60: MDR.MSLUT_0

Microstep table entries 0…31

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_0**	RW, unsigned 0xAAAAB554	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x61: MDR.MSLUT_1

Microstep table entries 32…63

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_1**	RW, unsigned 0x4A9554AA	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x62: MDR.MSLUT_2

Microstep table entries 64…95

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_2**	RW, unsigned 0x24492929	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x63: MDR.MSLUT_3

Microstep table entries 96…127

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_3**	RW, unsigned 0x10104222	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x64: MDR.MSLUT_4

Microstep table entries 128…159

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_4**	RW, unsigned 0xFBFFFFFF	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x65: MDR.MSLUT_5

Microstep table entries 160…191

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_5**	RW, unsigned 0xB5BB777D	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x66: MDR.MSLUT_6

Microstep table entries 192…223

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_6**	RW, unsigned 0x49295556	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x67: MDR.MSLUT_7

Microstep table entries 224…255

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:0] **MSLUT_7**	RW, unsigned 0x00404222	Each bit gives the difference between entry x and entry x + 1 when combined with the corresponding MSLUTSEL W bits: 0: W = %00: -1 %01: +0 %10: +1 %11: +2 1: W = %00: +0 %01: +1 %10: +2 %11: +3 This is the differential coding for the first quarter of a wave. Start values for CUR_A and CUR_B are stored for MSCNT position 0 in START_SIN and START_SIN90. ofs31, ofs30, …, ofs01, ofs00 … ofs255, ofs254, …, ofs225, ofs224 Reset default = sine wave table

0x68: MDR.MSLUTSEL

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:24] **X3**	RW, unsigned 0xFF	LUT segment 1 start. The sine wave lookup table can be divided into up to four segments using an individual step width control entry Wx. The segment borders are selected by X1, X2, and X3. Segment 0 goes from 0 to X1 -1. Segment 1 goes from X1 to X2 -1. Segment 2 goes from X2 to X3 -1. Segment 3 goes from X3 to 255. For defined response, the values shall satisfy: 0< X1 < X2 < X3
[23:16] **X2**	RW, unsigned 0xFF	LUT segment 1 start. The sine wave look up table can be divided into up to four segments using an individual step width control entry Wx. The segment borders are selected by X1, X2, and X3. Segment 0 goes from 0 to X1 -1. Segment 1 goes from X1 to X2 -1. Segment 2 goes from X2 to X3 -1. Segment 3 goes from X3 to 255. For defined response, the values shall satisfy: 0< X1 < X2 < X3
[15:8] **X1**	RW, unsigned 0x80	LUT segment 1 start. The sine wave look up table can be divided into up to four segments using an individual step width control entry Wx. The segment borders are selected by X1, X2, and X3. Segment 0 goes from 0 to X1 -1. Segment 1 goes from X1 to X2 -1. Segment 2 goes from X2 to X3 -1. Segment 3 goes from X3 to 255. For defined response, the values shall satisfy: 0< X1 < X2 < X3
[7:6] **W3**	RW 0x1	LUT width select from ofs(X3) to ofs255. Width control bit coding W0 … W3: %00: MSLUT entry 0, 1 select: -1, +0 %01: MSLUT entry 0, 1 select: +0, +1 %10: MSLUT entry 0, 1 select: +1, +2 %11: MSLUT entry 0, 1 select: +2, +3
	0: W3_SUB1_ADD0 Current MSLUT entry 0 (1): -1 (+0) to sinewave. 1: W3_ADD0_ADD1 Current MSLUT entry 0 (1): +0 (+1) to sinewave. 2: W3_ADD1_ADD2 Current MSLUT entry 0 (1): +1 (+2) to sinewave. 3: W3_ADD2_ADD3 Current MSLUT entry 0 (1): +2 (+3) to sinewave.	

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[5:4] **W2**	RW 0x1	LUT width select from ofs(X2) to ofs(X3-1). Width control bit coding W0 … W3: %00: MSLUT entry 0, 1 select: -1, +0 %01: MSLUT entry 0, 1 select: +0, +1 %10: MSLUT entry 0, 1 select: +1, +2 %11: MSLUT entry 0, 1 select: +2, +3
	0: W2_SUB1_ADD0 1: W2_ADD0_ADD1 2: W2_ADD1_ADD2 3: W2_ADD2_ADD3	Current MSLUT entry 0 (1): -1 (+0) to sinewave. Current MSLUT entry 0 (1): +0 (+1) to sinewave. Current MSLUT entry 0 (1): +1 (+2) to sinewave. Current MSLUT entry 0 (1): +2 (+3) to sinewave.
[3:2] **W1**	RW 0x1	LUT width select from ofs(X1) to ofs(X2-1). Width control bit coding W0 … W3: %00: MSLUT entry 0, 1 select: -1, +0 %01: MSLUT entry 0, 1 select: +0, +1 %10: MSLUT entry 0, 1 select: +1, +2 %11: MSLUT entry 0, 1 select: +2, +3
	0: W1_SUB1_ADD0 1: W1_ADD0_ADD1 2: W1_ADD1_ADD2 3: W1_ADD2_ADD3	Current MSLUT entry 0 (1): -1 (+0) to sinewave. Current MSLUT entry 0 (1): +0 (+1) to sinewave. Current MSLUT entry 0 (1): +1 (+2) to sinewave. Current MSLUT entry 0 (1): +2 (+3) to sinewave.
[1:0] **W0**	RW 0x2	LUT width select from ofs00 to ofs(X1-1) Width control bit coding W0 … W3: %00: MSLUT entry 0, 1 select: -1, +0 %01: MSLUT entry 0, 1 select: +0, +1 %10: MSLUT entry 0, 1 select: +1, +2 %11: MSLUT entry 0, 1 select: +2, +3
	0: W0_SUB1_ADD0 1: W0_ADD0_ADD1 2: W0_ADD1_ADD2 3: W0_ADD2_ADD3	Current MSLUT entry 0 (1): -1 (+0) to sinewave. Current MSLUT entry 0 (1): +0 (+1) to sinewave. Current MSLUT entry 0 (1): +1 (+2) to sinewave. Current MSLUT entry 0 (1): +2 (+3) to sinewave.

0x69: MDR.MSLUTSTART

Start values are transferred to the microstep registers CUR_A and CUR_B whenever the reference position MSCNT = 0 is passed.

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:24] **OFFSET_SIN90**	RW, unsigned 0x00	Signed offset for cosine wave ±127 microsteps. Adapt START_SIN90 to match the microstep wave table at position MSCNT = 0.
[23:16] **START_SIN90**	RW, unsigned 0xF7	START_SIN90 gives the absolute value for cosine wave microstep table entry at MSCNT = 0 (table position 256 + OFFSET_SIN90).
[7:0] **START_SIN**	RW, unsigned 0x00	START_SIN gives the absolute value at microstep table entry 0.

0x6A: MDR.MSCNT

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[9:0] **MSCNT**	R, unsigned 0x000	Microstep counter. Indicates actual position in the microstep table for CUR_B. CUR_A uses an offset of 256 (two-phase motor). **Hint:** Move to a position where MSCNT is zero before reinitializing MSLUTSTART or MSLUT and MSLUTSEL.

0x6B: MDR.MSCURACT

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[24:16] **CUR_A**	R, signed 0x0F7	Actual microstep current for motor phase A (cosine wave) as read from MSLUT (not scaled by current).
[8:0] **CUR_B**	R, signed 0x000	Actual microstep current for motor phase B (sine wave) as read from MSLUT (not scaled by current).

0x6C: MDR.CHOPCONF

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31] **diss2vs**	RW 0x0	Short-to-supply protection disable
	0: 0 1: 1	Short to VS protection is on. Short to VS protection is disabled.
[30] **diss2g**	RW 0x0	Short-to-GND protection disable
	0: 0 1: 1	Short-to-GND protection is on. Short-to-GND protection is disabled.
[29] **dedge**	RW 0x0	Enable double edge step pulses
	0: 0 1: 1	Disabled Enable step impulse at each step edge to reduce step frequency requirement.
[28] **intpol**	RW 0x1	The actual microstep resolution (MRES) is extrapolated to 256 microsteps for smoothest motor operation.
	0: DISABLED 1: ENABLED	No interpolation Interpolates to 256 microsteps

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[27:24] **MRES**	RW 0x0	Microstep resolution selection. %0000: Native 256 microstep setting. Normally, use this setting with the internal motion controller. %0001 … %1000: 128, 64, 32, 16, 8, 4, 2, FULLSTEP Reduced microstep resolution. The resolution gives the number of microstep entries per sine quarter wave. The driver automatically uses microstep positions, which result in a symmetrical wave, when choosing a lower microstep resolution. Step width = 2^(MRES) [microsteps]
	0: RES_256 — 256 steps per fullstep 1: RES_128 — 128 steps per fullstep 2: RES_64 — 64 steps per fullstep 3: RES_32 — 32 steps per fullstep 4: RES_16 — 16 steps per fullstep 5: RES_8 — 8 steps per fullstep 6: RES_4 — 4 steps per fullstep 7: RES_HS — 2 steps per fullstep 8: RES_FS — Fullstep	
[23:20] **TPFD**	RW, unsigned 0x4	Passive fast decay time TPFD allows dampening of motor mid-range resonances. Passive fast decay time setting controls duration of the fast decay phase inserted after bridge polarity change NCLK = 128 × TPFD %0000: Disable %0001 … %1111: 1 … 15
[19] **vhighchm**	RW 0x0	High velocity chopper mode This bit enables switching to chm = 1 and fd = 0 when VHIGH is exceeded. This way, a higher velocity can be achieved. Can be combined with vhighfs = 1. If set, the TOFF setting automatically is doubled during a high velocity operation to avoid doubling of the chopper frequency.
	0: CTOFF_THIGH_DIS — Disabled 1: CTOFF_THIGH_EN — Switch to constant TOFF chopper when reaching THIGH.	
[18] **vhighfs**	RW 0x0	High velocity fullstep selection This bit enables switching to fullstep when VHIGH is exceeded. Switching takes place only at 45° position. The fullstep target current uses the current value from the microstep table at the 45° position.
	0: FS_THIGH_DIS — Disabled 1: FS_THIGH_EN — Switches from microstep to fullstep on reaching THIGH.	

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[16:15] **TBL**	RW 0x2	TBL blank time setting. Sets comparator blank time in numbers of clock cycles. **Hint:** 24 or 36 clocks are recommended for most applications. Restriction for TBL = 0x0 : Use only in combination with external clock oscillator <= 8MHz. Restriction for TBL = 0x1 : May be used with internal clock, or if external clock frequency <= 13MHz is applied.
	0: TBL_16 1: TBL_24 2: TBL_36 3: TBL_48	16 clocks 24 clocks 36 clocks 48 clocks
[14] **chm**	RW 0x0	Chopper mode selection. This is only effective if en_pwm_mode is set to 0 or TSTEP < TPWMTHRS.
	0: SPREADCYCLE 1: CLASSIC_CHOP	Standard mode (SpreadCycle) Constant off time with fast decay time. Fast decay time is also terminated when the negative nominal current is reached. Fast decay is after on time.
[12] **disfdcc**	RW 0x0	Fast decay mode for chm = 1
	0: DISABLED 1: ENABLED	Enables current comparator usage for termination of the fast decay cycle. Disables current comparator usage for termination of the fast decay cycle.
[11] **fd3**	RW 0x0	TFD[3] With chm = 1: MSB of fast decay time setting TFD
	0: TFD3_0 1: TFD3_1	MSB of TFD setting: 0 MSB of TFD setting: 1
[10:7] **HEND_OFFSET**	RW, unsigned 0x2	With chm =0: HEND hysteresis low value %0000 … %1111: Hysteresis is -3, -2, -1, 0, 1, …, 12. (1/512 of this setting adds to current setting). This is the hysteresis value used for the hysteresis chopper. Wwith chm =1: OFFSET sine wave offset %0000 … %1111: Offset is -3, -2, -1, 0, 1, …, 12. This is the sine wave offset and 1/512 of the value is added to the absolute value of each sine wave entry.

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[6:4] **HSTRT_TFD210**	RW, unsigned 0x5	With chm =0: HSTRT hysteresis start value added to HEND. %000 … %111: Add 1, 2, …, 8 to hysteresis low value HEND. (1/512 of this setting adds to current setting). **Attention:** Effective HEND + HSTRT ≤ 16. **Hint:** Hysteresis decrement is done each 16 clocks. With chm =1: TFD [2..0] fast decay time setting. Fast decay time setting (MSB: fd3): %0000 … %1111: Fast decay time setting TFD with NCLK = 32 × TFD (%0000: slow decay only)
[3:0] **TOFF**	RW 0x0	TOFF off time and driver enable Off time setting controls duration of slow decay phase NCLK = 24 + 32 × TOFF %0000: Driver disable, all bridges off %0001: 1 – use only with TBL ≥ 2 %0010 … %1111: 2 … 15
	0: DRIVER_OFF 1: TOFF_56 2: TOFF_88 3: TOFF_120 4: TOFF_152 5: TOFF_184 6: TOFF_216 7: TOFF_248 8: TOFF_280 9: TOFF_312 10: TOFF_344 11: TOFF_376 12: TOFF_408 13: TOFF_440 14: TOFF_472 15: TOFF_504	Driver disabled and all bridges off. Slow decay phase duration: 56 × t_clk. Use with TBL >= 2. Slow decay phase duration: 88 × tclk. Slow decay phase duration: 120 × tclk. Slow decay phase duration: 152 × tclk. Slow decay phase duration: 184 × tclk. Slow decay phase duration: 216 × tclk. Slow decay phase duration: 248 × tclk. Slow decay phase duration: 280 × tclk. Slow decay phase duration: 312 × tclk. Slow decay phase duration: 344× tclk. Slow decay phase duration: 376 × tclk. Slow decay phase duration: 408 × tclk. Slow decay phase duration: 440 × tclk. Slow decay phase duration: 472 × tclk. Slow decay phase duration: 504 × tclk.

0x6D: MDR.COOLCONF

BITS AND NAME	TYPE NAD RESET	DESCRIPTION
[24] **sfilt**	RW 0x0	StallGuard2 filter enable
	0: FILT_DISABLED 1: FILT_ENABLED	Standard mode, high time resolution for StallGuard. Filtered mode, StallGuard signal updated for each four fullsteps only to compensate for motor pole tolerances.

BITS AND NAME	TYPE NAD RESET	DESCRIPTION
[22:16] **sgt**	RW, unsigned 0x00	StallGuard2 threshold value This signed value controls StallGuard2 level for stall output and sets the optimum measurement range for readout. A lower value gives a higher sensitivity. Zero is the starting value working with most motors. -64 to +63: A higher value makes StallGuard2 less sensitive and requires more torque to indicate a stall.
[15] **seimin**	RW 0x0	Minimum current for smart current control
	0: IRUN_DIV2 1: IRUN_DIV4	1/2 of current setting (IRUN) (when used with StealthChop requires IRUN ≥ 16). 1/4 of current setting (IRUN) (when used with StealthChop requires IRUN ≥ 28).
[14:13] **sedn**	RW 0x0	Current down step speed %00: For each 32 StallGuard2 values, decrease by one. %01: For each 8 StallGuard2 values, decrease by one. %10: For each 2 StallGuard2 values, decrease by one. %11: For each StallGuard2 value, decrease by one.
	0: STEP_DOWN_EACH_32 1: STEP_DOWN_EACH_8 2: STEP_DOWN_EACH_2 3: STEP_DOWN_EACH_1	For each 32 StallGuard2/StallGuard4 values, decrease by one. For each 8 StallGuard2/StallGuard4 values, decrease by one. For each 2 StallGuard2/StallGuard4 values, decrease by one. For each StallGuard2/StallGuard4 values, decrease by one.
[11:8] **semax**	RW, unsigned 0x0	StallGuard2 hysteresis value for smart current control If the StallGuard2 result is equal to or above (SEMIN + SEMAX + 1) × 32, the motor current is decreased to save energy. %0000 … %1111: 0 … 15
[6:5] **seup**	RW 0x0	Current up step width Current increment steps per measured StallGuard2 value.
	0: STEP_UP_1 1: STEP_UP_2 2: STEP_UP_4 3: STEP_UP_8	1 increment per Stallguard2/4 value. 2 increments per Stallguard2/4 value. 4 increments per Stallguard2/4 value. 8 increments per Stallguard2/4 value.
[3:0] **semin**	RW, unsigned 0x0	Minimum StallGuard2 value for smart current control and smart current enable. If the StallGuard2 result falls below SEMIN × 32, the motor current is increased to reduce motor load angle. %0000: smart current control CoolStep off %0001 … %1111: 1 … 15

0x6F: MDR.DRV_STATUS

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31] **stst**	R 0x0	Standstill indicator This flag indicates motor standstill in each operation mode. This occurs 2^(20) clocks after the last step pulse.
	0: INACTIVE 1: ACTIVE	Motor moving Motor in standstill
[30] **olb**	R 0x0	Open load indicator phase B. **Hint:** This is just an informative flag. The driver takes no action upon it. False detection may occur in fast motion and standstill. Check during slow motion only.
	0: OPERATIONAL 1: OPEN_LOAD	Normal operation Open load detected on phase B.
[29] **ola**	R 0x0	Open load indicator phase A
	0: OPERATIONAL 1: OPEN_LOAD	Normal operation Open load detected on phase A. **Hint:** This is just an informative flag. The driver takes no action upon it. False detection may occur in fast motion and standstill. Check during slow motion only.
[28] **s2gb**	R 0x0	Short-to-ground indicator phase B
	0: OPERATIONAL 1: ERROR	Normal operation Short-to-GND detected on phase B. The driver is disabled. The flags stay active until the driver is disabled by software (TOFF = 0) or by the ENN input.
[27] **s2ga**	R 0x0	Short-to-ground indicator phase A
	0: OPERATIONAL 1: ERROR	Normal operation Short-to-GND detected on phase A. The driver is disabled. The flags stay active until the driver is disabled by software (TOFF = 0) or by the ENN input.
[26] **otpw**	R 0x0	Overtemperature prewarning flag
	0: INACTIVE 1: ACTIVE	Normal operation Overtemperature prewarning threshold is exceeded. The overtemperature prewarning flag is common for both bridges.
[25] **ot**	R 0x0	Overtemperature flag
	0: OPERATIONAL 1: ERROR	Normal operation Overtemperature limit is reached. Drivers are disabled until the IC has cooled down. The overtemperature flag is common for both bridges.
[24] **stallguard**	R 0x0	StallGuard2/StallGuard4 status
	0: INACTIVE 1: ACTIVE	Normal operation Motor stall detected by StallGuard2 (in SpreadCycle operation), respectively, by StallGuard4 (in StealthChop2 operatoin) or DcStep stall (in DcStep mode).

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[20:16] **CS_ACTUAL**	R, unsigned 0x00	Actual motor current/smart energy current Actual current control scaling for monitoring smart energy current scaling controlled through settings in register COOLCONF or for monitoring the function of the automatic current scaling.
[15] **fsactive**	R 0x0	Full step active indicator
	0: USTEP 1: FSTEP	Microstepping active Indicates the driver has switched to fullstep, as defined by chopper mode settings and velocity thresholds.
[14] **stealth**	R 0x0	StealthChop2 indicator
	0: SPREADCYCLE_CTOFF 1: STEALTHCHOP	StealthChop2 not active. Driver operates in StealthChop2 mode.
[13] **s2vsb**	R 0x0	Short-to-supply indicator phase B. The driver is disabled. The flags stay active until the driver is disabled by software (TOFF = 0) or by the DRV_ENN input.
	0: OPERATIONAL 1: ERROR	No error Short-to-supply detected on phase B.The driver is disabled.
[12] **s2vsa**	R 0x0	Short-to-supply indicator phase A. The driver is disabled. The flags stay active until the driver is disabled by software (TOFF = 0) or by the DRV_ENN input.
	0: OPERATIONAL 1: ERROR	No error Short-to-supply detected on phase A. The driver is disabled.
[9:0] **SG_RESULT**	R, unsigned 0x000	StallGuard2 result, respectively, StallGuard4 result (depending on actual chopper mode), respectively, PWM on time for coil A in standstill with SpreadCycle for motor temperature detection. Mechanical load measurement: The StallGuard2/4 result gives a means to measure mechanical motor load. A higher value means lower mechanical load. For StallGuard2, a value of 0 signals highest load. With optimum SGT setting, this is an indicator for a motor stall. The stall detection compares SG_RESULT to 0 to detect a stall. SG_RESULT is used as a base for CoolStep operation by comparing it to a programmable upper and a lower limit. It is not applicable in StealthChop2 mode. StallGuard2 works best with microstep operation. Temperature measurement during SpreadCycle mode: In standstill, no StallGuard2 result can be obtained. SG_RESULT shows the chopper on-time for motor coil A instead. Move the motor to a determined microstep position at a certain current setting to get an estimation of motor temperature by reading the chopper on-time. As the motor heats up, its coil resistance rises and the chopper on-time increases. For StallGuard4 specifics, see SG4_RESULT.

0x70: MDR.PWMCONF

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:28] **PWM_LIM**	RW, unsigned 0xC	PWM automatic scale amplitude limit when switching on. Limit for PWM_SCALE_AUTO when switching back from SpreadCycle to StealthChop2. This value defines the upper limit for bits 7 to 4 of the automatic current control when switching back. It can be set to reduce the current jerk during mode change back to StealthChop2. It does not limit PWM_GRAD or PWM_GRAD_AUTO offset. (Default = 12)
[27:24] **PWM_REG**	RW, unsigned 0x4	Regulation loop gradient User-defined maximum PWM amplitude change per half wave when using pwm_autoscale =1. (1…15): 1: 0.5 increments (slowest regulation) 2: 1 increment 3: 1.5 increments 4: 2 increments (reset default)) … 8: 4 increments ... 15: 7.5 increments (fastest regulation)
[23] **pwm_dis_reg_stst**	RW 0x0	1= Disable current regulation when motor is in standstill and current is reduced (less than IRUN). This option eliminates any regulation noise during standstill.
	0: CTRL_ACTIVE 1: CTRL_INACTIVE	Current regulation active Disable current regulation when motor is in standstill and current is reduced (less than IRUN). This option eliminates any regulation noise during standstill.
[22] **pwm_meas_sd_enable**	RW 0x0	Slow decay phase low side current measurement control.
	0: DISABLED 1: ENABLED	Slow decay low side measurement disabled. Uses slow decay phases on low side to measure the motor current to reduce the lower current limit.
[21:20] **FREEWHEEL**	RW 0x0	Allows different standstill modes. Standstill option when motor current setting is zero (I_HOLD =0).
	0: NORMAL 1: FREEWHEEL 2: LS_SHORT 3: HS_SHORT	Normal operation Freewheeling Coil shorted using LS drivers Coil shorted using HS drivers

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[19] **pwm_autograd**	RW 0x1	PWM automatic gradient adaptation
	0: FIXED	Fixed value for PWM_GRAD (PWM_GRAD_AUTO = PWM_GRAD).
	1: AUTO	Automatic tuning (only with pwm_autoscale=1) (reset default) PWM_GRAD_AUTO is initialized with PWM_GRAD while pwm_autograd = 0 and is optimized automatically during motion. Preconditions PWM_OFS_AUTO is automatically initialized. This requires standstill at IRUN for >130ms to a) detect standstill b) wait > 128 chopper cycles at IRUN, and c) regulate PWM_OFS_AUTO so that -1 PWM_SCALE_AUTO motor running and 1.5 × PWM_OFS_AUTO × (IRUN+1)/32 PWM_SCALE_SUM PWM_OFS_AUTO × (IRUN+1)/32and PWM_SCALE_SUM Time required for tuning PWM_GRAD_AUTO is about 8 fullsteps per change of ±1. Also enables use of reduced chopper frequency for tuning PWM_OFS_AUTO.
[18] **pwm_autoscale**	RW 0x1	PWM automatic amplitude scaling
	0: USER	User-defined feed-forward PWM amplitude. The current settings IRUN and IHOLD have no influence! The resulting PWM amplitude (limited to 0…255) is: PWM_OFS × ((CS_ACTUAL+1)/32) + PWM_GRAD × 256/TSTEP.
	1: AUTO	Enable automatic current control (reset default)
[17:16] **PWM_FREQ**	RW 0x0	PWM frequency selection.
	0: FCLK_2DIV1024	fPWM = 2/1024 fCLK
	1: FCLK_2DIV683	fPWM = 2/683 fCLK
	2: FCLK_2DIV512	fPWM = 2/512 fCLK
	3: FCLK_2DIV410	fPWM = 2/410 fCLK
[15:8] **PWM_GRAD**	RW, unsigned 0x00	Velocity-dependent gradient for PWM amplitude: PWM_GRAD × 256/TSTEP This value is added to PWM_OFS to compensate for the velocity-dependent motor back-EMF. Use PWM_GRAD as initial value for automatic scaling to speed up the automatic tuning process. To do this, set PWM_GRAD to the determined, application-specific value, with pwm_autoscale = 0. Only afterwards, set pwm_autoscale =1. Enable StealthChop2 when finished. **Hint:** After initial tuning, the required initial value can be read out from PWM_GRAD_AUTO.

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[7:0] **PWM_OFS**	RW, unsigned 0x1D	User-defined PWM amplitude offset (0 to 255) related to full motor current (CS_ACTUAL =31) in standstill. (Reset default = 30) Use PWM_OFS as initial value for automatic scaling to speed up the automatic tuning process. To do this, set PWM_OFS to the determined, application-specific value, with pwm_autoscale = 0. Only afterwards, set pwm_autoscale =1. Enable StealthChop2, when finished. PWM_OFS = 0 disables scaling down the motor current below a motor-specific lower measurement threshold. This setting should only be used under certain conditions, that is, when the power supply voltage can vary up and down by a factor of two or more. It prevents the motor going out of regulation, but it also prevents power down below the regulation limit. PWM_OFS > 0 allows automatic scaling to low PWM duty cycles even below the lower regulation threshold. This allows low (standstill) current settings based on the actual (hold) current scale (register IHOLD_IRUN).

0x71: MDR.PWM_SCALE

Results of StealthChop2 amplitude regulator. These values can be used to monitor automatic PWM amplitude scaling (255 = max. voltage).

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[24:16] **PWM_SCALE_AUTO**	R, unsigned 0x000	
[9:0] **PWM_SCALE_SUM**	R, unsigned 0x000	Bits: 9...0: [0...1023]PWM_SCALE_SUM: actual PWM duty cycle. This value is used for scaling the values CUR_A and CUR_B read from the sine wave table. 1023: maximum duty cycle. This value is extended by two bits [1,0] for higher precision of duty cycle read out. Bits 9..2 correspond to the 8-bit values in other PWM duty cycle related registers.

0x72: MDR.PWM_AUTO

These automatically generated values can be read out to determine a default/power-up setting for PWM_GRAD and PWM_OFS.

BITS AD NAME	TYPE AND RESET	DESCRIPTION
[23:16] **PWM_GRAD_AUTO**	R, unsigned 0x00	Automatically determined gradient value
[7:0] **PWM_OFS_AUTO**	R, unsigned 0x00	Automatically determined offset value

0x74: MDR.SG4_THRS

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[10] **sg4_thrs_shl**	RW 0x0	1: SG4_THRS value is multiplied by two internally.
[9] **sg_angle_offset**	RW 0x1	1: Automatic phase shift compensation based on StallGuard4, when switching from StealthChop2 to SpreadCycle controlled using TPWMTHRS.
	0: DISABLE 1: ENABLE	No compensation for phaseshift. Compensates phaseshift (preferred)
[8] **sg4_filt_en**	RW 0x0	Enables the SG4 filter. 1: SG4_RESULT is the average of SG4_IND_0,_1,_2,_3 0: SG4_RESULT uses only SG4_IND_0
	0: FILT_DISABLE 1: FILT_ENABLE	Disable SG4 filter Enable SG4 filter
[7:0] **SG4_THRS**	RW, unsigned 0x00	Detection threshold for stall. The StallGuard4 value SG4_RESULT is compared to this threshold. A stall is signaled with: SG4_RESULT ≤ SG4_THRS SG4_THRS covers half of the possible SG4_RESULT range.

0x75: MDR.SG4_RESULT

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[9:0] **SG4_RESULT**	R, unsigned 0x000	StallGuard result for StallGuard4, only. SG4_RESULT is updated with each fullstep, independent of TCOOLTHRS and SG4THRS. A higher value signals a lower motor load and more torque headroom. Intended for StealthChop2 mode only. Bits 9 and 0 always show 0. Scaling to 10-bit is for compatibility to StallGuard2.

0x76: MDR.SG4_IND

BITS AND NAME	TYPE AND RESET	DESCRIPTION
[31:24] **SG4_IND_3**	R, unsigned 0x00	When SG4_filt_en = 1: Displays SG4 measurement 3 used as filter input.
[23:16] **SG4_IND_2**	R, unsigned 0x00	When SG4_filt_en = 1: Displays SG4 measurement 2 used as filter input.
[15:8] **SG4_IND_1**	R, unsigned 0x00	When SG4_filt_en = 1: Displays SG4 measurement 1 used as filter input.
[7:0] **SG4_IND_0**	R, unsigned 0x00	Displays SG4 measurement When SG4_filt_en = 1: Displays SG4 measurement 0 used as filter input.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
TMC2241ATU+	-40°C to +125°C	38 TQFN - 5mm x 7mm
TMC2241ATU+T	-40°C to +125°C	38 TQFN - 5mm x 7mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/25	Initial release	—