

DESCRIPTION

The RH[®]119 dual comparator features low input offset voltage and offset current, high voltage gain, guaranteed common mode rejection and input protection diodes.

The RH119 is capable of operation over a supply range from 5V to ±15V and can drive 25mA loads from each open collector output. A separate GND pin allows the RH119 to isolate system grounds.

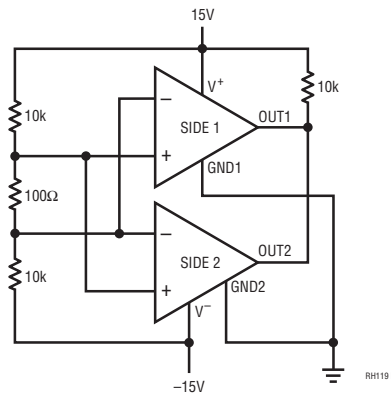
The wafer lots are processed to Analog Devices' in-house Class S flow to yield circuits usable in stringent military applications.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Differential Input Current	±5mA
Input Voltage (See Note 1)	
Output Short-Circuit Duration	10 sec
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec).....	300°C

BURN-IN CIRCUIT



PACKAGE/ORDER INFORMATION

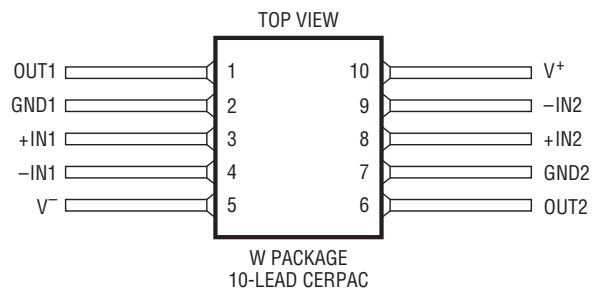
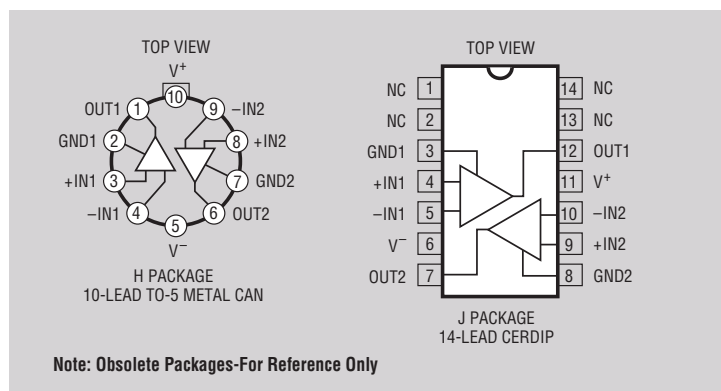


TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 2)

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ\text{C}$			SUB-GROUP	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$V_S = \pm 15\text{V}, V_{CM} = 0\text{V}$	3			4	1			7	2, 3	mV mV
CMRR	Common Mode Rejection Ratio			90			1					dB
I_{OS}	Input Offset Current		3			75	1			100	2, 3	nA
I_B	Input Bias Current					500	1			1000	2, 3	nA
A_V	Voltage Gain			10			4					V/mV
t_R	Response Time		4	80	200		4			200	5, 6	ns
V_{SAT}	Saturation Voltage	$V_{IN} \leq -5\text{mV}, I_O = 25\text{mA}$				1.5	1					V
		$V^+ \geq 4.5\text{V}, V^- = 0\text{V}$ $V_{IN} \leq 6\text{mV}, I_{SINK} \leq 3.2\text{mA}$ $T_A \geq 0^\circ\text{C}$ $T_A \leq 0^\circ\text{C}$				0.4	1			0.4 0.6	2 3	V V
	Output Leakage Current	$V_{IN} \geq 5\text{mV}, V_{OUT} \text{ to } V^- = 35\text{V}$				2	1			10	2, 3	μA
	Input Voltage Range	$V_S = \pm 15\text{V}$ $V^+ = 5\text{V}, V^- = 0\text{V}$		-12 1		12 3	1 1			12 3	2, 3 2, 3	V V
	Differential Input Voltage					± 5	1			± 5	2, 3	V
I_S	Supply Current	$V^+ = 5\text{V}, V^- = 0\text{V}$				4.3						mA
	Positive Supply Current	$V_S = \pm 15\text{V}$				11.5	1					mA
	Negative Supply Current	$V_S = \pm 15\text{V}$				4.5	1					mA

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 5 and Note 6)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si)		20Krad(Si)		50Krad(Si)		100Krad(Si)		200Krad(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Offset Voltage			4		4		4		4		8		mV
I_{OS}	Input Offset Current		3	75		100		150		300		500		nA
I_B	Input Bias Current		3	500		750		1000		1500		2000		nA
A_{VOL}	Large-Signal Voltage Gain			10		10		10		10		5		V/mV
V_{SAT}	Saturation Voltage	$V_{IN} \leq -5\text{mV}, I_O = 25\text{mA}$		1.5		1.5		1.5		1.5		1.5		V
		$V^+ \geq 4.5\text{V}, V^- = 0\text{V}$ $V_{IN} \leq -6\text{mV}, I_{SINK} \leq 3.2\text{mA}$		0.4		0.4		0.4		0.4		0.4		V
CMRR	Common Mode Rejection Ratio			90		90		90		90		90		dB
I_S	Positive Supply Current	$V_S = \pm 15\text{V}$		11.5		11.5		11.5		11.5		11.5		mA
	Negative Supply Current	$V_S = \pm 15\text{V}$		4.5		4.5		4.5		4.5		4.5		mA
	Output Leakage Current	$V_{IN} \geq 5\text{mV}, V_{OUT} \text{ to } V^- = 35\text{V}$		2		2		2		2		2		μA

ELECTRICAL CHARACTERISTICS (Continued)

Note 1: For supply voltages less than $\pm 15\text{V}$, the maximum input voltage is equal to the supply voltage.

Note 2: Unless otherwise noted, supply voltage equals $\pm 15\text{V}$, $V_{\text{CM}} = 0\text{V}$ and $T_{\text{A}} = 25^{\circ}\text{C}$. The GND pin is grounded. Note that the maximum voltage allowed between the GND pin and V^{+} is 18V . Do not tie the GND pin to V^{-} when the power supply voltage exceeds $\pm 9\text{V}$. The offset voltage, offset current and bias current specifications apply for all supply voltages between $\pm 15\text{V}$ and 5V unless otherwise specified.

Note 3: The offset voltages and currents given are the maximum values required to drive the output within 1V of either supply with a 1mA load—thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 4: Response time specified for a 100mV input step with 5mV overdrive.

Note 5: $V_{\text{S}} = \pm 15\text{V}$, $V_{\text{CM}} = 0\text{V}$, $T_{\text{A}} = 25^{\circ}\text{C}$ unless otherwise noted.

Note 6: Device is characterized at 10KRAD , 20KRAD , 50KRAD , 100KRAD , and 200KRAD and is production tested at 100KRAD only.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-PRF-38535 TEST REQUIREMENTS	SUBGROUP
Final electrical parameters	1*, 2, 3, 4, 5, 6
Group A test requirements	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters	1, 2, 3
Group D end-point electrical parameters	1, 2, 3
Group E end-point electrical parameters	1

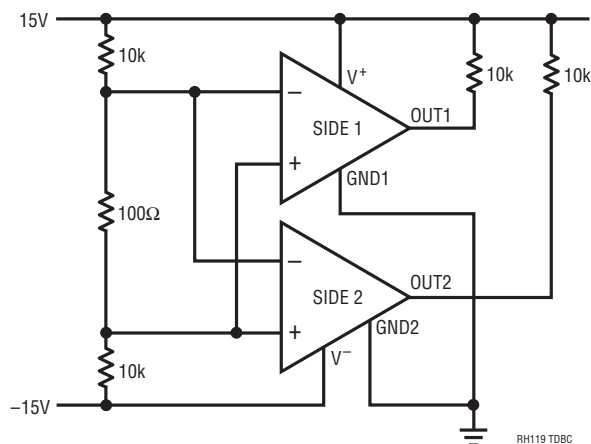
*PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

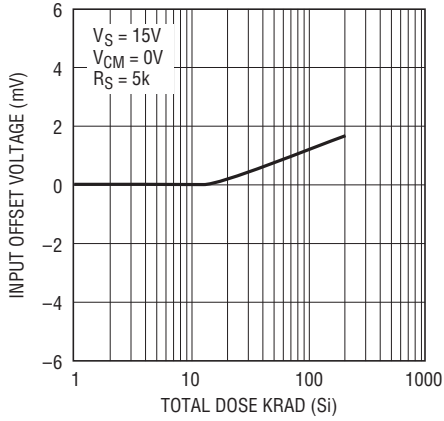
Analog Devices reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT

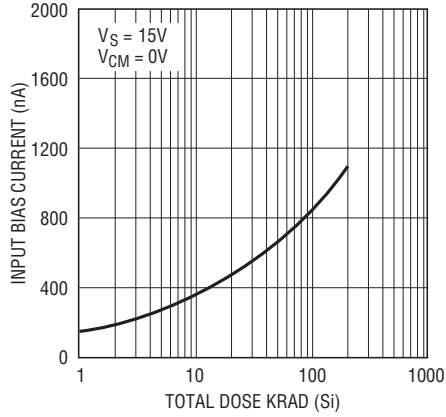


TYPICAL PERFORMANCE CHARACTERISTICS

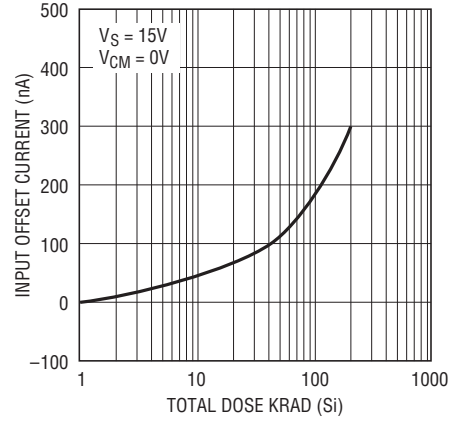
Input Offset Voltage



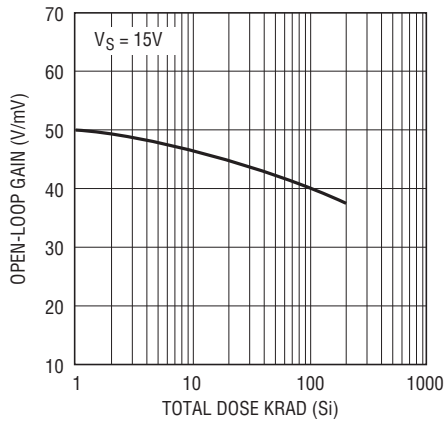
Input Bias Current



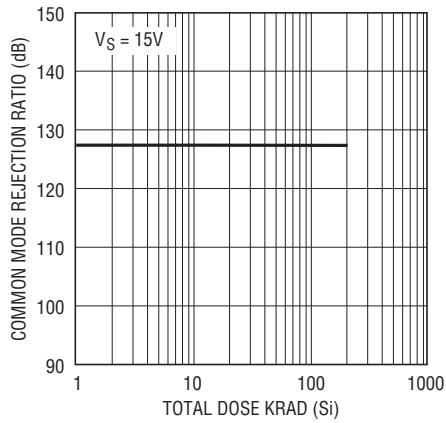
Input Offset Current



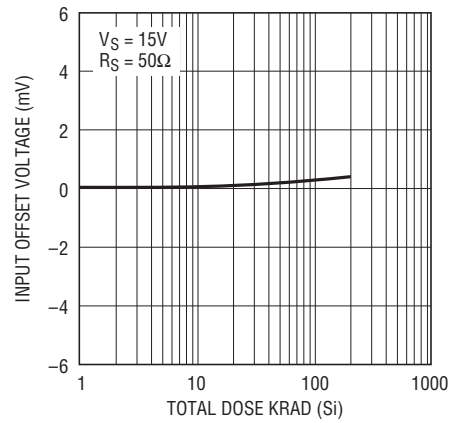
Open-Loop Gain



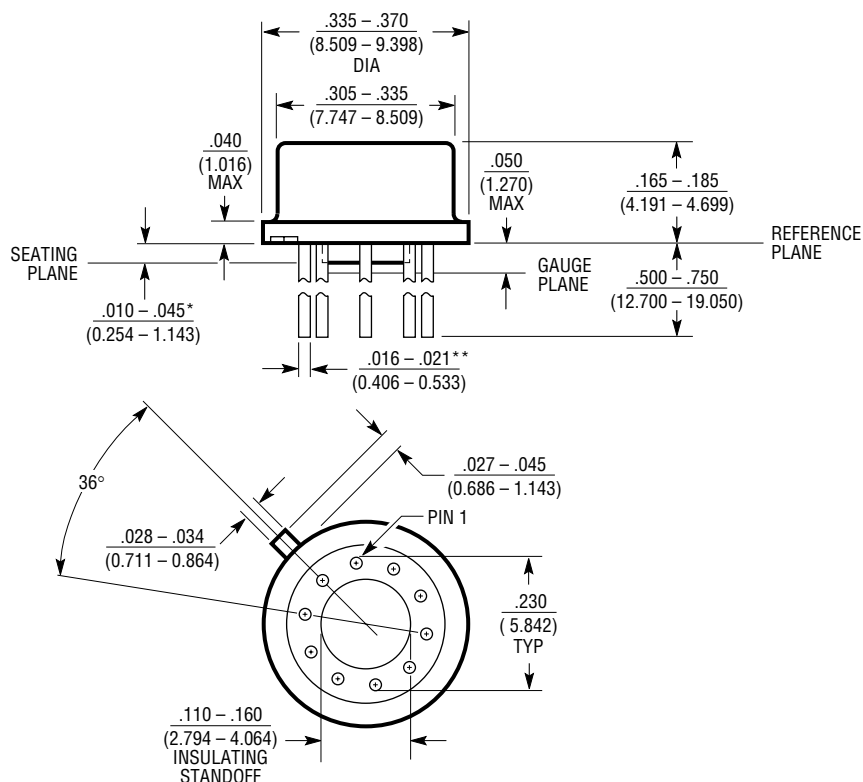
Common Mode Rejection Ratio



Input Offset Voltage



PACKAGE DRAWINGS

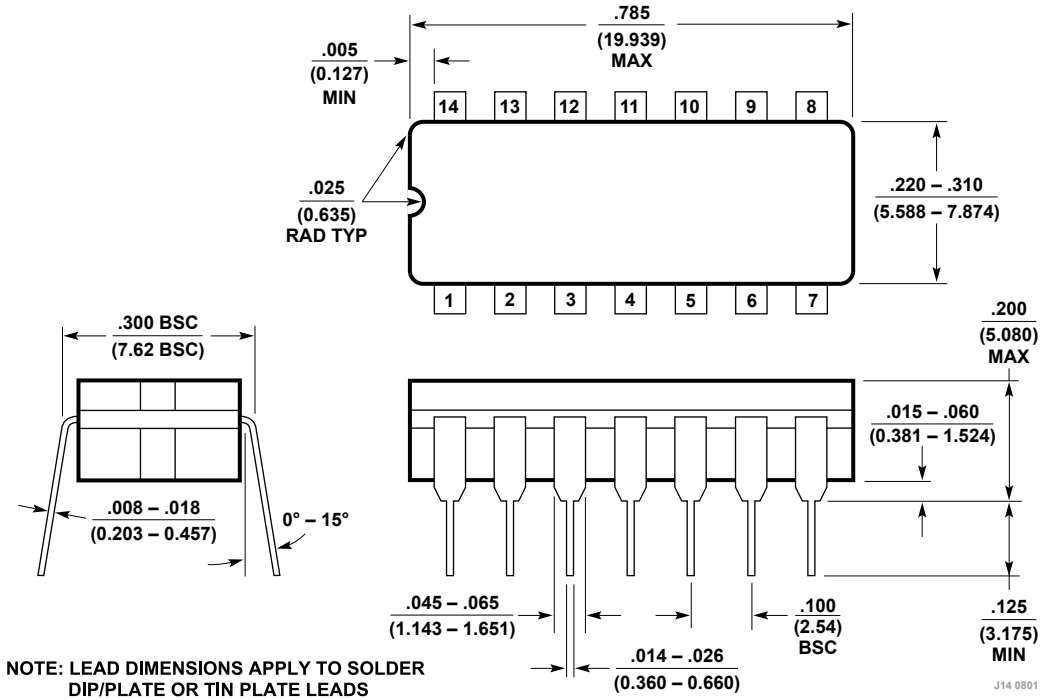


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $.016 - .024$ (0.406 - 0.610) H10(TO-5) 0204

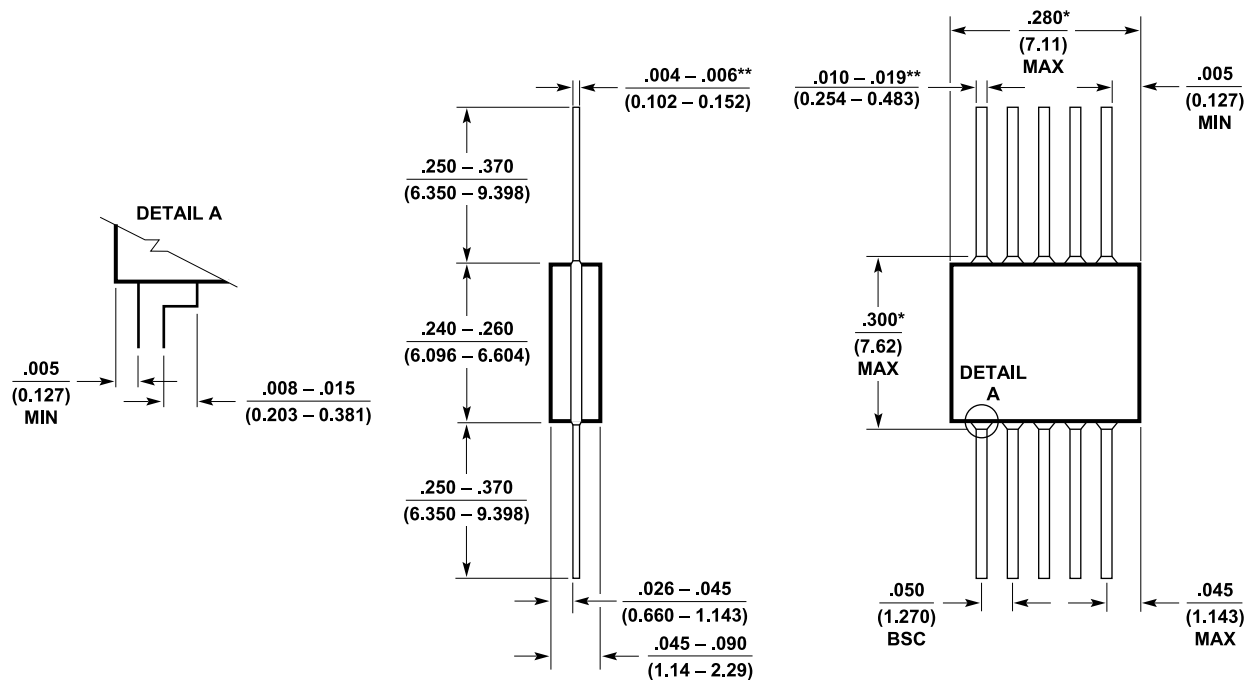
H Package
10-Lead TO-5 Metal Can
(Reference LTC DWG # 05-08-1322)

PACKAGE DRAWINGS



J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

PACKAGE DRAWINGS



NOTES:

*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN

**INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED)

W10 (GLASS) 0603

W Package
10-Lead Flatpak Glass Sealed (Hermetic)
(Reference LTC DWG # 05-08-1130)

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
D	04/19	Obsoleting J package and updating to ADI format	1-4
E	07/23	Updated art title in the Electrical Characteristics section	2
F	03/24	Updated Table 2	3
G	05/25	Changes to Table 1 and Table 1A and added Package Drawings	2, 5-7